International Journal of Engineering Research and General Science Volume 3, Issue 2, March-April, 2015
ISSN 2091-2730

REDUCING DYNAMIC POWER DISSIPATION IN LFSR USING LOOK AHEAD CLOCK GATING AND DOUBLE EDGE TRIGGERING

[1]G.Kalaiarasi ,[2]K.Sasipriya, [3]E.Roobashini, [4]K.Saranya
[1]Assistant professor , [2], [3], [4]UG Students
Department of Electronics and Communication Engineering
[1]kalaiibe@gmail.com, [2]sasipriya.ece2011@gmail.com,
JAY SHRIRAM GROUP OF INSTITUTIONS ,TIRUPUR

ABSTRACT: In normal LFSR consumes large dynamic power dissipation. A linear feedback shift register (LFSR) is constructed by N number of flip flops. LFSR is a shift register whose input bit is a linear function of its previous state. This novel paper presents the two methods to reduce power dissipation and increases the speed of the operation in LFSR. One of the method is LACG, it computes the clock enabling signals for each FF ahead of time and based on the present cycle data of those FFs on which it depend. It reduces the dynamic power dissipation. And other method is double edge triggering in which the FF is operate on both positive and negative edge of the clock cycle. So it increases the speed of operation. The power reduction 25% is achieved. Xilinx ise 8.1i is used for power analysis.

Index terms: clock gating, LACG, LFSR

I.INTRODUCTION

The main challenging area in VLSI area performance, cost, test, area, reliability and power. In this power consumption is major challenging. The power consumption increased due to the power dissipation in the circuits. Most of the power dissipation occurs due dynamic power. In normal LFSR consumes large dynamic power dissipation.

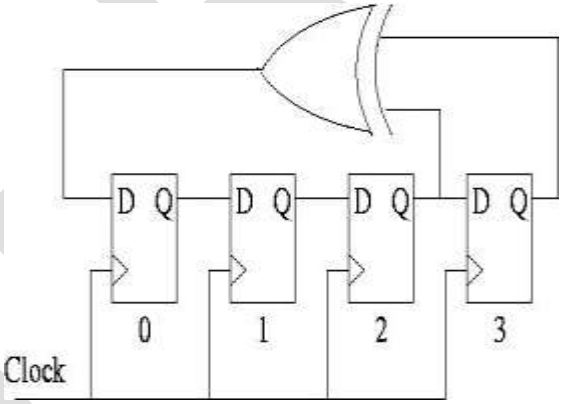

Fig.1.Normal LFSR

A linear feedback shift register is constructed by N number of flip flops. LFSR is a shift register whose input bit is a linear function of its previous state. In this continuous clock pulse is given as input[4]. LFSR is based on XOR or XNOR feedback logic is the initial value of the shift register, shift register taps and feedback logic determines the output sequence. The shift register taps is nothing but combination of XOR or XNOR logic and the feedback input to the shift register. LFSRs are very easy to implement.

The taps of an LFSR can be represented as a polynomial mod. It shows the coefficient of polynomial must be 1's or 0's. The powers of the terms represent the tapped bits, counting from the left. The first and last bits are always connected as an input and tap respectively.

In this major drawback is power dissipation, it occurs due to continuous clock pulse is given whether the data is toggle or not to the next state[4] and [5].

II.LFSR USING LACG AND DOUBLE EDGE TRIGGERING.

The proposed method to increase the speed of operation and reduce dynamic power dissipation there are two methods used. The methods are look ahead clock gating and double edge triggering.

LOOK AHEAD CLOCK GATING

The increased dynamic power dissipation in the digital system can be reduced by deactivating the clock signal to flip flop when the output signal is same as the input signal[3],[6] and [7]. There are several techniques has been developed for reducing dynamic power dissipation, the clock gating plays the major role. There are three techniques in clock gating: synthesis based, data driven method and auto gated flip flop. Synthesis based is deriving clock enabling signal for the flip flop based on the logic. In data driven method to reduce the overhead of the gating logic several FF are driven by the same clock signal generated by ORing the enabling signal of individual FF[1] and[2]. In auto gated FF the master slave ff is used to reduce the size and saving the power[1].

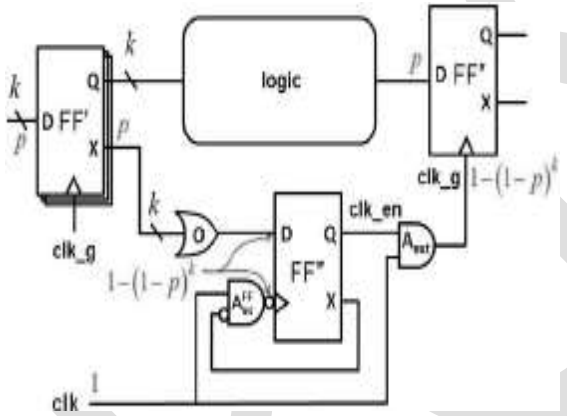

Fig.2. General logic of LACG

The look ahead clock gating is the combination of these three methods. LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depend[1] .LACG is very useful in reducing the clock switching power. The computation of the clock enabling signal one cycle ahead of the time avoids the tight time constraints existing in other gating methods.

Fig.2.illustrates the general logic for LACG. The FF' is the source and FF" is the target. The target FF is based on the source FF, it does not have any external input of the block. The XOR is used to perform XOR operation between the outputs of any two FF, it define the data to clock toggling probability. The AND gate is used to enabling the clock signal based on the clock gating and XOR output.

The overall block diagram is designed as a single block

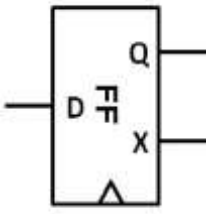

Fig.3. LACG flip flop

The separate gating logic for each target FF, it consumes the considerable amount of power and area[1]. The gating logic should be minimized, therefore in many cases target FF depend on the similar source FF. To develop logic sharing model to minimize the

gating cost. The ORing logic is merged and a single gater is used for the two FFs. In addition to logic reduction, the number of clock drivers and gaters will also be reduced.

The dynamic power overhead of LACG has been considerable in the break even analysis. There is also static power overhead. It should be noted that due to the full cycle allotted for the derivation of the enabling signals, the logic involved uses high threshold voltage and smallest device.

MODELING THE POWER SAVINGS

Let X be a random variable of the FFs data to clock toggling and let p=Pr[X=1] be it is probability[1]. The FFs are toggling their data independently of each other exists

$$\Pr[\sum_{X(D")} X(t) = 0] = (1-p)^k$$

Let X is independently that the probability of enabling the clock while it could be disabled is

$$\Pr[\sum_{X(D")} X(t) = 1\hat{}X"(t+1) = 0] = [1-(1-p)^k](1-p)$$

The power savings in terms of capacitance and data toggling probability, since the frequency and voltage do not matter for relative savings calculation. The product of capacitance and data toggling probability is called dynamic capacitance or cdyn. Let c_{FF} be the clock input capacitance of a FF and let c_{FF+CLK} include the clock driver. The net cdyn savings per target FF , denoted by C_{dyn}^{save} is

$$C_{dyn}^{save} = (1-p)^k(c_{FF} + CLK + c_{FF} + c_O) - p(C_x + kc_O) - (\frac{c_{FF}+CLK}{3} + c_{Aint} + c_{FF} + c_O)$$

The C_{dyn}^{save} is decreasing with the increase of p and k.

DOUBLE EDGE TRIGGERING

Most of the flip flops are designed to operate in single clock edge that is either operates in positive edge or negative edge. In double edge triggering the flip flop is made to operate in both clock edges. So, it will not waste the clock pulse and also speed of operation is increased.

III.OPERATION OF PROPOSED LFSR

The operation of LFSR using look ahead clock gating and double edge clock triggering as same a normal LFSR. In this input is given as clock gating, it deactivating the clock signal when there is no change in the state and when the output is same as the input signal[1]-[3],[6] and[7]. The clock gating it operates on the both clock edges are positive edge and the negative edge.

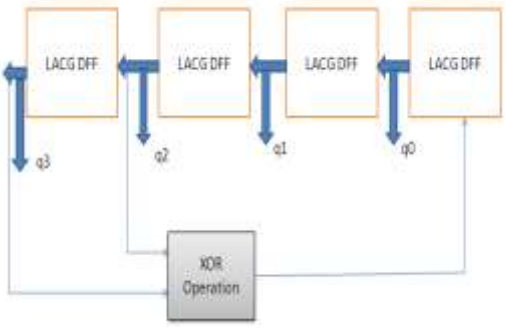

Fig.4.Proposed LFSR

In this LACG flip flop is used as four times as LFSR. The initial input to first LACG FF is XOR feedback logic. The output determines by initial value of shift register taps, shift register taps and XOR feedback logic. The tapped bits determine the polynomial mod. The characteristics polynomial is x^4+x^3+1.

The power terms are represented by tapped bits, it counting from the left. The output of 3rd and 4th bits are XORed and given as input to the initial FF. It reduces the dynamic power dissipation, increases the speed of operation, increases throughput and reduces the delay.

IV.APPLICATION OF LFSR

LFSR can be implemented in the hardware and it makes useful in applications that may require fast generation of a pseudo random sequence.

USES AS COUNTERS

The LFSR allows the repeating sequence of states is to be used as clock divider. LFSR counters have simpler feedback logic than natural binary counters or gray code counters and it operate at higher clock rates. It is necessary to ensure that the LFSR never enters an all zero state.

USES IN CRYPTOCRAPHY

LFSRs have been used as pseudo random generators for used in stream ciphers, due to construction from simple electro mechanical or electronics circuits and very uniformly distributed output streams.

USES IN DIGITAL BROADCASTING AND COMMUNICATION

SCRAMBLING:

To prevent short repeating sequences from forming that complicate symbol tracking at the receiver or it may interfere with other transmission, LFSR are often used as " randomize" the transmitted bit stream. This randomization removes at the receiver after demodulation. When LFSR runs at the same rate as the transmitted symbol stream, this technique is refer as scrambling[4]s. When the LFSR runs faster than the symbol stream the transmitted signal bandwidth is expanded, this is direct sequence spread spectrum.

VII.SIMULATION

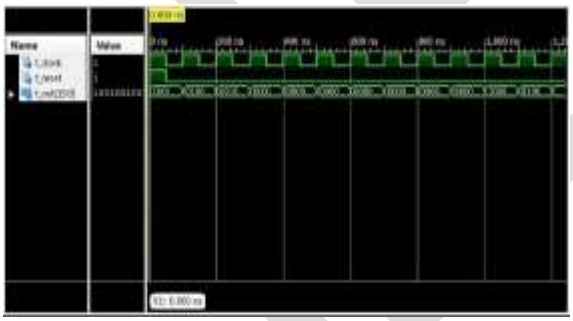

Fig.5.Waveform of normal LSFR

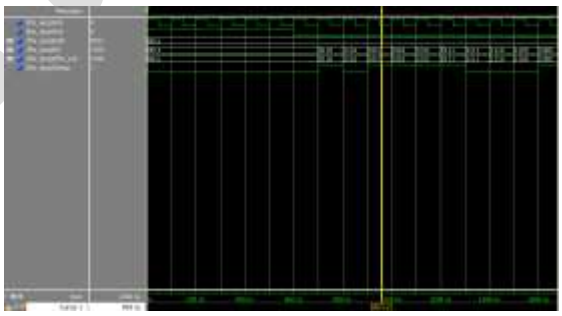

Fig.6.Waveform of proposed LFSR

V.EXPERIMENTAL RESULTS

The EDA tool is used to verify the circuit. In this Modelsim SE 6.5 is used analysis and run simulation output. Xilinx ISE8.1i is used for power analysis and gets synthesized output. The table.1.shows the comparison between LFSR and proposed LFSR. In order to evaluate the power reduction obtained by applying proposed LFSR, have evaluate the power consumption in the normal LFSR and power consumption proposed LFSR for same input vector and the same clock cycle. VHDL code of proposed LFSR was simulated and synthesized.

	LFSR	PROPOSED LFSR
TOTAL POWER	67.00 mW	63.00 mW
DYNAMIC POWER	33.33 mW	29.05 mW
QUIESCENT	27.00 m W	26.95 mW

Table.1.Comparison between LFSR and proposed LFSR

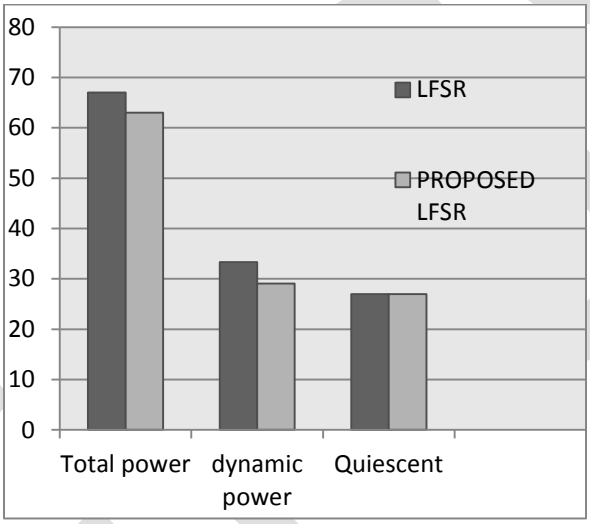

Fig.7. Comparison between LFSR and Proposed LFSR

VI.CONCULSION

The proposed LFSR has been shown to be very useful in reducing the dynamic power dissipation and increases the speed of operation. The proposed LFSR has been used in many application were at all normal LFSR is used. As, a result reduced dynamic power dissipation, increases speed, throughput and reliability.

REFERENCES:

1)Shmuel Wimer,and Arye Albahari," A Look-Ahead Clock Gating Based on Auto-Gated Flip-Flops,"IEEE Trans.VLSI Syst., VOL. 61, NO. 5, MAY 2014

2)S. Wimer and I. Koren, "Design flow for flip-flop grouping in data driven clock gating," IEEE Trans. VLSI Syst., vol. 22, no. 4, april 2014.

3) S. Wimer and I. Koren, "The Optimal fan-out of clock network for power minimization by adaptive gating," *IEEE Trans. VLSI Syst.*, vol. 20, no. 10, pp. 1772–1780, Oct. 2012.

4)Yasmeen Khan," Power Optimization of Linear Feedback Shift Register Using Clock Gating ," Volume 7, Issue 1 (May 2013), PP. 109-115 .

5)Anuja aravind and Raseena K.A,"Design of an ALU with a low power LFSR using Clock gating"IJSETR,Volume3,Issue 10, Oct.2014.

6)Priya singh and Ravi Goel,"Clock gating: A Comprehensive power Optimization Technique for Sequential Circuits" IJARCST,vol 2,Issue 2,Apr-June 2014.

7)Dr.Neelam R.Prakash and Akash,"Clock Gating for Dynamic power reduction in synchronous circuits", IJETT,vol.4,issue 5,may 2013