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REVIEW ON ERROR DETECTION AND CORRECTION

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Abstract— Majority logic decodable codes are suitable for memory applications because of their capability to correct large number of errors. Another method of decodable logic is Majority Logic Decoder/Detector which reduces not only the decoding time but also memory access time as well as area utilization. Euclidean Geometry Low-Density Parity-Check (EG-LDPC) codes are used for error correction, because of their fault-secure detector capability. EG-LDPC codes are used to avoid high decoding complexity. The application of a similar technique to a class of Euclidean geometry low density parity check (EG-LDPC) codes that are one step majority logic decodable. The obtained results show that the method is also effective for EG-LDPC codes. The proposed design of error detection and correction will coded using VHDL, verified and synthesize on Modelsim and Xilinx FPGA respectively.

Keywords— Fault detection, Error correction, Serial one step MLD, Majority logic decoder/detector, Memory, Soft error, Sorting network.

INTRODUCTION

Now a day, data communication is essential part of life and a lot of data has being transferred. Many communication channels are subject to channel noise, and therefore errors may be introduced during transmission from the source to a receiver. There are various ways of hacking, when the intruder modifies the data while communication. Not only to protect the confidentiality of the data but also to retain the correctness of the data, secure communication is very important. There are various methods of implementing the secure communication. Every method has its own advantages and disadvantages. This project is use for the improvement on most of the available methods for secure communication.

For reliable communication, errors must be detected as well as corrected. Some multi error bit correction codes are BCH codes, Reed Solomon codes, but in which the algorithm is very difficult. These codes can correct a large number of errors, but need complex decoders. Among the error correction codes, cyclic block codes have higher error detection capability as well as low decoding complexity and that are majority logic (ML) decodable. A low-density parity-check (LDPC) code is a linear error correcting code, used to avoid a high decoding complexity. one specific type of low density parity check codes, namely Euclidean Geometry-LDPC codes are used due to not only their fault secure detector capability but also higher reliability and lower area overhead.

To protect the memories from so-called soft errors error correction codes are commonly used, which change the logical value of memory cells without damaging the circuit. Memory devices become larger and more powerful error correction codes are needed, as technology scales. To end this, recently proposed the use of more advanced codes. These codes can correct a larger number of errors, but require complex decoders. The use of one step majority logic decodable codes was first proposed for memory applications, to avoid a high decoding complexity. One step majority logic decoding is implemented serially with very simple circuitry, but required long decoding times. This would increase the access time in memory which is an important system parameter.

Fig.1 shows the generic schematic of a memory system with MLDD. It consists of Encoder, Memory and MLDD.

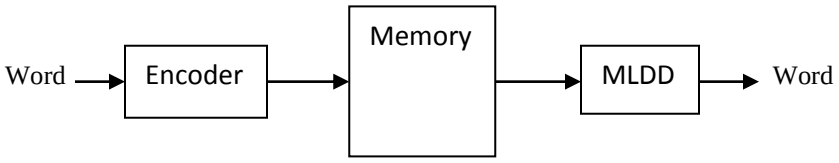

Fig -1: Memory system schematic with MLDD

First the data words are encoded and which is stored in the memory. When the memory is read then the codeword is fed through the MLDD before sent to the output for the processing. And this decoding process, the data word is corrected from all bit flips that it might have suffered while being stored in the memory.

LITERATURE REVIEW

[1]. Pedro Reviriego, Juan A. Maestro, and Mark F. Flanagan presented Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes. A method was proposed to accelerate the logic decoding of various set low density parity check codes. In the serial one step Majority Logic Decoder of EG-LDPC codes has been studied for the detection of errors during the first iteration. The objective was to minimize the decoding time by stopping the decoding process when no errors are detected. The obtained simulation results show that all the tested combinations of errors affecting up to four bits are detected in the first three iterations of decoding. These results are extend the ones recently presented for DS-LDPC codes, for memory application the modified one step majority logic decoding more attractive. The designer now has a larger choice of word lengths as well as error correction capabilities.

[2]. P. Kalai Mani, V. Vishnu Prasath, presented Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes. Error detection in memory applications was proposed to accelerate the majority logic decoding of various set low density parity check codes. LDPC is useful as majority logic decoding can be implemented serially with simple hardware but a large decoding time is required. For memory applications, this is increases the memory access time. This method detects whether a word has errors in the first iterations of majority logic decoding, if there are no errors then the decoding process is stop without completing the rest of the iterations. Therefore most words in a memory will be error free, and then the average decoding time is greatly reduced. The obtained results show that the method is also effective for EG-LDPC codes.

[3]. M. Pramodh Kumar, S. Murali Mohan, presented Serial one-step majority logic decoder for EG-LDPC code. In this brief, the detection of errors during the first iterations of serial one step Majority Logic Decoding of EG-LDPC codes has been studied. The objective was to minimize the decoding time by stopping the decoding process when no errors are detected. The obtained simulation results show that all the tested combinations of errors affecting up to four bits are detected in the first three iterations of decoding. These result was extend the ones recently presented for DS-LDPC codes.

[4]. Adline Priya, presented Low Power Error Correcting Codes Using Majority Logic Decoding. Moreover, the decoder architecture for LDPC codes are designed. And the simulation results for encoder, decoder, memory and detector are obtained. And also the majority logic decoder is implemented serially.

[5]. Senbagapriya. S. presented An Efficient Enhanced Majority Logic Fault Detection with Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes for Memory Applications. In this paper, the detection of errors during first iterations of serial one step Majority Logic Decoding of EG-LDPC codes has been presented. The obtained simulation results show that to decode a codeword of 15-bits the one step MLD would takes 15 cycles, which would be excessive for applications. The MLD design requires small area but large decoding time is required and which can be able to detect two or few errors. Hence, memory access time increases. Another method, called MLDD can detect up to five bit-flips and consumes the area of majority gate. These designs are under progress.

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CONCLUSION

In this paper majority logic decoder/detector can be detect the number of errors and correct it. Fault secure detector can be detect error and serial one step majority logic decoder can be correct these errors. MLDD have the capability of reduces the area of majority gate by using sorting network.

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