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Design & Implementation of MQAM based zigbee Transceiver using HDL

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Abstract— The present paper reports the Physical Layer implementation of 2.4 GHz-band MQAM digital transceiver for a Zigbee Application. A novel design method is proposed using Verilog HDL through Xilinx ISE 13.1. The digital transmitter is designed using Verilog. The Transmitter model is then implemented on Xilinx Spartan3E XC3S200E field-programmable gate array (FPGA). Simulations and Measurements verify the functionality of the designed transmitter. With the frequencies of 1 MHz and 8 MHz, the digital transmitter design matches theoretical expectation

Keywords— Zigbee, FPGA, Transceiver, HDL, Verilog.

INTRODUCTION

The development of wireless interface devices has made a strong demand for short-range low-data-rate wireless networking. This is the main motivation of development of Zigbee standard. The standard Zigbee is developed by the Zigbee Alliance [1]. It has hundreds of member companies, from the software developers and semiconductor industry to original equipment manufacturers (OEMs) and installers. In 2002 the Zigbee Alliance was formed as a nonprofit organization [2]. The Zigbee standard has accepted IEEE 802.15.4 Medium Access Control (MAC) and Physical Layer (PHY) protocols [3]. The Physical layer PHY supports three frequency bands: 2.45 GHz band with 16 channels, 915 MHz band with 10 channels and 868 MHz band with 1 channel.

In this research we will only focus on used 2.45 GHz band which is worldwide acceptable with data rate 250 kbps. The MAC layer supports two types of nodes; one is Reduced Function Devices (RFDs) nodes and another is Full Function Devices (FFDs). RFDs can only behave as end-devices and are comprised of actuators or sensors like lamps, light switches and transducers. They can interact only with a single FFD [4]. FFDs are comprised of a full set of MAC layer functions, by which they can act as a network end-device or a network coordinator [4].

The Zigbee networking topologies are classified into mainly two types: peer-to-peer and star. In the peer-to-peer topology, if the devices are close enough to establish a successful communication link, each device can directly communicate with any other device. In the star topology, every device can communicate only with the central personal area network (PAN) coordinator in the network. The central node or PAN coordinator is FFD and other nodes can be RFDs or FFDs. [2].

The IEEE 802.15.4 defines four MAC frame structures: MAC command frames, data, beacon and acknowledgment. The MAC command frame carries MAC commands. The data frame carries data to be transmitted .The coordinator use beacon to transmit beacons. The beacons are used for synchronizing the clock of all the devices which are in the same network. In the meantime, the acknowledgement frames are used to confirm successful frame reception [3].

LITERATURE ANALYSIS

There are many wireless control and monitoring applications for home and industrial environments which need less complexity, lower data rates and longer battery life than those from existing standards. What the world requires is a globally designed standard that meets the requirement for low power, security, reliability and low cost. Zigbee defines a set of communication protocols for low data rate, short range wireless networking. Since Zigbee and its underlying standard IEEE 802.15.4 are recent, there has been little research investigating the power and area consumption, speed of operation and performance. The broad area of problem is that designing a Zigbee transmitter in order to attain improvements in terms of area, power and performance.

The Zigbee standard is designed by Zigbee Alliance, which has adopted IEEE 802.15.4 as its Physical layer (PHY) and Medium Access Control (MAC) protocols. Zigbee standard is developed to address the need for implementation of low data rate, very low cost wireless networks with ultra-power consumption. The Zigbee standard reduces the implementation cost by reducing the data rate and simplifying the communication protocols. The minimum requirements to meet IEEE 802.15.4 and Zigbee specifications are relatively relaxed than other standards such as IEEE 802.11, which reduces the cost of implementation and complexity of Zigbee Transceivers.

The digital part of transmitters can be designed either with Matlab, schematic or hardware description language (VHDL, VERILOG). However, schematic approach is suitable for large designs, where usually more logic functionality is involved. Shuaib et al. [5] developed and simulated the zigbee transmitter using Matlab. Unfortunately, this design has not been implemented yet.

In contrast, Meng et al. [6] has designed, tested and implemented the Zigbee receiver with Harris SIP transceiver. The receiver was

designed by using VHDL and tested on Xilinx Virtex-4 FPGA. The receiver consists of IF down-conversion, carrier synchronization, chip synchronization and dispreading blocks, filtering quadrature demodulation. The implementation results showed that the slices used are up to 11%, with 6% flip-flops and 7% look-up-tables (LUTs) usages.

Another Zigbee transmitter is modeled by Rahmani [7] using VHDL on Spartan-2 FPGA board. The transmitter architecture comprises of bit-to-symbol encoder, symbol-to-chip mapper and offset quadrature phase-shift keying (OQPSK) modulator. The Design utilization summary showed 150,000 gates have been used. Above two papers prove that the VHDL instruction requires large number of slices. Therefore, it leads to a large design size.

In present paper, Using Verilog a novel design approach for the digital Zigbee transmitter is proposed, and is then implemented on FPGA. FPGA is an integrated gate array developed to be configured by the designer or customer at Field. Fig.4 shows the FPGA board which is used in this research work. The Spartan3E family is designed specifically for high-volume and cost-sensitive needs of consumer electronic applications and it's combined with advanced 90 nm technology process [8]. The combine usage of Verilog and FPGA enable the transmitter developed in a shorter timeframe. In comparison with schematic and VHDL, The implementation is also more efficient.

The rest of the paper is organized as follows. Section III discusses the transmitter architecture. Section IV highlights results and discussion. Finally, Section V presents the conclusion.

TRANSCEIVER ARCHITECTURE

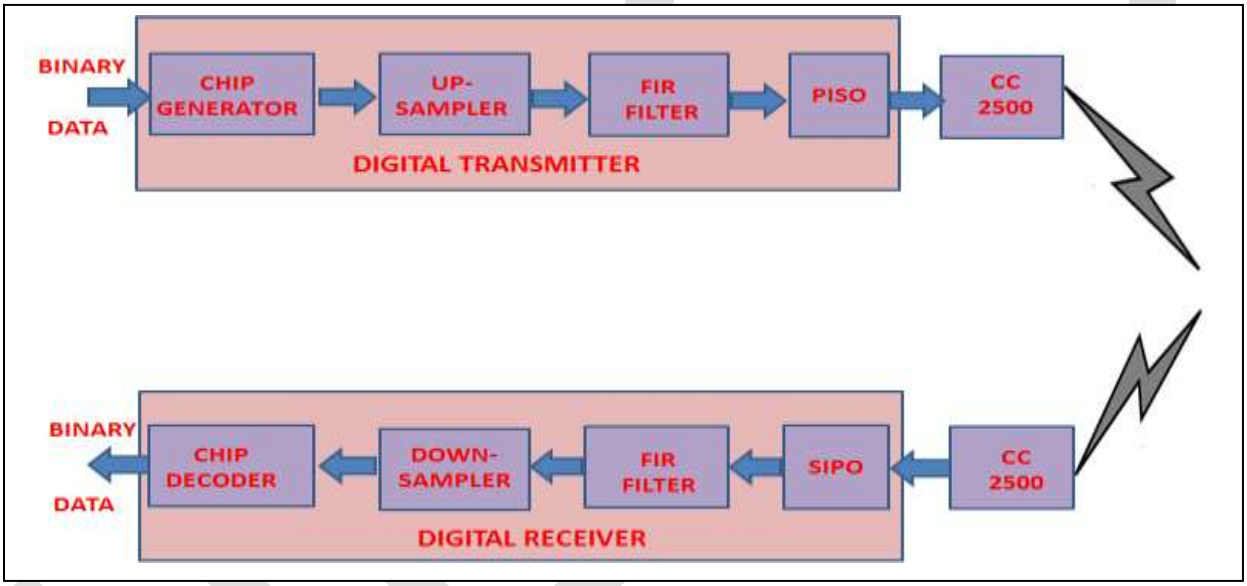

Figure: 1. Block diagram of zigbee transceiver.

For 2.4 GHz band zigbee applications, sixteen channels are available with 5 MHz ample channel spacing .The Transceiver architecture is shown in fig.1. The binary data is first applied to chip generation block which first maps each four bits into one symbol .Then each symbol is mapped into eight bit p-n chip sequence.as shown in table 2. After that each bit of p-n sequence is up sampled to match nyquist criteria .The even bits are up sampled by "up sampler-I", and odd bits are up sampled by "up sampler- Q".

These up sampled bits are passed through separate Fir filters. The output of up sampler-I is passed through filter Fir-I and output of up sampler-Q is passed through filter Fir-Q.

These filters are nothing but half cosine pulse shaping filter's which is reduces the digital noise. The output of FIR is 10bit block which is then transmitted to "CC2500" module serially by parallel in serial out (PISO) block. "CC2500" module transmits incoming packets to wireless channel.

At receiver side "CC2500" receiver module receives the packets serially & serial in parallel out (SIPO) converts the serial packets into parallel blocks. These parallel packets are the applied to FIR filter. The output of FIR filter is then down sampled by down sampler. The output of down sampler is the applied to chip decoder. The chip decoder decodes incoming chip signal and at output

gives corresponding four bit symbol. This data is then applied to parallel to serial convertor which gives serial stream of original binary data sent by transmitter.

RESULT AND DISCUSSION

SIMULATION AND WAVEFORM

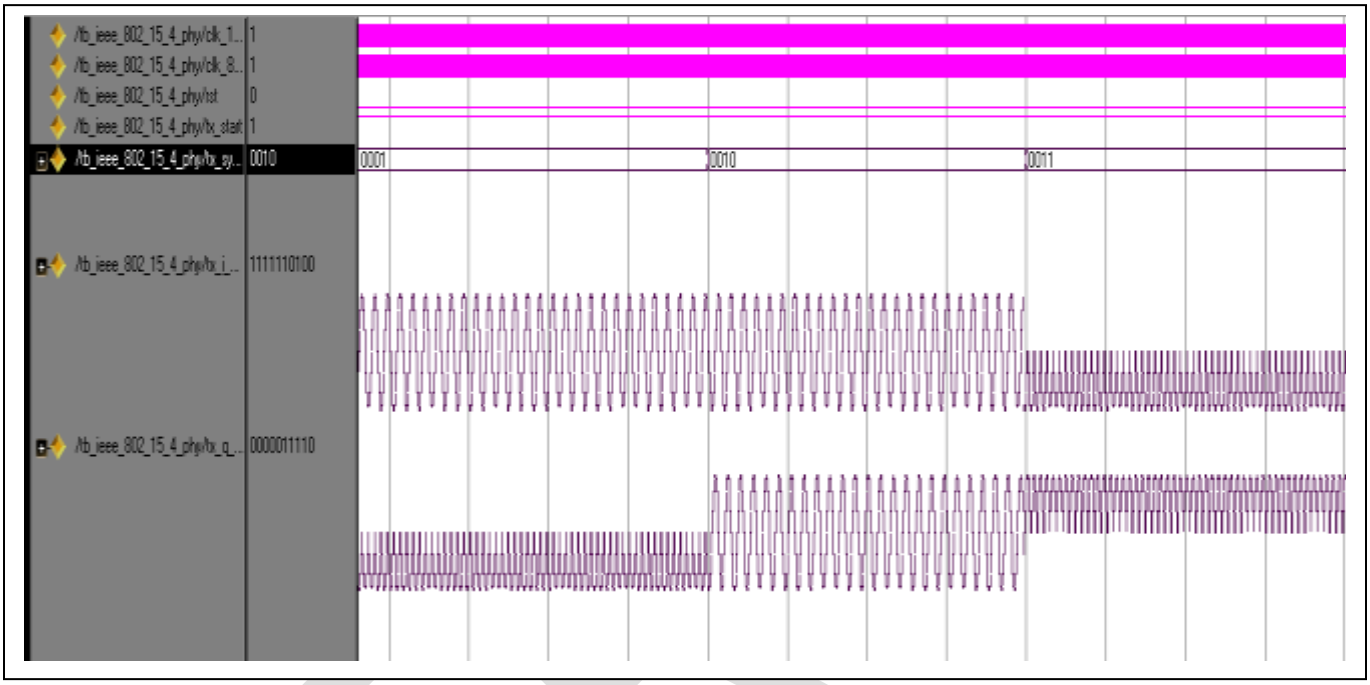

Figure: 2. Output Simulation Waveform on Modelsim 6.2 C simulator.

Fig.2. shows the simulation waveform for zigbee transmitter. The waveforms for I-channel & Q-channel for various symbols are shown in figure. For simulation Mentor Graphics "modelsim 6.2 C" tool is used .The 1 MHz & 8 MHz clocks are applied to transmitter, Logic high is applied to the "start" bit of transmitter. Then negative edge trigger is applied to "reset" bit.

RTL SCHEMATIC

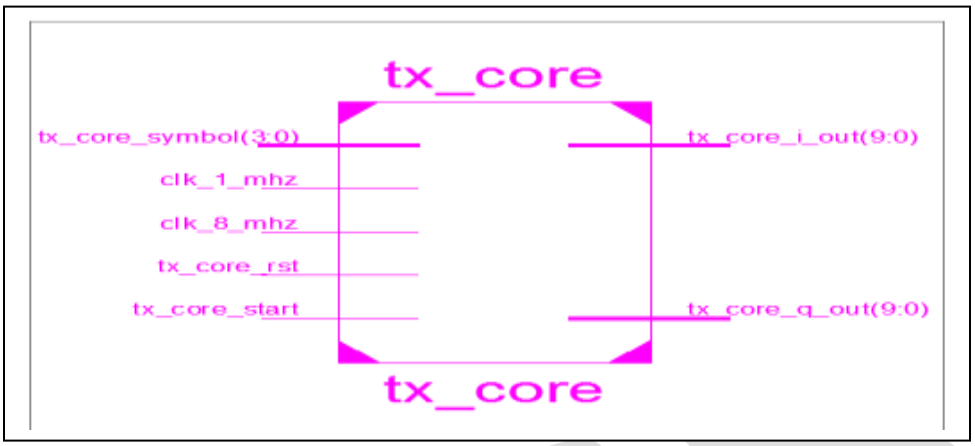

Figure: 3. RTL schematic of Zigbee Transmitter.

The digital transmitter structure is shown in Fig.3. The "clk_1_mhz" and "clk_8_mhz" are the clock frequencies of 1 MHz and 8 MHz, respectively. The input ports are comprised of "tx_core_symbol(3:0)", "tx_core_rst", "tx_core_start". The "tx_core_i_out (9:0)" and "tx_core_q_out (9:0)" are the output ports of I-phase and Q-phase signal, respectively.

DESIGN UTILIZATION SUMMARY

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	272	1920	14%
Number of Slice Flip Flops	102	3840	2%
Number of 4 input LUTs	509	3840	13%
Number of bonded IOBs	28	141	19%
Number of GCLKs	2	8	25%

Figure: 4. Design Utilization Summary of Zigbee Transmitter.

CONCLUSION

The Transmitter Block of Zigbee Transceiver is developed on Xilinx 13.1 ISE and tested successfully. The implementation of transmitter is done on Xilinx Spartan 3E XC 3S200 FPGA. The data transmission is also verified by receiving packets at computer. The simulation has been performed using modelsim 6.2 C simulator .The waveform matches with theoretical expectations. The

remaining part of the transceiver will be designed and synthesized in future

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