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VHDL based Sobel Edge Detection

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Abstract — Edge detection of an image is the primary and significant step in lower level image processing. This edge detection technique finds significant applications in various fields which mainly includes object tracking, image analysis, image segmentation etc. This paper mainly focuses on sobel operator based edge detection for real time applications using FPGA. Due to the better noise sensitivity as compared to other operator sobel operator is mainly used. The proposed architecture is coded using VHDL; synthesis is done using Xilinx ISE 13.1 and targeted for Xilinx vertex 5 FPGA platform. There is much reduction in the FPGA resources which reduces the area of the FPGA. The proposed model precisely detects edges of an image.

Keywords — FPGA , Gradient operator, Image processing, Matlab, Sobel edge detection, VHDL, Xilinx system generator.

INTRODUCTION

Real-time image processing is widely used in different applications such as video surveillance, traffic management and medical image processing. These operations frequently require digital signal processing (DSP) algorithms for numerous vital operations [2]. The processing of two dimensional images via computer is called as Digital Image Processing. Sampling and quantization is used to obtain a digital image from real image. The process of locating edges of an image is termed as Edge detection. Edge detection of an image is a very significant step for understanding features of images. Edges consist of noteworthy features and contained important information. It reduces the size of the image and filters out information that is treated as less relevant, preserving the important properties of an image [4]. So this edge detection proposal can be used in image processing field for motion detection and object tracking. Edges can be classified depending upon their intensity values like Ridge Edge, Step edge, Ramp Edge. The four basic steps used for edge detection are smoothing, Enhancement, Detection and localization. There are several edge detection algorithms such as canny, Robert, Prewitt and Sobel but the proposed work is designed by using Sobel Edge detection. FPGA hardware is widely used for implementing image processing algorithms because it can be easily used to implement nearly all digital logic function. Logic functions can be designed by writing VHDL/Verilog code. Then this VHDL code is converted into bit file and targeted on FPGA. The proposed design is implemented on Vertex 5 Xilinx FPGA because Xilinx provides most resourceful devices. FPGAs are the RAM Based Devices with some special routing resources to implement competent arithmetic functions like comparators, counters, adders whereas CPLDs are EEPROM based devices and do not have routing resources. Microcontrollers are considered to be not much useful when we implement image processing algorithms on embedded platform. With the arrival of Field Programmable Gate Arrays it becomes an alternative option for the efficient realization of algorithms of image processing on ASIC as it offer speed compared to an ASIC and is easy to reconfigure [6]. Look up tables (LUTs), registers and flip flops can be used for area optimized implementation. The proposed designs is implemented by using serial architecture by taking better benefit of look up tables, flip flop and shift registers present on the target device. The fully-parallel design is not able to share much hardware and consume more amounts of resources. Hence to minimize hardware requirement an efficient implementation of such filters has very much importance.

SOBEL EDGE DETECTION

For the detection of edges the Sobel operator is extensively used. The proposed algorithm is briefly explained below. In Sobel operator two filters Hx and Hy are mainly used

$$Hx=\begin{bmatrix}-1 & 0 & 1\\ -2 & 0 & 2\\ -1 & 0 & 1\end{bmatrix} \text{------(1)} \quad \text{and} \quad Hy=\begin{bmatrix}-1 & -2 & -1\\ 0 & 0 & 0\\ 1 & 2 & 1\end{bmatrix} \text{------(2)}$$

The gradient components across the neighboring lines or columns are computed by these filters correspondingly. This gradient magnitude defines local edge strength and is given by equation (3).

$$GM(x,y)=\sqrt{Hx^2 + Hy^2} \text{ - - - - - - - - - (3)}$$

Due to square root and square operations for each and every pixel this expression (3) is computationally expensive. So the square and square root operations are approximate by absolute values.

$$GM(x , y) = | Hx | + | Hy | \text{ - - - - - - -(4)}$$

This expression (4) can be easily computed and helps in preserving the edges in images/video. The above mentioned process is applied separately for each and every pixel of an image and the final edge plot is calculated by aggregating the edge maps of all channels.

PROPOSED MODEL

The proposed model for Sobel Edge Detection by using XSG is shown in Fig. 1. The Input and Output Image are blocksets of simulink where the block can read/write image from/into Matlab workspace. The Pre-processing unit and Display Controller Unit that transfer the image into the appropriate standard for next entity are also present in simulink blocksets. Here the Sobel Edge Detection algorithm is designed by using blocksets of Xilinx.

Figure 1: Proposed Model

DESIGN METHODOLOGY

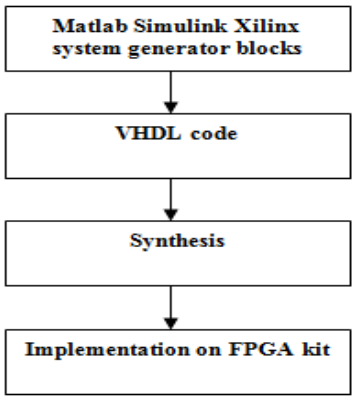


Figure 2: Design Methodology

Design methodology consists of designing of 2D filter in Matlab. Synthesis and optimization is done using VHDL Programming using Xilinx ISE design suite 13.1 and vertex 5 FPGA platform is used for the hardware implementation as shown in figure 2.

SYSTEM IMPLEMENTATION

1.BLOCK DIAGRAM FOR IMAGE PRE-PROCESSING

Figure 3 represents image pre-processing operation. Most important implication of image pre-processing is data serialization with appropriate data rate for the hardware implementation purpose.

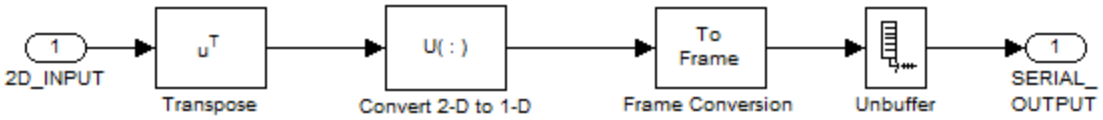


Figure 3: Image pre-processing

2. BLOCK DIAGRAM FOR IMAGE POST-PROCESSING

Figure 4 represents image post-processing operation. Most important implication of image pre-processing is to make data available for displaying in Matlab workspace with proper data rate.

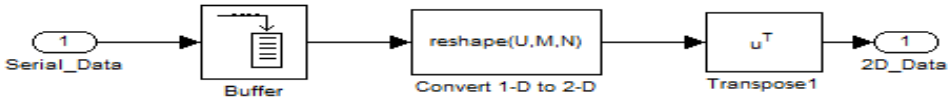


Figure 4: Image post-processing

3. HORIZONTAL GRADIENT FILTER FOR SOBEL OPERATOR

Figure 5 represents horizontal filter required for sobel edge detection. By moving horizontal kernel of 5×5 over an image horizontal gradient of an image is computed for sobel edge detection.

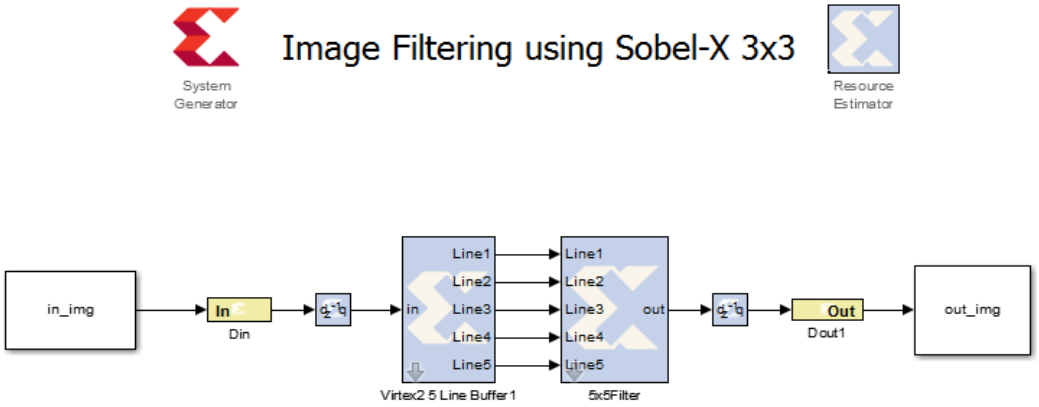


Figure 5: Horizontal Gradient Filter

4. VERTICAL GRADIENT FILTER FOR SOBEL OPERATOR

The vertical filter for sobel edge detection is shown in figure 6. By moving vertical kernel of 5×5 over an image vertical gradient of an image is computed for sobel edge detection. Here the same blocksets of Xilinx are used as that of horizontal gradient but we have to select vertical gradient by double clicking on 5×5 filter.

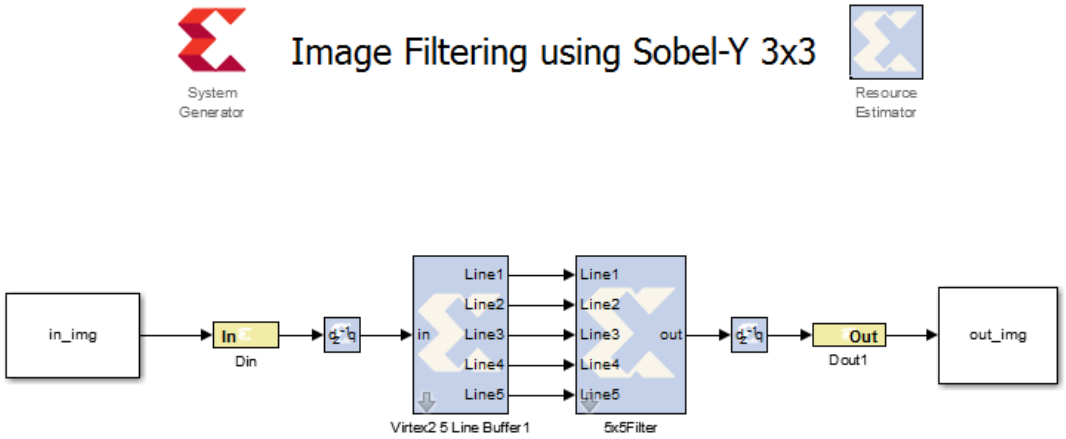


Figure 6: Vertical Gradient Filter

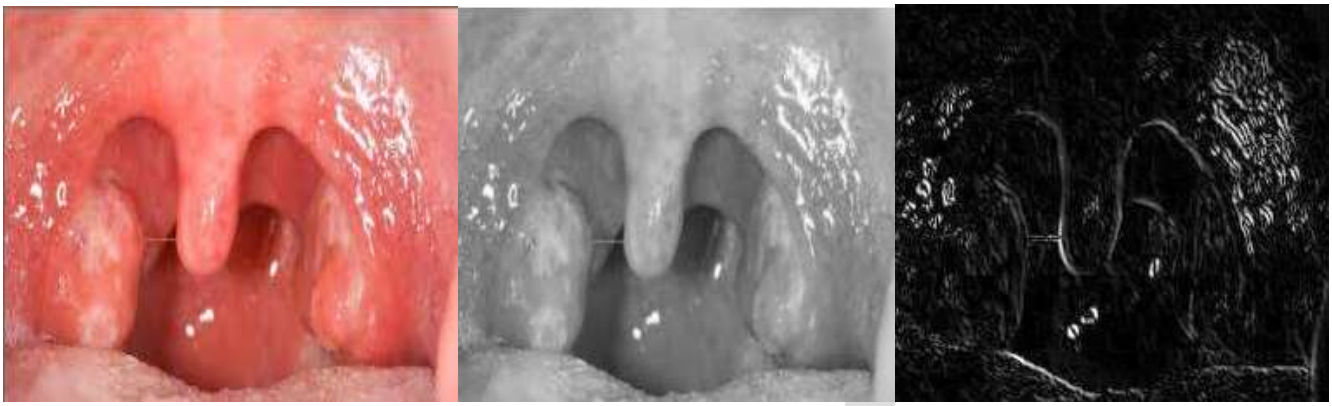
5. VHDL CODE GENERATION

Figure 6 indicates how the VHDL code is generated for the entire sobel edge detection model. The system generator is a token that serves as a control panel for controlling the system and parameters during simulation. Every Simulink design should contain at 1least one System Generator token.. This VHDL code is stored in the target directory.

Figure 7: VHDL code generation

RESULT AND ANALYSIS

The proposed design is implemented by using Matlab Simulink and Xilinx System Generator with blocksets of Xilinx. The method is tested on tonsillitis image as shown in figure 8. The output results show an edge detected image using Xilinx system generator and FPGA platform. The generated system is targeted for VIRTEX 5 FPGA kit. System Generator token is used for VHDL code generation. The generated code is synthesized using xilinx ISE 13.1 design Suit. After synthesis the device utilization summary is obtained for the targeted device.



(a) (b) (c)

Figure 8: (a) Input Image; (b) Converted grayscale image; (c) Edge detected output image

Further this sobel edge detection algorithm is tested on staircase Railings image and the result obtained is shown in figure 9.

(a) (b) (c)

Figure 9: (a) Input Railing Image; (b) Converted grayscale image; (c) Edge detected output image

Table 1 shows the device utilization summary generated for virtex 5 FPGA kit.

Logic utilization	**Used**	**Available**	**Utilization**
Number of slice Register	524	32,640	1%
Number of slice LUTs	297	32,640	1%
Number used as logic	193	32,640	1%
Number used as Memory	95	12,480	1%
Number used as shift Register	95	12,480	1%
Number with an unused Flip Flop	14	538	2%

Number of fully used LUT-FF pairs	283	538	52%
Number with an unused LUT	241	538	44%

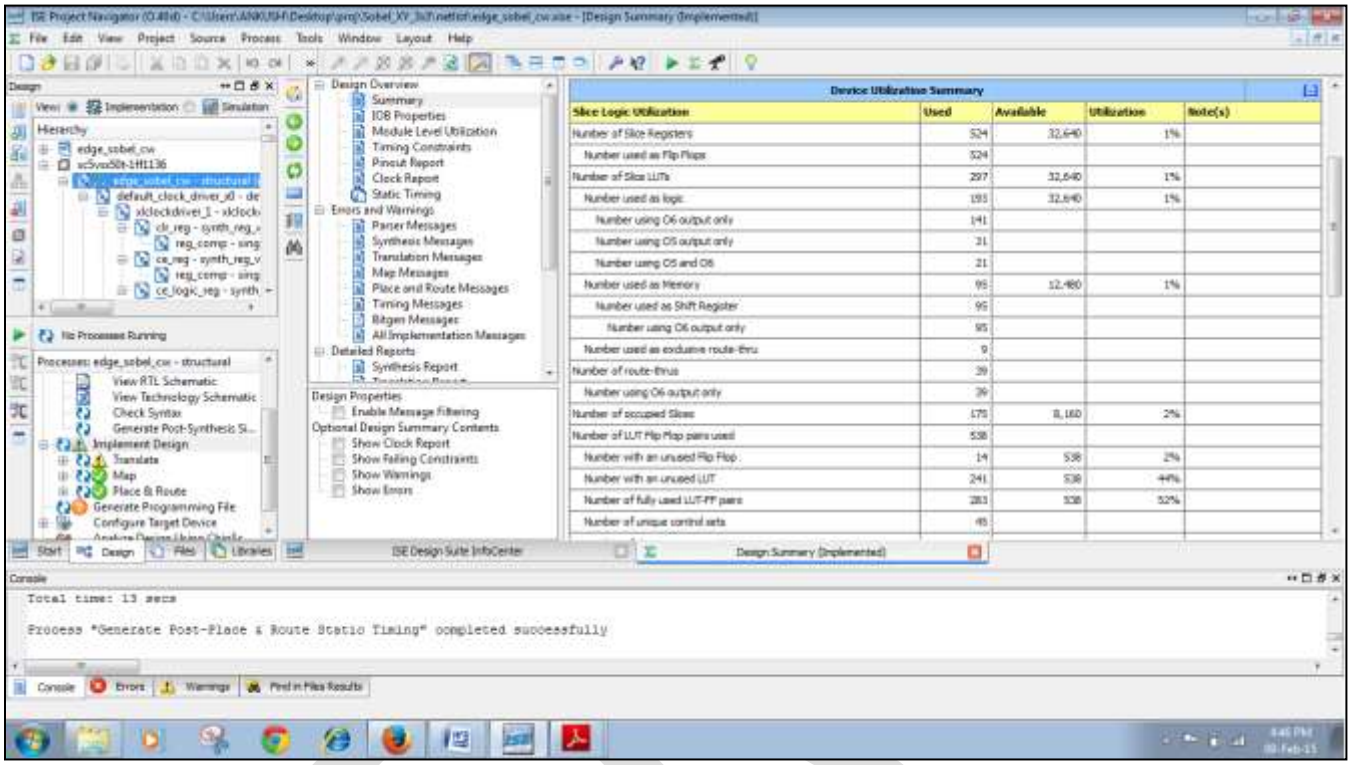


Figure 10: Device Utilization Summary for Virtex 5 FPGA kit

CONCLUSION

This paper presents the hardware and software architecture for the Sobel operator based edge detection which is designed for Xilinx vertex 5 FPGA platform. This architecture significantly reduces the FPGA resources usages (area). There is much reduction in the FPGA resources. This method reduces the complication of the system and thus the processing time. The time required for the execution of complete model for edge detection of a picture size 256×256 is only some seconds. The edges of the given gray image can be located rapidly and powerfully through this approach. Since this approach is free of multiplier, area is optimized. Pipelining can be used in order to improve the speed and effectiveness.

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