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Efficient reversible multiplier using column bypass technique for dsp applications

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Abstract—Power dissipation is one of the important criteria in VLSI system. Reversible logic computation is one of the efficient ways to minimize power which has the property of logical and physical reversibility. This paper presents an efficient 4x4 reversible multiplier using column bypass technique through which the switching activity is reduced. Since the design focus is to implement a reversible multiplier, proper selection of gate is also necessary. It must have not only reversible property, but also be fault tolerant. However, the major constraints in reversible logic are to minimize the number of garbage outputs & reduce the delay. Hence by this technique, power dissipation is controlled with reduced number of garbage values.

Keywords: Reversible logic, Constant input, Garbage output, Reversible multiplier, partial product, multipliers, XILINX.

I. INTRODUCTION

In the nano-scale design of today's circuits, the power consumption which leads to heat dissipation in computer machinery has become one of the major challenges and attracts the attention of many researchers. Power dissipation is an important factor in VLSI design as modern logic circuits offer a great deal of computing power in a small footprint. The logic elements are normally irreversible in nature and according to Landauer's principle [1] irreversible logic computation results in energy dissipation due to power loss. This is because; erasure of each bit of information dissipates at least KTln2 Joules of energy where K is Boltzmann's constant and T is the absolute temperature at which the operation is performed. Also, as Moore predicted that the number of transistors approximately doubles in every eighteen months and if this trend continues to hold, in the near future more and more energy will be lost due to the loss of information.

This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s. Charles Bennett [2] showed that energy loss could be avoided or even eliminated if the computations are carried out in reversible logic and also proved that circuit built from reversible gates have zero power dissipation.

Reversible computation has emerged as a promising technology having applications in low power CMOS, nanotechnology, optical computing, optical information processing, DNA computing, bioinformatics, digital signal processing and quantum computing. It is very clear that reversible circuits will play dominant role in future technologies.

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): Refers to the cost of the circuit in terms of primitive gates. It is calculated knowing the number of primitive reversible logic gates (1 x 1 or 2 x 2) required to realize it.

Multipliers are an integral part of many computational units. It is important for every processor to have a high speed multiplier. Multiplication is an essential arithmetic operation for common DSP applications such as Filtering, computation of FFTs etc. High end DSP processors also need to cater to the execution speed, accuracy of the results and also keep an eye on the power consumption. To achieve this, parallel array multipliers are used, where there is a need to check power efficiency.

A. Contribution

In this paper, we have proposed a reversible 4x4 column bypass multiplier circuit using Taffoli gate (TG) and Peres gate (PG) for partial product generation. We have also used two new gates, Mux Full Adder gate (MFA) and Mux Half Adder gate (MHA) along with Haghparast-Navi gate (HNG) and Peres gate (PG) for the summation circuit. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost, and this design can be generalized to construct reversible n x n multiplier.

B. Organization

The paper is organized into the following sections. Section 2 is an overview of basic reversible gates. The background work is described in section 3. Section 4 is about the new reversible gates. The proposed multiplier design is described in section 5. Results and discussion of the proposed design is presented in section 6. Conclusions are contained in section 7, and a comprehensive list of references has also been provided.

II. REVERSIBLE GATES

A. Basic reversible gates

1) Feynman Gate*:* Fig.1 shows a 2x2 Feynman gate [3]. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

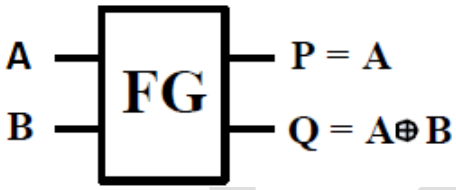

Fig. 1 Feynman gate

2)Toffoli Gate: Fig 2 shows a 3x3 Toffoli gate [4] the input vector is I (A, B, C) and the output vector is O (P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

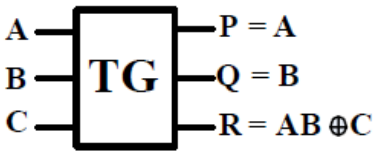

Fig. 2 Toffoli gate

3)Fredkin Gate: Fig 3 shows a 3x3 Fredkin gate [5]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

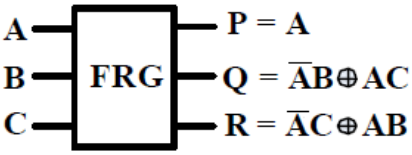

Fig. 3 Fredkin gate

4) Peres Gate*:* Fig 4 shows a 3x3 Peres gate [6]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

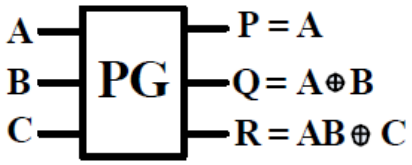

Fig. 4 Peres gate

5) Haghparast Navi Gate(HNG)*:*Fig.5 shows HNG gate [7].The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S). The outputs are defined by the following equations: P=A, Q=B, R=A⊕B⊕C and S= (A⊕B)C⊕AB⊕D. When D=0 HNG gate can be used as FA.

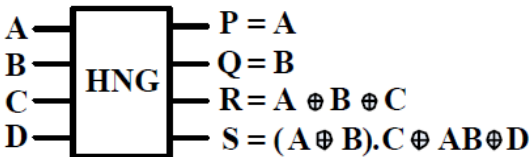

Fig. 5 HNG gate

B. Reversible multiplexer

1) PV Gate*:* Fig 6.shows a 3X3 PV gates which is a reversible multiplexer. The input vector is I(S, A, B) and output vector is O (P, Q, R). The outputs are defined by P=S, Q=S'A+SB, R=SA+S'B. S can be used as select line.

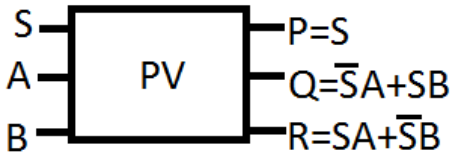

Fig. 6 PV gate

III. RELATED WORKS

In the recent years many reversible circuits as a replacement for conventional irreversible circuits have been proposed. On the other hand, because of the extensive use of multipliers in computer systems, several reversible circuits for implementing multipliers have been proposed [8-11]. For example, in [8], Haghparast et al. have introduced a two-part reversible multiplier circuit. The first part is for partial product generation and the second part takes the result from the first part and performs addition for producing the final result. The design uses an array of 16 PG gates for partial product generation and then addition is accomplished using a circuit which consists of PG [7] and HNG [5] gates. Another study in reversible multiplier design has been proposed by Rakshith Saligram and Rakshith T.R [12]. Their paper presents the design of 4x4 reversible multiplier employing column bypass and 2-dimensional row and column bypass techniques. The reversible column bypass multiplier has three computational units namely the product unit, the full adder unit and the column bypass unit. Peres gate (PG) is used to compute the partial products and full adder unit comprises of Double Peres gate (DPG) which is used in the last row of the multiplier as a ripple carry adder. Column bypass unit is a combination of Double Peres gate (DPG) and Fredkin gate (FRG) and is used in the carry save adder stages. Here Fredkin gate (FRG) functions as a multiplexer which chooses the sum term when column bypass control input (CBCI) is 1 and the partial product term if CBCI is 0.
Another study in multiplexer design has been proposed by Praveen.B and Vinay Kumar S.B [13]. A 3x3 reversible PV gate is proposed in order to function as a 2:1 multiplexer. Based on the select input S, the corresponding message bits are passed on to the output Y. Our proposed design is compared with the existing works based on four main parameters: number of garbage outputs, number of constant inputs, number of gates and quantum cost.

IV. PROPOSED REVERSIBLE GATES

A. MHA gate

Fig .7 shows the proposed 4 x 4 reversible MHA gate. The inputs are I(A,B,C,D) and their corresponding outputs are O(P,Q,R,S). If C=0 it works as a half adder. Input D acts as the select line. Carry is generated at P and Sum at S.

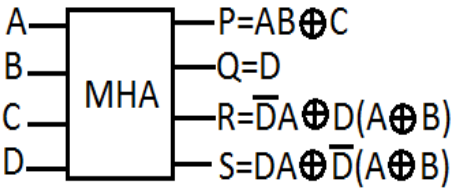

Fig. 7 MHA gate

B. MFA gate

Similarly MFA gate is a 5 x 5 reversible gate which is represented in Fig .8. The inputs are I(A,B,C,D,E) and their corresponding outputs are O(P,Q,R,S,T). If D=0 it works as a full adder. Input E functions as the select line. Carry is generated at P and Sum at R.

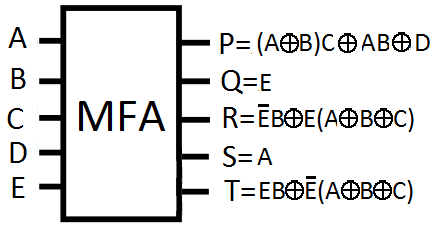

Fig.8 MFA gate

MHA and MFA gates are used in carry save adder stages of the column bypass multiplier. The internal architecture of the proposed gates is as depicted in Fig. 9 and Fig. 10 respectively.

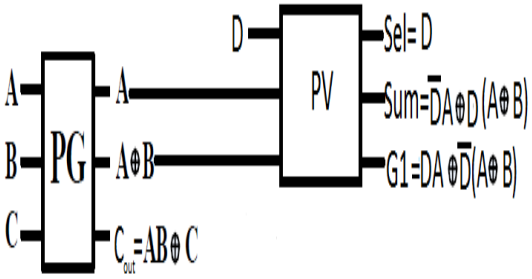

Fig. 9 Internal architecture of MHA gate

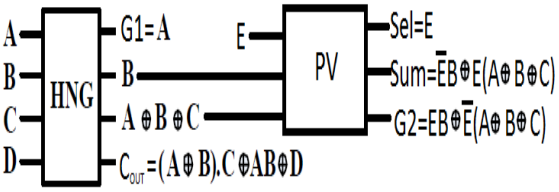

Fig. 10 Internal architecture of MFA gate

The multiplexer is realized using a PV gate which chooses the sum term when the select input is 1 and the partial product if the select input is 0. The carry out is passed unaltered.

V. PROPOSED 4 X 4 MULTIPLIER

Consider two unsigned n-bit numbers where $X=X_{n-1},X_{n-2}\ldots X_0$ is the multiplicand and $Y=Y_{n-1},Y_{n-2},\ldots,Y_0$ is the multiplier.
The product of these two bits can be written as

$$P = \sum_{i=0}^{n-1} X_i \sum_{j=0}^{n-1} Y_j \, 2^{i+j}$$

x_3 x_2 x_1 x_0 y_3 y_2 y_1 y_0

x_3y_0 x_2y_0 x_1y_0 x_0y_0

x_3y_1 x_2y_1 x_1y_1 x_0y_1

x_3y_2 x_2y_2 x_1y_2 x_0y_2

x_3y_3 x_2y_3 x_1y_3 x_0y_3

P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0

Fig. 11 Partial products in 4 x 4 multiplications

Proposed reversible multiplier circuit is divided into two parts.

A. First part: Partial Product Generation Circuit

The partial product generation circuit is depicted in fig 12.The partial products are generated using a combination of Taffoli gate (TG) and Peres gate (PG). First three rows consist of 12 TG and the last row comprises of 4 PG. Here the propagated multiplicand bits x0 – x2 which are considered to be garbage at the last stage are fed to the select lines of the multiplexers in the first row of the summation circuit. Thus at this stage, 3 garbage outputs are reduced. Therefore this stage produces only 5 garbage outputs.

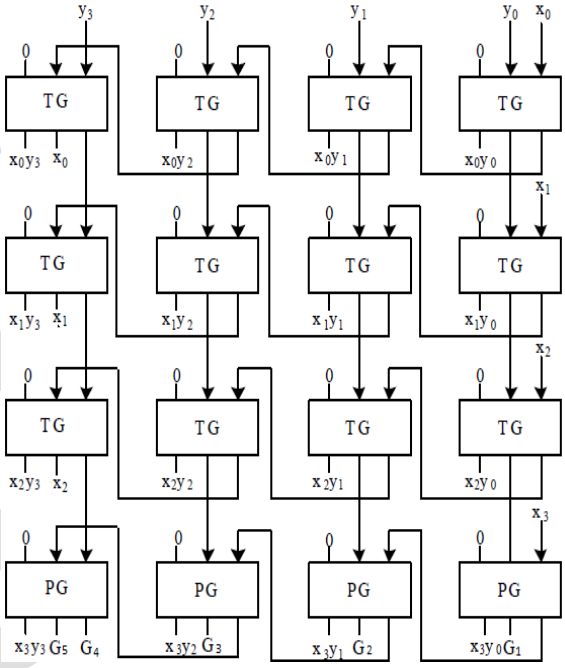

Fig.12 Partial products generation circuit

B. Second part: Summation Circuit

In the proposed summation circuit shown in Fig. 13, the first stage is implemented using MHA gate because the value of the carry inputs are considered to be '0' in the first stage. The carry outputs of each adder circuit are diagonally forwarded to the next stage of adder circuits. Thus MFA gate is used for further stages. This results in carry save technique where the carry bits are not immediately added but saved for the next stage. Also if the bit x_i in the multiplicand is '0', then the corresponding diagonal cells are all '0'. Consequently the appropriate diagonal cells are disabled by the multiplexer and the sum output of the above cell is let to bypass this unimportant diagonal. In the final stage, carries and sums are merged using a ripple carry adder circuit which is formed by a combination of PG and HNG gate.

VI. RESULTS

The reversible column bypass multiplier is synthesized and simulated to test its functionality using XILINX in conjunction with MODELSIM. The simulation results for the 4x4 reversible column bypass multiplier is shown in Fig. 13. Table 1 shows the comparison of column bypass multiplier with the multiplier in [12].It is evident from the table that the proposed reversible column bypass multiplier is better in terms of garbage outputs, constant inputs and total number of gates.

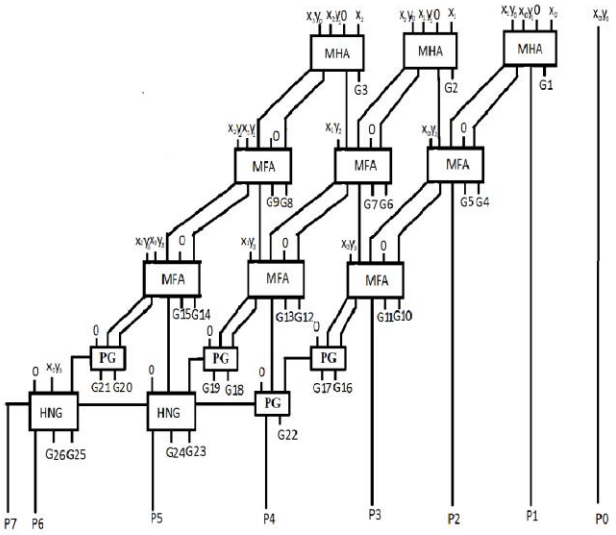

Fig.13 Proposed reversible summation network

TABLE I
COMPARISON OF PERFORMANCE PARAMETERS

Multiplier	No. of gates	Garbage outputs	Constant inputs
Reversible Multiplier[13]	40	80	31
Proposed design	31	31	31

VII. CONCLUSION

This study presents an optimized reversible multiplier circuit using column bypass technique. It eliminates the extra correction circuits needed and has a simpler modified full adder as compared to the row bypass multiplier. This design helps in reducing the switching activity when the binary input has zeros in it. Thus the delay in this multiplier gets reduced. Power reduction is accomplished using reversible logic gates. This paper presents two new gates namely MHA and MFA using which the garbage outputs and constant inputs are greatly reduced.

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