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# Development of High-Level Asymmetric Multilevel Inverter with Reduced Number of Switches for Fuel Cells

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## ABSTRACT

Multilevel inverters have been an attractive topology for academia as well as industry in the recent decade for high power and medium voltage energy control. An asymmetric multilevel inverter, a new topology increases the level of output with reduced lower order harmonics and total harmonic distortion. In this topology, the output voltage and power increases with the number of level and increasing output voltage does not require an increase in voltage rating of individual commutated devices. In this paper, a fifteen-level asymmetric MLI with three DC sources and seven switches have been proposed which will be suited for fuel cell applications. For the proposed MLI, a new hybrid modulation technique combining the PWM and fundamental frequency switching technique is developed. The inverter structure is studied and simulated in MATLAB/SIMULINK for investigating the spectral quality of the output. Total Harmonic Distortion (THD) is analyzed for the various PWM techniques and the results are verified through simulation results.

**Keywords:** Asymmetric Multilevel inverter, Total Harmonic Distortion, Sinusoidal Pulse Width Modulation, Fundamental frequency Pulse Width Modulation.

## 1. INTRODUCTION

Multilevel inverters have the advantages like reduced EMI/RFI generation, minimum total harmonic distortion and can operate on several voltage levels compared with the conventional two-level inverter. Harmonics are reduced due to multi-switching and output is approximately a sine wave so the filter design and cost are reduced. The requirements of AC loads are fulfilled by controlling the output voltage of the inverters when such loads are fed by inverters. The MLI is used for high power ratings and for renewable energy sources such as fuel cell, wind and photovoltaic that can be interfaced easily for a high power application. The multilevel inverter can operate at both fundamental switching frequency and high switching frequency PWM. Multilevel inverter has two major classifications: Symmetric Multilevel Inverter and Asymmetric Multilevel Inverter (AMLI). AMLI is more advantageous than the symmetric one, because it produces more number of levels with same number of switches by having unequal voltage

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sources. As a result, the installation space and total cost of an asymmetric cascaded multilevel inverter is lower. This paper focuses on the development of asymmetric multilevel inverter with least number of switches which produces fifteen output voltage levels. The performance parameters of this multilevel inverter such as THD for different modulation indices will be computed. Finally, the feasibility of the proposed inverter will be verified through simulation results.

## 2. ASYMMETRIC MULTILEVEL INVERTER

### 2.1 Circuit configuration and its operation

Cascaded multilevel inverter is one of the best topologies when compared with diode clamped and flying capacitors because it requires least number of components. From this basic asymmetric cascaded topology, fifteen level inverter requires three H-bridges, three DC sources of unequal voltages. Fig:1 shows that conventional asymmetric multilevel inverter which has three different voltage sources and twelve switches to produce fifteen level. In general, 'n' switches are required to produce 2n+1 level. The proposed asymmetric multilevel inverter consists of seven switches and voltage sources of $V_1 = V_{dc}, V_2 = V_{dc}/2$, $V_3 = V_{dc}/4$ ($V_1$=6V,$V_2$=12V,$V_3$=24V) which is

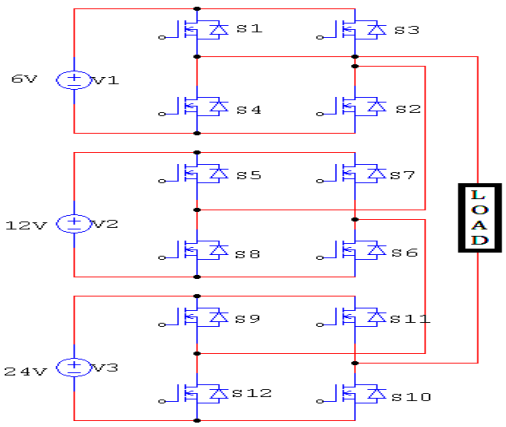


Fig1: Conventional AMLI

shown in Fig.2. The overall output voltage for fifteen level inverter is $V(t) = V_1+V_2+V_3$ which is based on opening and closing of switches $S_1$,$S_2$ and $S_3$. The asymmetric basic unit has three voltage sources, three switches and three diodes alongwith a full bridge inverter configuration. The conduction state of the Switches are given based on they have to withstand both positive and negative voltages and zero voltage. The proposed inverter can generate positive, negative and zero voltage levels. The output voltage is zero when all switches are turned OFF or conduction of all switches in lower leg or upper

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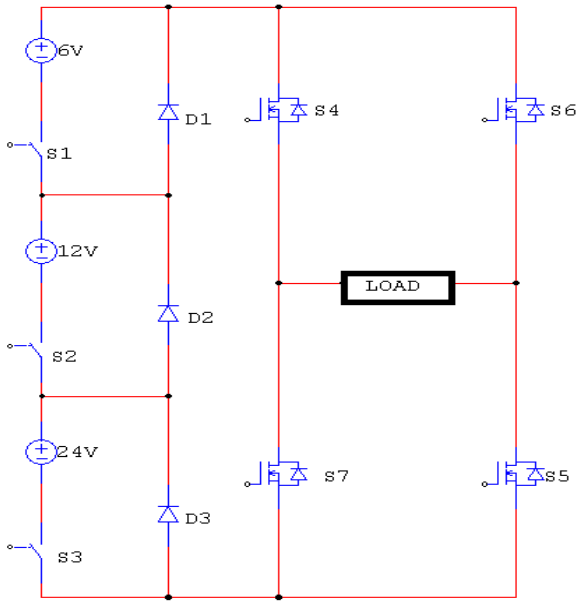


Figure 2 Proposed AMLI

Table 1: Conduction state of AMLI

| SWITCHES | | | | | | | OUTPUT VOLTAGE |
|---|---|---|---|---|---|---|---|
| S1 | S2 | S3 | S4 | S5 | S6 | S7 | V0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 6 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 18 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 24 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 30 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 36 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 42 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | -6 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | -12 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | -18 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | -24 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | -30 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | -36 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | -42 |

leg in H-bridge unit. The other voltage levels are obtained by proper switching between the switches. In this table 1, means that corresponding switch is turned on to get the corresponding voltage and zero indicates OFF

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state. For generating output voltage levels, two switches must be turned ON in full bridge inverter unit, one from upper switches and other from lower switches. To get positive voltage, $S_4$ and $S_5$ switches are in ON state and to get negative voltage, $S_6$ and $S_7$ switches are in conduction state. The difference between values of sources improves performance of multilevel inverter and enhances the number of levels. The design of pulse generation circuit makes the topology differs from other so as to obtain the unique pulse pattern to trigger the switches at the proper instant. To eliminate the switches get distorted, all the switches in this topology is unidirectional. In this topology, reduced switches are used to develop fifteen levels and it makes the circuit user friendly and switches reduction benefits in low switching losses. The maximum output voltage, number of power electronic devices, and number of levels for proposed asymmetric multilevel inverter are formulated as

$$V_{omax} = (2^{n-1}) * V_1 \quad (1)$$

$$N_{IGBT} = n+4 \quad (2)$$

$$N_{Level} = 2^{(n+1)} - 1 \quad (3)$$

where n represents the number of voltage sources used in asymmetric multilevel inverter.

## 3. MODULATION STRATEGIES FOR ASYMMETRIC MULTILEVEL INVERTER

### 3.1 Hybrid modulation technique

A newly developed new modulation technique is used to generate a stepped switched waveform with high power quality and minimum harmonic content. Hybrid modulation used in the paper is the combination of the fundamental frequency modulation (FPWM) and sinusoidal PWM. The output is obtained with reduction in switching loss from FPWM and good harmonic reduction from SPWM. The output voltage of the proposed asymmetric multilevel inverter can be controlled using modulation index and multicarrier based PWM technique. For fifteen level asymmetric multilevel inverter, fundamental frequency modulation is used for four switches and SPWM is used for three switches.

### 3.2 FPWM technique for H-bridge switches

The key issue of the fundamental frequency modulation control is to eliminate harmonics of particular frequency by choosing the switching angles for the pulse generation of the switches in the full bridge inverter unit. In fig:2, the gating pattern for four switches in full bridge inverter unit is given by fundamental frequency modulation to reduce switching losses.

### 3.3 SPWM technique for asymmetric basic unit switches

Multicarrier based PWM strategies are easy to implement and very popular. It uses several triangle carrier signals, one carrier for each level and one reference, or modulation signal per phase. In the proposed inverter as shown in Fig.2, asymmetric unit is operated under SPWM which has three switches with three different voltage sources. SPWM is implemented using the four basic techniques and the best technique is selected based on the reduction in harmonic content.

#### 3.3.1 Phase disposition PWM

For this technique, carriers which are in inphase accordingly are required. For fifteen level inverter, four carriers of equal amplitude and equal frequency are required to employ the less harmonic content output voltage waveform. It is based on the comparison between the vertically shifted triangular carrier signal and sinusoidal reference signal as shown in the figure 3. In the PD PWM, the harmonics are

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cancelled in the line voltage due to the symmetry. This cancellation is independent of the absolute carrier frequency and carrier to fundamental frequency ratios does affect the harmonic performance of the modulation algorithm. Thus, PD-PWM modulation technique gives the excellent line voltage performance with reduced harmonic contents.The amplitude modulation index $m_a$ and frequency modulation index $m_f$ are

$$m_f=f_c/f_r \quad (4)$$

$$m_a=2A_r/(m*A_c) \quad (5)$$

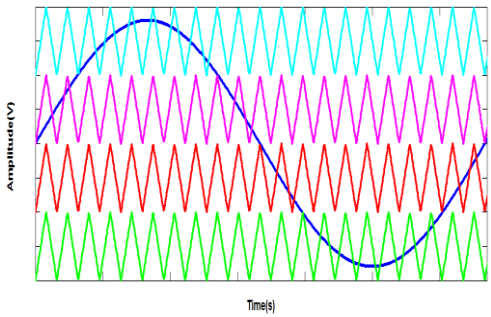


Fig 3: Carrier and reference signal for PDPWM.

### 3.3.2 Phase opposition and disposition PWM

In POD-PWM control technique, the carrier signals which are above the zero level are in phase and the carrier signals which are below the zero level are out of phase by $180^0$. In POD, the output phase voltage has quarter-wave symmetry and odd symmetry respectively, if $m_f$ is even and odd. Similar to APOD-PWM, POD modulation contains significant harmonics in the line voltage spectrum, especially in the first carrier band. Comparing to APOD, this modulation has less harmonic distribution along the harmonic orders.The amplitude modulation index $m_a$ and frequency modulation index $m_f$ for this technique are

$$m_f=f_c/f_r \quad (6)$$

$$m_a=2A_r/(m*A_c) \quad (7)$$

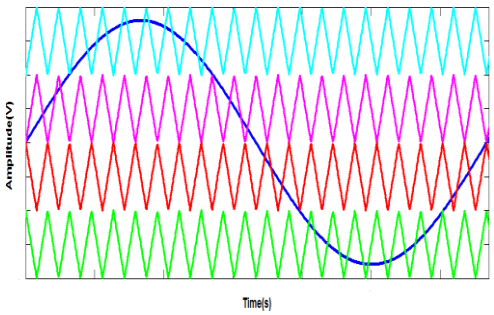


Fig 4: Carrier and reference signal for PODPWM

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### 3.3.3 Alternate phase opposition and disposition PWM

This technique requires carriers which are displaced from each other by $180^0$ alternatively. In particular, it can be seen that APOD modulation does not produce a first carrier harmonic. Instead the dominant harmonics are channeled into the sidebands around the first carrier harmonic. But APOD modulation contains some considerable harmonic energy in the line voltage spectrum. In addition, output voltage has quarter wave symmetry, if $m_f$ is even. If $m_f$ is odd, then the output waveform has odd symmetry. The amplitude modulation index $m_a$ and frequency modulation index $m_f$ are

$$m_f=f_c/f_r \quad (8)$$

$$m_a=2A_r/(m*A_c) \quad (9)$$

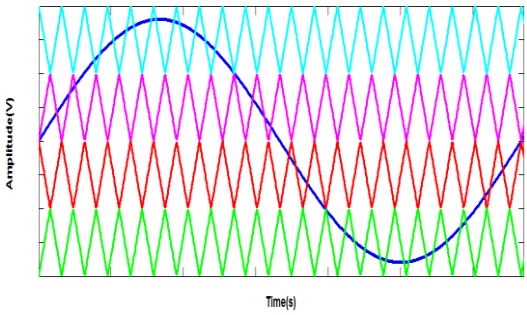


Fig 5: Carrier and reference signal for APODPWM

### 3.3.4 Phase shift PWM

A carrier phase shift for cascaded inverter is introduced to generate the stepped multilevel output waveform with lower distortion. This technique distributes the switching angles uniformly but it is more difficult to implement. The amplitude modulation index $m_a$ and frequency modulation index $m_f$ are

$$m_f=f_c/f_r \quad (10)$$

$$m_a=2A_r/(A_c) \quad (11)$$

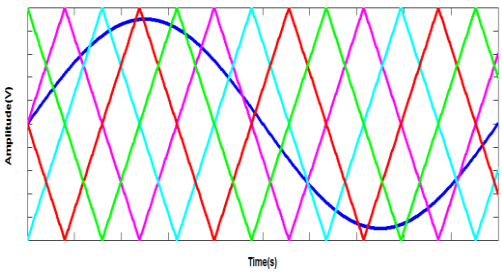


Fig 6: Carrier and reference signal for PSPWM.

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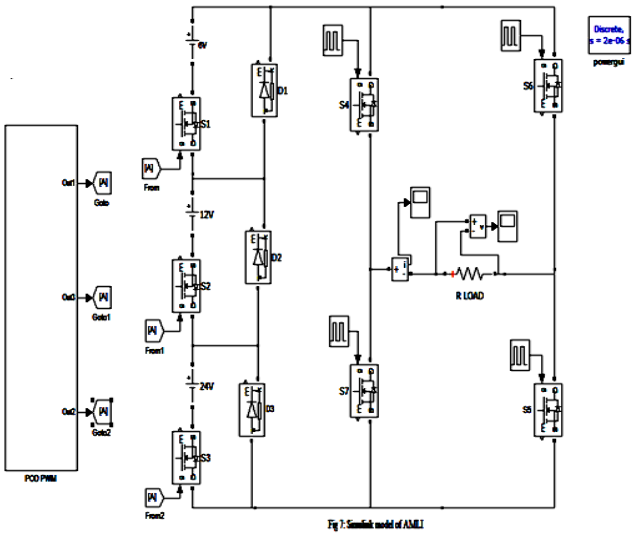


Fig 7:Simulink model of AMLI AMLI

## 4. STUDY CASE IMPLEMENTATION IN MALTAB

Simulation studies of the proposed Asymmetric Multilevel inverter with hybrid PWM strategies are performed by using MATLAB-SIMULINK The simulation of asymmetric multilevel inverter is carried out using MATLAB-SIMULINK. It is shown in the fig: 7. The simulation parameters are

Table 2: Simulation parameters

| | |
|---|---|
| DC source, $V_1$ | 6V |
| DC source, $V_2$ | 12V |
| DC source, $V_3$ | 24V |
| Fundamental frequency, $f_c$ | 3150Hz |
| Load resistance, R | 10 ohm |
| Switching frequency, $f_s$ | 50Hz |

The gating pattern for the seven switches is given by hybrid modulation technique employing POD technique. The pulse for three switches from asymmetric basic unit is given by SPWM and is shown in fig:8. The pattern for remaining four switches from full bridge inverter is given by FPWM and is shown in fig:9.

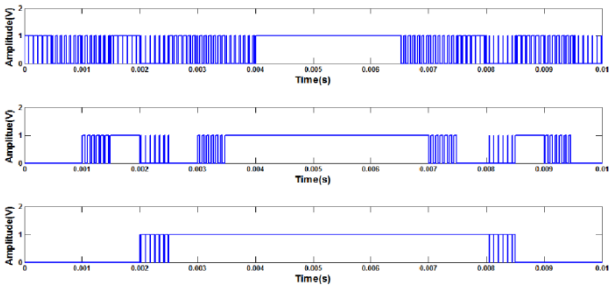


Fig 8: Gating pulses by SPWM using POD for S1,S2,S3 switches.

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Fig:10 shows the output voltage waveform for fifteen level asymmetric multilevel inverter with R-load employing POD modulation technique. The FFT analysis is used for comparing various modulation techniques based on THD values and the result is PODPWM which is the best one with minimum harmonic distortion. The FFT analysis for voltage waveform with PODPWM is shown in the fig:11.

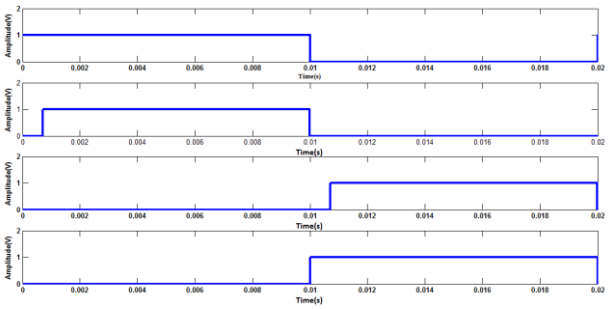

Fig 9: Gating pulses by FPWM for S4,S5,S6,S7 switches.

The output volatge of asymmetric multilevel inverter is compared for PD,POD,APOD,PS by using FFT analysis which is shown in the table 3.

Table 3: THD Comparison

| S.No | PWM Technique | THD% |
|---|---|---|
| 1 | Phase Disposition | 13.21% |
| 2 | Phase Opposition and Disposition | 13.13% |
| 3 | Alternate Phase Opposition and Disposition | 13.19% |
| 4 | Phase Shift | 13.25% |

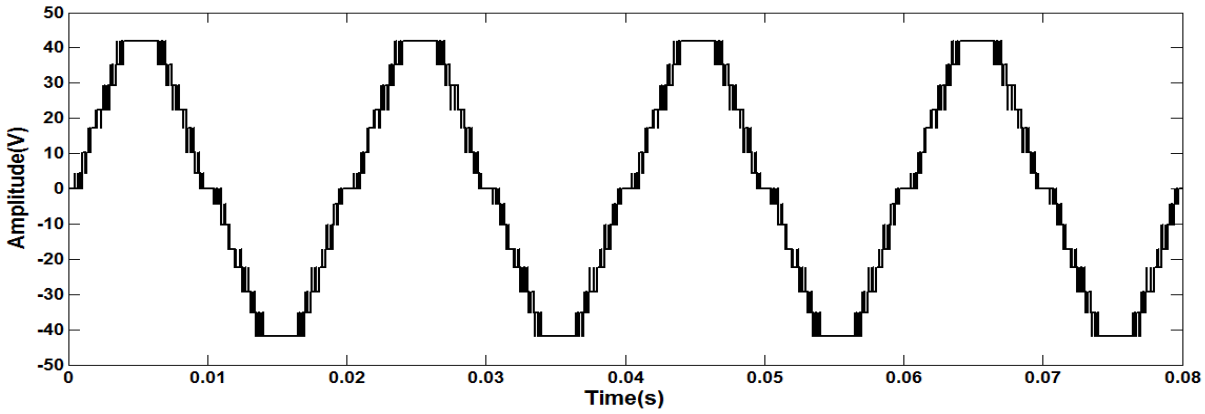


Fig 10: Simulation output for PWM based AMLI with PODPWM

The THD results are used for comparison of various modulation strategies to find out the best one. The comparison of THD is provided in table 3. Figure 11 shows the THD results for Phase Opposition and Disposition From the table, POD PWM is the best one

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which has minimum harmonic content when compared with others and also it has the minimum third order harmonic contents than other PWM technique..

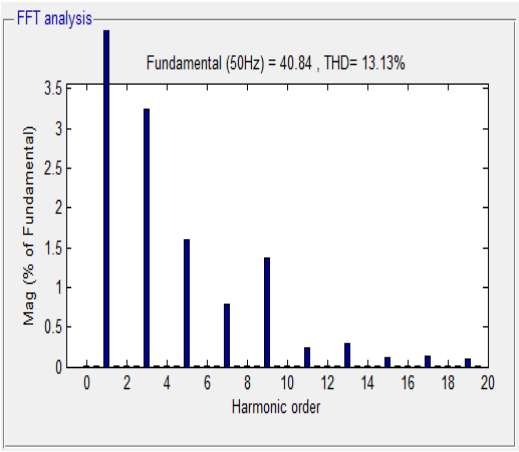


Fig 11: FFT analysis for PODPWM.

## 5. CONCLUSION

In this paper, hybrid modulation technique for fifteen level asymmetric multilevel inverter with hybrid PWM technique is proposed. It also presents the comparison of the proposed asymmetric multilevel inverter with conventional multilevel inverter. By implementing various hybrid PWM techniques, it is found that the POD is the best technique that has less THD and can be easily extended to higher number of levels and number of phases. Therefore, the proposed AMLI is well suited for fuel cell applications.

## 6. ACKNOWLEDEMENT

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## 7. REFERENCES:

[1] Rasoul Shalchi Alishah, Daryoosh Nazarpour, Seyyed Hossein Hosseini, Mehran Sabahi,2013:'New Hybrid Structure for Multilevel inverter with fewer number of components for high voltage level' IET power electronics., Vol. 7, Issue. 1, pp. 96–104.

[2] A.Reddiprasanna1, P. Chandrasekhar2, G. Jayakrishna,2013:' A novel seven level multilevel inverter with photovoltaic cell' International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering., Vol. 2, Issue 10.

[3] Bharath.K, R.J.Satputaley,2013:' Single phase Asymmetrical cascaded multilevel inverter design for induction motor' ASAR International Conference, Bangalore Chapter, ISBN: 978-81-927147-07.

[4] E.Babaei, S. Alilu, and S. Laali 2014, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Trans. Ind. Electron., vol. *61*,no. 8, pp. 3932-3939.

[5] Gupta, K.K., Jain, S,2012.: 'A multilevel voltage source inverter (VSI) to maximize the number of levels in output waveform', Elsevier J. Electr. Power Energy Sys., 1, (44), pp. 25–36.

[6] B harath. K,R J. Satputaley,2013.:' Single phase asymmetrical cascaded multilevel inverter design for Induction motor', ASAR International Conference, Bangalore Chapter- 2013, ISBN: 978-81-927147-0-7.

[7] Mariusz Malinowski, K. Gopakumar, Jose Rodriguez, and Marcelo A.2010"A Survey on Cascaded Multilevel Inverters", IEEE Trans on Industrial Electronics, Vol. 57,NO. 7, JULY 2010 2197.

GLOBAL JOURNAL OF ADVANCED RESEARCH
(Scholarly Peer Review Publishing System)

[8] Ebrahim Babaei Sara Laali, and Zahra Bayat, 2014' A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches' IEEE transaction on industrial electronics, Vol 60.

[9] E.Sambath,S.P.Natarajan,C.R.Balamurugan, 2012,' Performance evaluation of multi carrier based pwm techniques for single phase five level h-bridge type FCMLI'iosr journal of engineering issn: 2250-3021 volume 2, issue 7, pp 82-90

[10] J.H. Kim, S.K. Sul, and P.N. Enjeti,2008, "A carrier-based PWM method with optimum switching sequence for a multilevel four-leg voltage source inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239-1248.

[11] L. Haiwen, L.M. Tolbert, S. Khomfoi, B.Ozpineci and D. Zhong,2008 , Hybrid Cascaded Multilevel Inverter with PWM Control Method, Proc. Power Electronics Specialists Conference, pp.1- 5.

[12] R.Nagarajan, M. Saravanan,2013,' Staircase Multicarrier SPWM Technique for Nine Level Cascaded Inverter', International Conference on Power, Energy and Control

[13] Jih-sheng Lai and Fang Zheng Peng 1996, "Multilevel Converters-A new Breed Of Power Converters" presented at IEEE May/June 1996.

[14] L. M. Tolbert, J. N. Chiasson, Z. Du and K. J. McKenzie,2005, Elimination of Harmonics in a Multilevel Converter with Nonequal DC Sources, IEEE Transactions on Industry Applications, Vol. 41, No. 1, pp. 75-81.