RESEARCH ARTICLE OPEN ACCESS

Dynamic Power reduction of synchronous digital design by using of efficient clock gating technique

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Abstract:

Clock gating is an effective method of reducing the dynamic power consumption in synchronous circuits. One of the ways to achieve this is by masking the clock that goes to the idle portion of the circuit. In This paper we will present a comparative analysis of existing clock gating techniques on some synchronous digital design like ALU (Arithmetic logical unit) etc. Also a new clock gating technique that provides more immunity to the existing problem in available technique. In new proposed clock gating the Gated Clock Generation Circuit is using tri state buffer and Gated logic is used which is created by the combination of double gated (AND, OR, AND logic gate) with bubbled input respectively. This circuit saves power even when Target device's clock is ON. All experiments are done on Xilinx14.1 EDA tool. Mentor Graphics Model SIM. For power calculation we are using XPOWER. Sparten-3 (90nm) FPGA platform is used for result and analysis. The proposed design will reduce the hardware complexity with approximately 10-20%. Similar clock power complexity will reduce with 5-10%.

Keywords — ***Tri state buffer; VLSI; Xilinx; glitches; hazards;Sparten.***

I. INTRODUCTION

The introduction of integrated circuits (ICs), commonly referred to as microchips or simply chips, was accompanied by the need to test these devices. Small-scale integration (SSI) devices, with tens of transistors in the early 1960s, and medium scale integration (MSI) devices, with hundreds of transistors in the late 1960s, were relatively simple to test. However, in the 1970s, large-scale integration (LSI) devices, with thousands and tens of thousands of transistors, created a number of challenges when testing these devices. In the early 1980s, very-large-scale integration (VLSI) devices with hundreds of thousands of transistors were introduced. Steady advances in VLSI technology have resulted in devices with hundreds of millions of transistors.

One of the major dynamic power reduced by clock gating method in computing and consumer electronics products in the overall system's clock signal then reduce the 30%–70% of the total dynamic power consumption and then reduce the overall circuit power to reduce15- 20% of Grouping Flip Flop data driven clock gating method [1].Clock gating is major method of reducing clock signal. Generally, when a logic unit is clocked, it is based on the sequential elements receiving the clock signal, sequentially they will toggle in the next cycle whether it is required or not. The data driven clock gating circuit using clock enabling signals are manually added for every FF as a part of a design methodology [1]. With clock gating, the clock signals are ANDed with explicitly predefined enabling signals. Clock gating is employed at all levels of system architecture, block design, logic design, and gates. Several methods to take advantage of this technique are described, with all of them depending on various heuristics in an attempt to increase clock gating opportunities. With the rapid increase in design complexity, computer aided design tools supporting system-level hardware description have become commonly used. Although substantially increasing design productivity, such tools require the employment of

a long chain of automatic synthesis algorithms, from register transfer level (RTL) down to gate level and net list . Unfortunately, such automation leads to a large number of unnecessary clock toggling, thus increasing the number of wasted clock pulses at flip-flops (FFs) as shown in this paper through several industrial examples.

A. Dynamic power

The power dissipated when circuit is switching from one state to another or ON state. The switching power of a single gate can be expressed as

$$P_{Dynamic} = C_L V_{DD}^2 f$$

Where f is the clock frequency, C_L is the switching capacitance, V_{DD} is the supply voltage. Reducing the dynamic power dissipation is obtained by the methods of reducing any of the variables in this equation. [5]

B. Dynamic power reduction technique

Though the leakage power increases significantly in every generation with technology scaling, the dynamic power still continues to dominate the total power dissipation of the general purpose microprocessors. Effective circuit techniques to reduce the dynamic power consumption include transistor size and interconnect optimization, gated clock, multiple supply voltages and dynamic control of supply voltage. Incorporating the above approaches in the design of nano-scale circuits, the dynamic power dissipation can be reduced significantly.[4]

C. Clock gating

Clock gating is an effective way of reducing the dynamic power dissipation in digital circuits. In a typical synchronous circuit such as the general purpose microprocessor, only a portion of the circuit is active at any given time. Hence, by shutting down the idle portion of the circuit, the unnecessary power consumption can be prevented. One of the ways to achieve this is by masking the clock that goes to the idle portion of the circuit. This prevents unnecessary switching of the inputs to the idle circuit block, reducing the dynamic power.[19]

II. PROBLEMS IN PREVIOUS TECHNIQUES

- In AND gate clock gating we have output correctness problem due to glitches and hazards.
- In NOR gate clock gating we have output correctness problem due to glitches and hazards.
- In Latch based AND gate clock gating hazards problem is removed but glitches problem still exists.
- In Latch based NOR gate clock gating hazards problem is removed but glitches problem still exists.
- In MUX based clock gating requires an expensive MUX per bit and consumes more power and hardware.
- In FF based clock gating the sleep period is longer so there is a greater chance to change that happens on Enable signal.
- In Positive level sensitive Latch based clock gating more hardware is required.
- In T flip flop based clock gating the gate count is maximum compare to other.
- In Double gated flip flop based clock gating the gate count is more and also more power consumption.
- In Gated clock using negative latch based clock gating we have large hardware problem.

In previous all clock gating approaches are facing with the problem of size means those approach which are require less size there is some other issue of glitches and those approaches which having large size so there is no any glitches problem but those structure are increase static problem.[19]

In all previous approach only few approaches will reduce the clock power but still some are facing the problem of clock power.[19]

In some previous architecture there is need of extra input and output pins as we know for VLSI

chip increase in input and output pins will increase the cost of the whole process.

III. PROPOSED APPROACH

Here we will discuss a new design that will save more power and area. The new Gated Clock Generation Circuit is shown in below figure using tri state buffer and Gated logic is used which is created by the combination of double gated (AND, OR, AND logic gate) with bubbled input respectively. This circuit saves power in such a way that even when Target device's clock is ON, the controlling device's clock is OFF and also when the target device's clock is OFF then also Controlling device's clock is OFF. This way we can save more power by avoiding unnecessary switching at clock net . This clock gating design is on at posedge and off at negedge means clock power and dynamic power is save at the time of negedge clock. To understand the working of circuit , an input signal named Clk is provided to the And , And, OR and tri-state buffer.

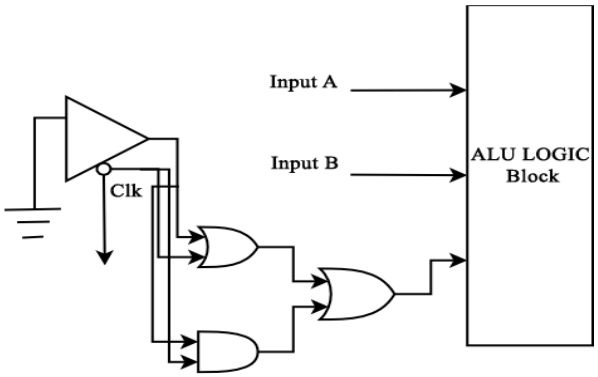


Figure 1. Proposed Clock gating Logic

IV. IMPLEMENTATION DETAIL

We have implemented different type of clock gating techniques and proposed technique to reduce power. All the techniques are performed at different technology with temperature, voltage and frequency variation and their Dynamic, static and total power has been computed, In this we are applying clock gating techniques on a 8bit Arithmetic logical unit (ALU). The results are in tables shown below. All experiments are done on Xilinx14.1 EDA tool. Mentor Graphics Model SIM. For power calculation we are using XPOWER. Sparten-3 (90nm) FPGA platform is used for result and analysis.

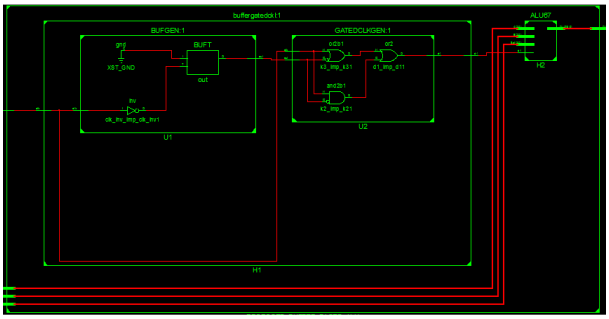
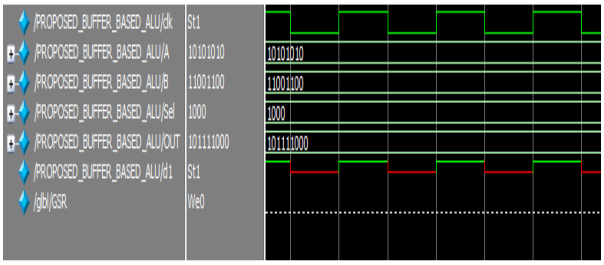


Figure 2. Schematic of Proposed Clock Gating



When clk turns to '1' at that time En output is '0' , and double gated (AND, OR and AND gate) with posedge clock will produce output ='1' which goes to the first clock generation logic that generates clock for controlling device. In first logic we have an TRI gate which have Global Clock as an input at the other input of ground. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '1'.In the next clock pulse, when CLK turns to '0' clk at its input and when Gen goes '1' it generates clock pulse that goes to the target device. This design only requires 4 logic gates it will save dynamic and clock power. This design will make a justice with spa metrics and also there is no any glitches problem in our design.

TABLE I. COMPARISON OF POWER FOR PROPOSED TRISTATE BUFFER CLOCK GATING TECHNIQUE WITH VOLTAGE VARIATION

Voltage	90nm Technology		
	Dynamic	Static	Total
1.14	0.083	0.027	0.11
1.2	0.087	0.028	0.114
1.26	0.119	0.029	0.119

TABLE II. COMPARISON OF FREQUENCY FOR PROPOSED TRISTATE BUFFER CLOCK GATING TECHNIQUE WITH VOLTAGE VARIATION

Frequency	90nm Technology		
	Dynamic	Static	Total
10G Hz	1.272	0.034	1.306
7G Hz	0.901	0.031	0.932
5G Hz	0.642	0.030	0.673

TABLE III. COMPARISON OF TEMPERATURE FOR PROPOSED TRISTATE BUFFER CLOCK GATING TECHNIQUE WITH VOLTAGE VARIATION

Temperature	90nm Technology		
	Dynamic	Static	Total
25	0.201	0.276	0.477
50	0.201	0.369	0.570
75	0.201	0.508	0.709

Table I, II and III represents the comparison of dynamic, static and total power with various voltages (1.14,1.2and1.26), various frequencies (10, 7 and 5Hz) and various temperatures (25,50and 75degree)

TABLE IV. COMPARISON OF DYNAMIC POWER FOR VARIOUS CLOCK GATING TECHNIQUES AT 90NM TECHNOLOGIES OPERATING AT 1.14 VOLTAGE

Clock Gating Technique	90 nm Technology
Without clock gating	0.220
AND gate based	0.137
Latch based	0.115
MUX based	0.146
Flip flop based	0.137
Positive level sensitive latch based	0.136
T-FF based	0.149
Double gated based	0.203
Negative latch based	0.125
Proposed	0.083

In table IV the comparison of Dynamic power at 1.14 voltage for various clock gating is shown at 90 nm technology which shows that the proposed clock gating consumes less Dynamic power as compare to other different types of clock gating that means the proposed clock gating is better as compared to other previous techniques.

TABLE V. COMPARISON OF DYNAMIC POWER FOR VARIOUS CLOCK GATING TECHNIQUES AT DIFFERENT TECHNOLOGIES OPERATING AT 10GHZ FREQUENCY

Clock Gating Technique	90 nm
Without clock gating	2.215
AND gate based	1.378
Latch based	1.375
MUX based	1.365
Flip flop based	1.375
Positive level sensitive latch based	1.392
T-FF based	1.512
Double gated based	1.387
Negative latch based	1.25
Proposed	1.272

In table V the comparison of Dynamic power at 10 GHz frequency for various clock gating techniques is shown at 90 nm technology which shows that the proposed clock gating consumes less Dynamic power at that particular frequency as compare to other different types of clock gating techniques that means the proposed clock gating is better as compared to other previous techniques.

TABLE VI. COMPARISON OF DYNAMIC POWER FOR VARIOUS CLOCK GATING TECHNIQUES AT DIFFERENT TECHNOLOGIES OPERATING AT 25 DEGREE TEMPERATURE

Clock Gating Technique	90 nm technology

Without clock gating	0.223
AND gate based	0.14
Latch based	0.158
MUX based	0.149
Flip flop based	0.204
Positive level sensitive latch based	0.141
T-FF based	0.153
Double gated based	0.141
Negative latch based	0.141
Proposed	0.201

In table VI the comparison of Dynamic power at 25 degree temperature for various clock gating is shown at 90 nm technology which shows that the proposed clock gating consumes less Dynamic power at that particular temperature as compare to other different types of clock gating techniques that means the proposed clock gating is better as compared to other previous techniques.

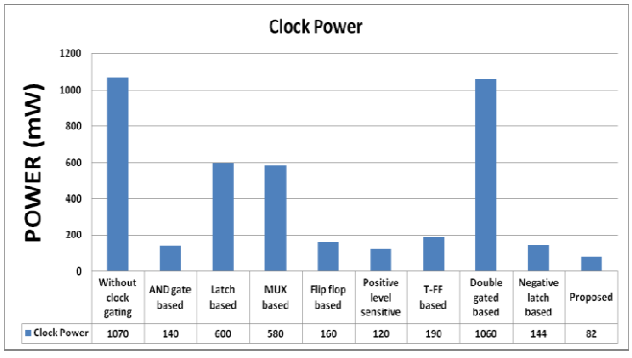


Figure 3 Comparison of clock power for various clock gating

We know that the previous clock gating techniques the techniques which reduces the more dynamic power consumption will have large hardware requirement and techniques which requires small hardware will consumes more dynamic power. From figure 8 it is clear that the proposed clock gating consumes less dynamic power (only 82mW) as compare to other techniques.

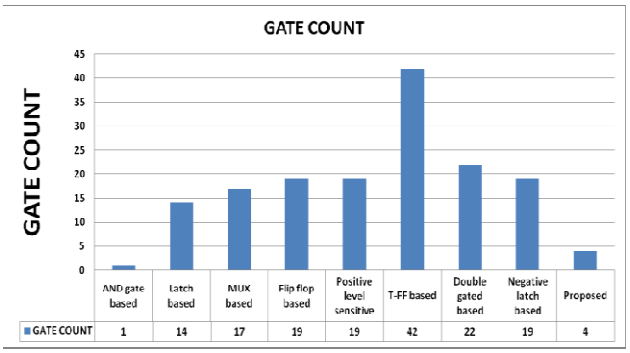


Figure 4 Gate count comparison of Proposed and existing approaches.

as well as it requires very less hardware (only 4 logic gates) that means the proposed clock gating approach is very good technique because it consumes less dynamic power also requires less hardware.

V. CONCLUSIONS

We conclude the dissertation with a brief summary of contributions.

Contributions:

The key contribution of this paper is to develop a new clock gating technique with low area overhead and improved performance of the digital circuit. The increase in dynamic power consumption makes the system unreliable, so to control the dynamic switching power various techniques are studied and analyzed to reduce it. A New double gated tri state based clock gating technique is proposed with low area overhead. Comparative analysis shows that the proposed technique impacts on the dynamic power reducing up to 2-3 folds in compare to conventional one. The proposed design will reduce the hardware complexity with approximately 10-20%. Similar clock power complexity will reduce with 5-10%. All the analysis is done on a 8 bit ALU with process variation parameters.

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