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Controller Tuning for Disturbance Rejection Associated with a Delayed Double Integrating Process, Part I: PD-PI Controller

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Abstract:

This paper investigates using a PD-PI controller for disturbance rejection associated with delayed double integrating processes. The control is tuned using the MATLAB optimization toolbox and five different error-based objective functions for process time delay between 0.2 and 1 s. The more suitable objective function for disturbance rejection with PD-PI controller used with the delayed double integrating process is assigned and the effect of the process time delay on the performance of the control system in the time domain is shown. The unit step disturbance input time response of the control system has a maximum value less than 3.62, time of maximum time response less than 1.71 s and a settling time less than 26 s. The simulation results using the PD-PI controller are superior when compared with other disturbance rejection technique based on using a PID controller.

Keywords — **Disturbance rejection, delayed double integrating process, PD-PI controller, controller tuning.**

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I. INTRODUCTION

Disturbance rejection is a performance requirement associated with feedback control systems. This performance depends on the type of process to be controlled and the type of controller or compensator used. This area finds rich interest from automatic control researchers and scientists.

Otsuka (2000) investigated the solvability conditions of the disturbance rejection problem with dynamic compensator. He did not assume that the order of the compensator equals that of the plant [1]. Lin and Hsiao (2001) presented an approach to treat the disturbance rejection problem for missile seeker. They proposed a multi-layer feedforward neural network to realize a nonlinear adaptive feedforward controller. They showed that with a neural controller there were possibilities for improving the miss distance performance of the rocket [2]. De Paor (2002) developed two stage procedure for stabilization and disturbance rejection for the control of integrating and unstable processes with time delay. They handled a number of illustrative examples showing the frequency response, unit step response and unit disturbance response [3].

Liu, Yan, Zhou and Cai (2003) presented an scheme for an auto-disturbance rejection control for hybrid power compensators. They employed a nonlinear state-error-feedback to realize the tracing of reference input. Test results proved the effectiveness of their control approach [4]. Leonardi and Da Cruz (2004) discussed the robust design of compensators aiming at disturbance rejection with time domain specifications. They assumed that the plant model is subjected to uncertainties and the design specifications were written in the form of loop shape constraints. They used the H∞ or LQG/LTR as design tools [5]. Yu, Shen, Li and Chan (2005) proposed a coordinated nonlinear auto-disturbance-rejection controller for the excitation system and the static compensator of a four-bus power system. They introduced a dynamic feedback linearization method based on a nonlinear extended state observer. Their simulation results showed the excellent performance using their proposed controller against disturbances and model uncertainties [6].

Tang and Zhang (2006) studied the optimal rejection with zero steady-state error of sinusoidal disturbances for linear systems with time-delay. They constructed a disturbance compensator to counterbalance the external sinusoidal disturbances based on the internal model principle. They attained an approximate physically realizable optimal control law avoiding complex calculations [7]. Hoagg and Bernstein (2007) studied a fixed gain analysis of a high-gain-stabilizing dynamic compensator for command following and disturbance rejection. Their compensator utilized a Fibonacci series construction to control systems with unknown-but-bounded relative degree [8]. Li, Herrmann, Stoten, Tu and Turner (2008) considered the disturbance rejection problem of stable systems with input saturation based on the anti-windup framework. They applied their approach to the control of a dynamic sub-structured system subjected to a measurable disturbance signal and actuator limits [9].

Shamsuzzoha and Lee (2008) proposed a PID controller design method which was mainly focused on disturbance rejection. They illustrated their approach for delayed integrating process, delayed double integrating process and a boiler steam drum [10]. Otsuka and Hinata (2009) introduced the concept of generalized S(C,A,B)-pairs. They formulated the parameter-insensitive disturbance rejection problem with dynamic compensator and presented its solvability conditions with illustrative example [11]. Lee, Pan and Huang (2010) investigated robust observer-controller compensator design using Vidyosagar's structure. They illustrated the application of the proposed method in rejecting input and output step disturbances and input and output multiple sinusoidal disturbances [12]. Vrancic and Huba (2011) presented a tuning technique based on characteristic measured magnitude optimum criterion for some unstable processes. They used inner compensator to stabilize the process which was controlled by 2DOF PI controller tuned for desired tracking or disturbance rejection performance [13].

Hast and Hugglund (2012) presented design rules for optimal feedforward controllers with lead-lag structure in the presence of measurable disturbances. They derived the rules for open-loop setting considering a step disturbance. The design rules were optimal in the sense of minimizing an integrating error function (ISE and IAE) [14]. Lee, Chang and Chang (2013) proposed a modified discrete Smith predictor control scheme for stable processes with dead time. They presented different simulation examples for periodic disturbance rejection with comparison with other work about periodic disturbance rejection [15]. Thirunavukkarasu, Zyla, George and Priya (2013) tuneda PID controller in closed-loop with time-delay for double integrator systems for particular stability margins. They considered a delayed double integrating process of 0.7 gain and 0.1 s time delay, showing the load disturbance response [16].

Li, Wu, Li, Yang and Li (2014) proposed an optimal disturbance rejection control method for systems with disturbance using a compound neural network prediction approach. They applied their proposed scheme to control the temperature of a jacketed stirred tank heater showing the response curves for set-point input and external disturbance input [17]. Hassaan (2014) studied the application of PD-PI controllers to control difficult processes such as highly oscillating second-order-like and first-order delayed processes. He could achieve excellent performance to step-input change for both processes through controller tuning using ISE objective function [18,19]. Wang, Wang, Pan and Guo (2015) proposed a method for designing of roll motion controller to restrain wave disturbance and improve roll stabilizing performance under different sea conditions. They applied active disturbance rejection fuzzy control based on nonlinear motion model of autonomous underwater vehicle. The results showed better robustness [20]. Anil and Sree (2015) designed a PID controller for various forms of integrating systems with time delay using direct synthesis method. They applied the proposed controller design to various transfer function models showing step reference input and step disturbance responses [21].

II. CLOSED-LOOP CONTROL SYSTEM

The closed-loop control system incorporated a PD-PI controller and a delayed double integrating process. The control system is a linear invariant one having two inputs, a reference input and a disturbance input. The block diagram of the system is shown in Fig.1.

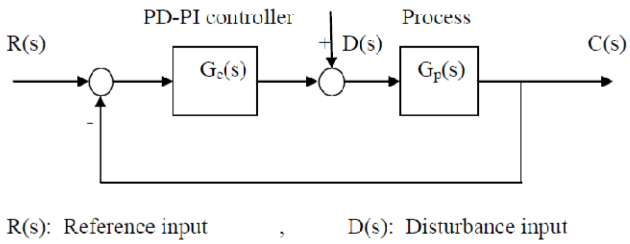

Fig.1 Block diagram of the control system.

The closed-loop control system of Fig.1 has two inputs: the reference input R(s) and the disturbance input D(s). To investigate the effectiveness of the proposed controller in disturbance rejection, the reference input R(s) will be omitted from the block diagram, and the transfer function C(s)/D(s) will be derived.

The process is a delayed double integrating one having the transfer function:

$$G_p(s) = (K_p/s^2)\exp(-T_d s) \qquad (1)$$

Where K_p is the process gain and T_d is its time delay.

Using first-order Taylor expansion for the time delay expression [axp($-T_d s$)], Eq.1 becomes [22]:

$$G_p(s) = (-T_d s + K_p) / s^2 \qquad (2)$$

The controller is a PD-PI controller having the transfer function [23]:

$$G_c(s) = [K_{pc}K_d s^2 + (K_{pc}+K_iK_d)s + K_i] / s \qquad (3)$$

Where K_{pc} is the proportional gain of the controller, K_i is its integral gain and K_d is its derivative gain.

The closed loop transfer function of the closed loop control system, C(s)/D(s) is given using the block diagram of Fig.1 and Eqs.2 and 3 by:

$$C(s)/D(s) = (b_0s^2+b_1s)/(a_0s^3+a_1s^2+a_2s+a_3) \qquad (4)$$

Where:

$b_0 = -T_dK_p$, $b_1 = K_p$

$a_0 = 1 - T_dK_pK_{pc}K_d$

$a_1 = K_pK_{pc}K_d - T_dK_p(K_{pc} + K_iK_d)$

$a_2 = K_pK_{pc} + K_pK_iK_d - T_dK_pK_i$

$a_3 = K_pK_i$

III. CONTROLLER TUNING

Tuning of the PD-PI controller allows adjusting the controller three parameters to achieve successful rejection of the input disturbance. The desired steady-state response in this case is zero. This means that the control system has to be less sensitive to disturbance input. This allows us to define an error function e(t) as the time response to its disturbance input d(t). That is:

$$e(t) = c(t) \qquad (5)$$

The controller tuning is performed using the error function of Eq.5 which is incorporated in an objective function to be minimized using the MATLAB optimization toolbox [24]. The objective functions used are [25-28]:

ITAE: $\int t|e(t)|\,dt$ (6)

ISE: $\int [e(t)]^2\,dt$ (7)

IAE: $\int |e(t)|\,dt$ (8)

ITSE: $\int t[e(t)]^2\,dt$ (9)

ISTSE: $\int t^2[e(t)]^2\,dt$ (10)

The tuning results for a delayed double integrating process of unit gain and unit time constant with the specification parameters of a unit step disturbance input are given in Table 1.

TABLE 1
PD-PI CONTROLLER TUNING AND CONTROL SYSTEM PERFORMANCE

	ITAE	ISE	IAE	ITSE	ISTSE
K_{pc}	0.1569	0.1615	0.1263	0.1727	0.1816
K_i	0.0963	0.0981	0.0502	0.1139	0.1254
K_d	5.0012	5.0015	5.0006	5.0016	5.0017
C_{max}	3.6899	3.3843	3.9866	3.4621	3.6192
T_{cmax} (s)	2.4181	2.2655	4.0000	1.9275	1.5091
T_s (s)	15.5579	14.7537	19.2417	14.0540	11.8897

IV. DISTURBANCE REJECTION

The time response of the control system for a unit gain and unit time delay double integrating process using a PD-PI controller using the five objective functions of Eqs.6 to 10 is shown in Fig2.

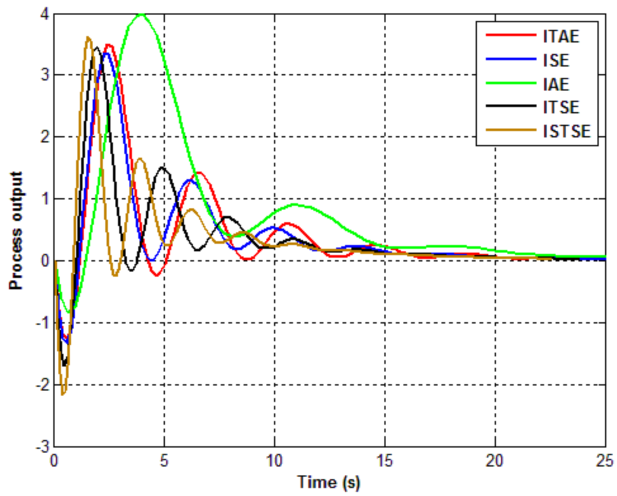

Fig.2 Unit disturbance system time response for a unit gain and unit time delay double integrating process.

The effect of the time delay of the process on the dynamic performance of the control system when disturbance rejection is the objective and using the ISTSE objective function is shown in Fig.3.

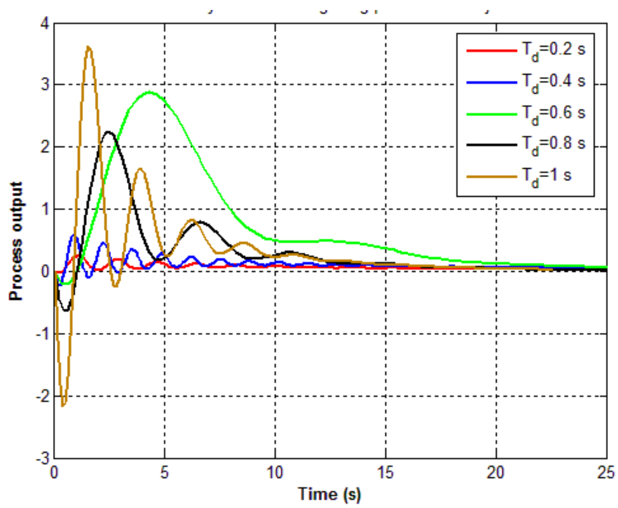

Fig.3 Effect of process time delay on the system disturbance time response.

The effect of the process time delay on the maximum process output and settling time due to unit step disturbance input using the ISTSE objective function is shown in Fig.4.

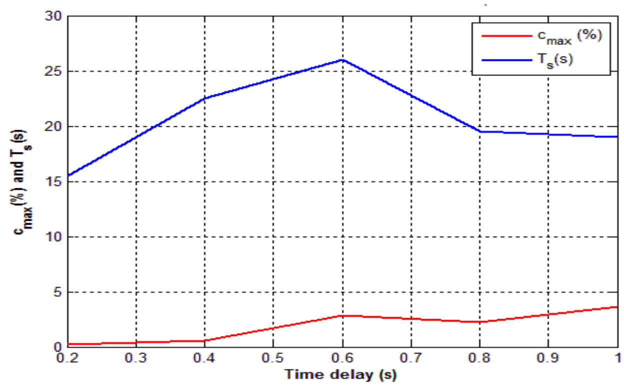

Fig.4 Effect of process time delay on the maximum process response and its settling time.

V. COMPARISON WITH OTHER RESEARCH WORK

The results of the present research using a PD-PI controller to reject the disturbance is compared with that of Anil and Sree using a PIDF controller for the same process of a delayed double integrating process having a unit gain and a unit time delay [21]. The unit step disturbance response of the control system is shown in Fig.5.

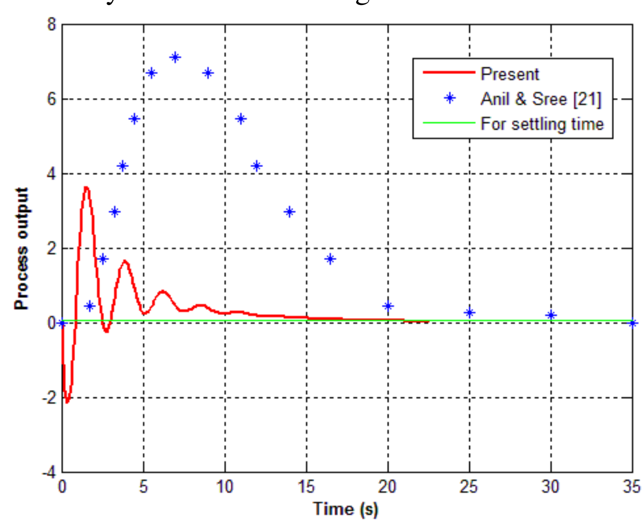

Fig.5 Comparison of the unit step disturbance.

The control system performance is compared in Table 2 between the present technique and the Anil and Sree technique using a PIDF controller.

TABLE 2
PERFORMANCE COMPARISON

	c_{max}	T_{cmax} (s)	Ts (s)
Present	3.619	1.509	19
Anil & Sree [21]	7.100	7.000	32.5

The settling time, T_s is assigned as the time where the time response of the process violates and stays within a band of ± 0.05. This simply because the steady-state response of the control system in the dynamic case in hand is zero. So, there is no meaning to use the traditional zone of ± 0.05 c_{ss}.

VI. CONCLUSIONS

- A PD-PI controller was used for disturbance rejection associated with delayed double integrating processes.
- A process time delay between 0.2 and 1 seconds was covered.
- The controller was tuned using the MATLAB optimization toolbox and five different objective functions were examined.
- The time response of the control system to a unit disturbance input had an oscillating nature for all the objective functions investigated.
- Better control system performance based on time response was obtained using the ISTSE objective function.
- The effect of process time delay on the control system performance was investigated during disturbance rejection.
- The maximum output time response varied between 0.25 and 2.877.
- The time at the maximum output time response varied between 0.859 and 4.313 seconds.
- The settling time of the time response varied between 15.5 and 26 seconds.
- Comparing with the work of Anil and Sree [21], the maximum response for a unit disturbance input of a unit gain and unit time delay double integrating process was 3.619 compared with 7.1 for Anil and Sree.
- The time at the maximum time response was 1.509 s compared with 7 s for Anil and Sree.
- The settling time was 19 s compared with 32.5 s for Anil and Sree.

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