Comparison of adiabatic and Conventional CMOS

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Abstract*:*-The Power dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation.With the help of TANNER simulations, the energy consumption is analyzed by variation of parameter. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter. It is finding that adiabatic technique is good choice for low power application in specified frequency range.

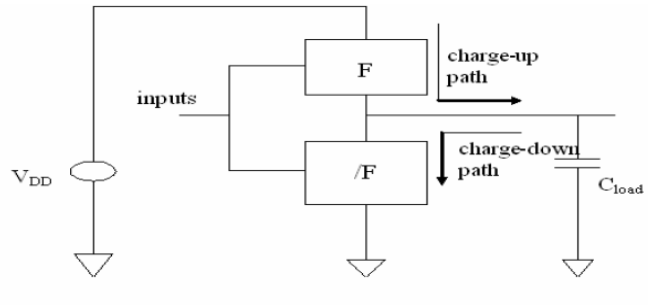
***Keywords*: Adiabatic, VLSI, T-SPICE,Inverter and NAND using CMOS, ECRL and PFAL.**

1.Introduction

The term "adiabatic" describe the thermodynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. But in VLSI, the electric charge transfer between nodes of a circuit is considered as the process and various techniques can be applied to minimize the energy loss during charge transfer event. Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component. In conventional CMOS logic circuits, from 0 to VDD transition of the output node, the total output energy drawn from power supply and stored in capacitive network. Adiabatic logic circuits reduce the energy dissipation during switching process, and utilize this energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage. The equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source. Adiabatic Logic does not abruptly switch from 0 to VDD (and vice versa), but a voltage ramp is used to charge and recover the energy from the output. Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy[1]. A brief description of some of these techniques is as CMOS ECRL and PFAL .

1.1 CMOS :

The latest technology used for constructing integrated circuits is Complementary metal–oxide–semiconductor (CMOS). The technology is being used in various digital and analogy logic circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of applications.



" Fig. 1. Logic diagram of CMOS."

It is also known as complementary-symmetry metal–oxide–semiconductor (COSMOS) because it uses complementary and symmetrical pairs of both p& n type semiconductor field effect transistor. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off , the series combination draws significant power for short duration of time only while switching between on and off states. Also, CMOS devices produce lesser

heat in comparison to other forms of logic, e.g., PMOS or NMOS logic[2]. The main reason which

made CMOS the most used technology to be implemented in VLSI chips is that, it allows large number of logic functions on a chip.

1.2Adiabatic Principle

The word ADIABATIC emanates from a Greek word that is utilized to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In authentic-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by decelerating the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as ENERGY RECOVERY CMOS. In the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems. Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits). Here, R is the resistance of the PMOS network. A constant charging current corresponds to linear voltage ramp **[3].** Assume, the capacitor voltage VC is zero initially.

The voltage across the switch = IR 1

P(t) in the switch $=I^2R$ 2

Energy during charge = $(I^2R)T$

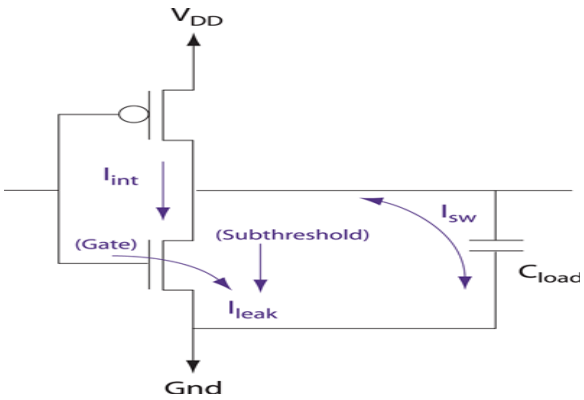
E $E=(I^2R)T=(CV/T)^2$ RT $=C^2V^2/T$ R 3

E = Edis $=(RC/T)CV^2 =(2RC/T)\ (1/2CV^2)$ 4

where, the various terms of Equation (3) are described as follows:

E — energy dissipated during charging,
Q — charge being transferred to the load,
C — value of the load capacitance,
R — resistance of the MOS switch turned on,
V — final value of the voltage at the load,
*T*_ time .

Now, a number of observations can be made based on Equation (3) as follows:



"Figure.2:Adiabatic logic."

(i) The dissipated energy is smaller than for the conventional case, if the charging time T is larger than 2RC. That is, the dissipated energy can be made arbitrarily small by increasing the charging time,
(ii) Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation[4].

Table I. Comparison between Fully adiabatic and partially adiabatic

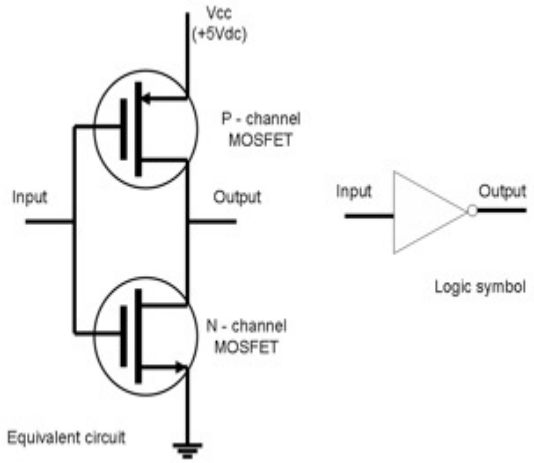
Fully Adiabatic	Partially energy adiabatic
All charge on the load capacitance is recovered by the power supply.	Some charge is allowed to be transferred to the ground
More complex architecture	Simpler architecture.
Lose energy due to leakage current through non ideal switches	Energy loss is directly proportional to the capacitance driven and square of threshold voltage
Related techniques:- 1. Pass transistor adiabatic 2. logic(PAL) 3. split rail charge recovery 4. logic(SCRL)	Related techniques:- 1. Efficient Charge Recovery Logic(ECRL) 2. 2N2N2P Adiabatic Logic

"Table1:Comparison of between fully adiabatic and partially adiabatic."

3.LOGIC STYLE

3.1 CMOS INVERTER

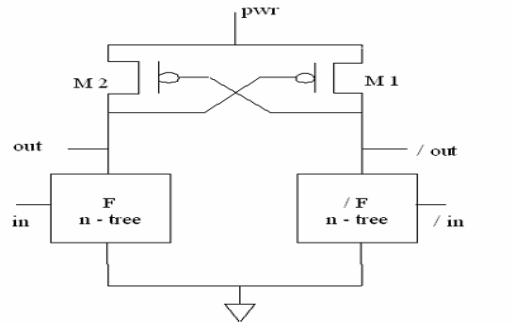
The most important CMOS gate is the CMOS inverter. It consists of only two transistors, a pair of one N-type and one P-type transistor. As fig.1 shows the basic circuit of CMOS Inverter.Voltage levels are at logical '1' corresponding to electrical level VCC, a logical '0' (corresponding to 0V or GND)[5] .



"Fig. 3: CMOS Inverter."

3.2 ECRL INVERTER

ECRL technology is that in which precharge and evaluation simultaneously performed and by implementing this method energy dissipation is reduced to a large extent. ECRL eliminates the precharge diode which dissipates less energy than the other adiabatic methods. It can also eliminates the need of more number of PMOS switches, in ECRL only two PMOS switches are used and it is the matter of fact that PMOS is the big source of power dissipation. It provides the charge on the output with full swing and it charges the load capacitance with the constant supply which is completely independent of the input signal [6]**.**

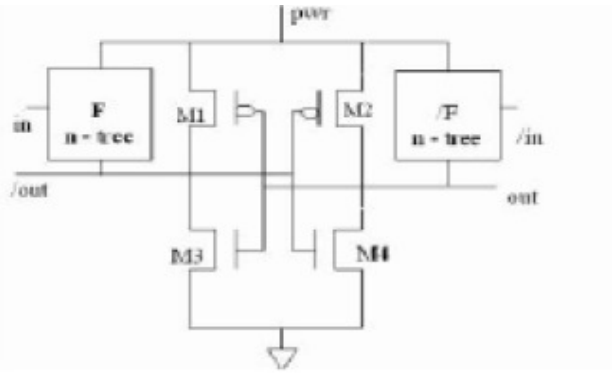


"Figure4:ECRL Inverter."

The circuit has two cross coupled transistors M1 and M2 of PMOS and two NMOS functional blocks for ECRL adiabatic logic implementation. An AC power supply pwr is used, so as to recover and reuse the supplied energy. Both out and /out are drive a constant load capacitance independent of the input signal. The cross coupled PMOS transistors helps for obtaining full swing in both precharge and recover phases. ECRL always provides the charge on the outputwith the full swing . hence, the voltage on the supply clock approaches to $|Vtp|$, the PMOS transistor gets turned off.

3.3PFAL INVERTER

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions[7]. This logic family also generates both positive and negative outputs.

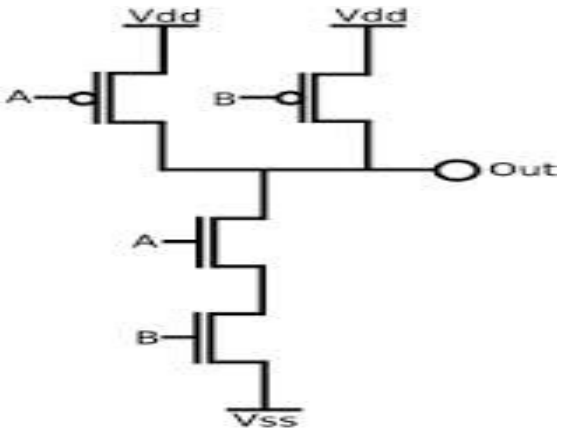


"Figure5:PFAL Inverter."

Thus the equivalent resistance is smaller when the capacitance needs to be charged.

3.4 CMOS NAND

A NAND gate (Negated AND or NOT AND) is a logic gate which produces an output that is false only if all its inputs are true. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. The NAND gate is significant because any Boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness[8].

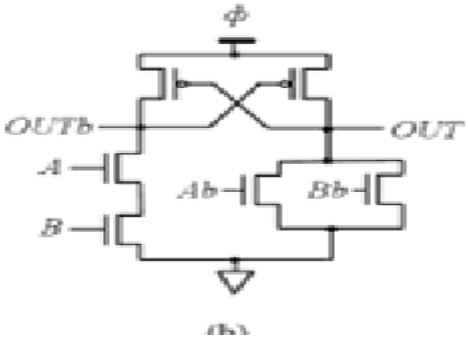


"Figure6:CMOS NAND Gate."

In CMOS NAND circuit, PMOS are connected in parallel and NMOS is connected in series.

3.5. ECRL NAND

It functions same as that of CMOS NAND circuit.



"Figure7:ECRL NAND Gate."

3.6 PFAL NAND

It consist of two inverters in which both out and /out are cross coupled to both the inverters. In left side of the inverter two NMOS are connected parallel and in right
hand side two NMOS are connected serially. It has power clock and ground connection
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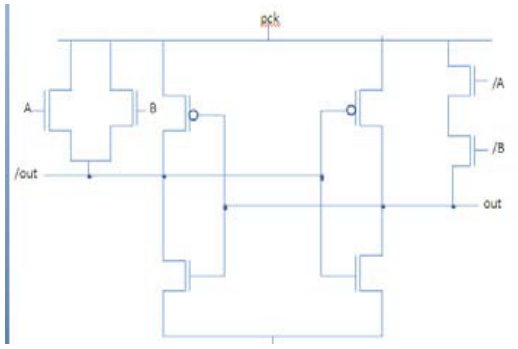
[9].



"Figure6:PFAL NAND Gate."

CONCLUSION :-

The adiabatic approach to VLSI circuit design is an attractive method in designing low power dissipating digital applications. This paper primarily focuses on the design of low power high speed CMOS cell structures. A family of conventional CMOS Logic and an Adiabatic Logic units were designed and simulated on the tanner using the 0.18 µm CMOS technology and further analysis of average dynamic power dissipation with respect to the frequency and load capacitance was done. It was observed that the adiabatic logic style is advantageous in applications where power reduction as well as speed is of prime importance. In this paper,We observed that an improvement of 90 to 95% in energy savings as compared with conventional CMOS circuits.

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