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An Advanced Topology for Cascade Multilevel Inverter Based on Developed H-Bridge

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Abstract— In this paper, an advanced topology for cascaded multilevel inverter using developed H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches ,which results in decreased complexity and total cost of the inverter. Moreover, a Bee algorithm(BA) to determine the magnitude of dc voltage sources is proposed. It is used to solve the transcendental equations for finding the switching angles. This algorithm can be used for any number of voltage levels without complex analytical calculations. Simulation results for 15-level inverter verify the validity and effectiveness of the proposed algorithm.

Keywords—. Cascaded multilevel inverter, Developed H-bridge, Multilevel inverter, Bee Algorithm, Multicarrier PWM technique,Voltage source inverter.

I.INTRODUCTION

Basically Inverter is a device that converts DC power to AC power at desired output voltage because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference [1],[2]. and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, were going to multilevel inverter[3].Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform..The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage[4]. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multi level inverters are mainly classified as Diode clamped, Flying capacitor inverter and cascaded multi level inverter[5].The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. Moreover, abundant modulation techniques have been developed in cascade multilevel inverter and reducing the power losses.The most attractive features of multilevel inverters are as follows.

1.They can generate output voltages with extremely low distortion and lower order harmonics.

2. They draw input current with very low distortion.

3.In addition, using sophisticated modulation types of methods, CM voltages can be eliminated.

4.They can operate with a less switching frequency.

II.CASCADE MULTILEVEL INVERTER

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are $2n+1$, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two types.Figure.1 shows the power circuit for one phase leg of a three-level and five-level cascaded inverter. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors. The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc. The output voltage of an M-level inverter is the sum of all the individual inverter outputs. Each of the H- Bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi- square waveform by phase- shifting ts positive and negative phase legs with switching timings.Further each switching

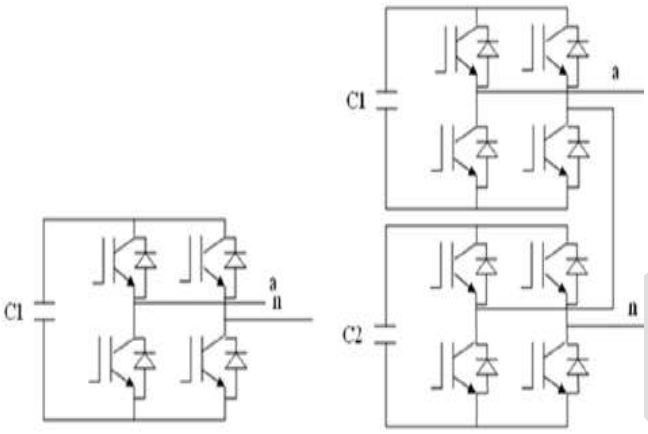

Figure.1. Single Phase Structures Of Cascaded Inverter (A)3-Level,(B)5-Level

device always conducts for 180˚ (or 1/2 cycle)regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device. This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches.The major advantage of this topology and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage

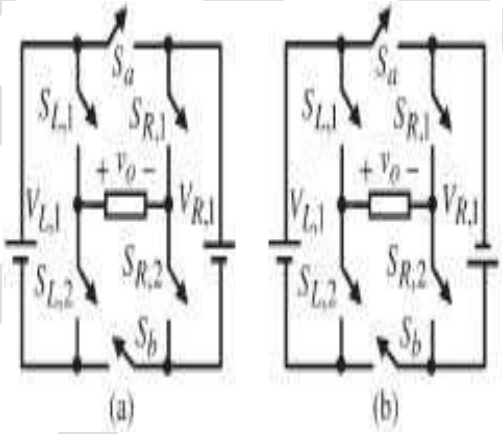

Fig. 2.Proposed seven level inverters
(a).First proposed topology,(b). Second proposed topology

TABLE I
OUTPUT VOLTAGES OF THE PROPOSED SEVEN- LEVEL INVERTERS

No.	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o (Fig. 1(a))	v_o (Fig. 1(b))
1	1	0	0	1	0	1	$V_{L,1}$	$V_{L,1}$
2	1	0	0	1	1	0	$V_{R,1}$	$-V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}-V_{R,1}$	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1}$	$-V_{L,1}$
6	0	1	1	0	0	1	$-V_{R,1}$	$V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}-V_{R,1})$	$-(V_{L,1}+V_{R,1})$

In this paper, in order to increase the number of output voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed[2],[4],[7] and [8].Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of IGBTs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed topology in generating all voltage levels through a 15-level inverter is confirmed by simulation using power system computer aided design (PSCAD) software.

III. ADVANCED TOPOLOGY

It can be obtained by adding two unidirectional power switches and one dc voltage source to the H- bridge inverter structure. In other words, the proposed inverters are comprised of six unidirectional power switches ($S\,a$, $S\,b$, $S\,L,1$, $S\,L,2$, $S\,R,1$, and $S\,R,2$) and two dc voltage sources ($VL,1$and $VR,1$).Inthis paper, these topologies are called the developed H bridge. As shown in Fig. 2,the simultaneous turn on of $S\,L,1$ and $S\,L,2$ (or $S\,R,1$ and $S\,R,2$)causes the voltage sources to short circuit in that Figure2.Then the simultaneously turned on to mentioned switches must be avoided. In addition, $S\,a$ and the $S\,b$ should not turn on. The difference in the topologies illustrated in Fig.1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc volt age sources.

An advanced topology, the number of output voltage levels (N step), number of switches (N switch), number of dc voltage sources (N source), and the maximum magnitude of the generated voltage are calculated as follows, respectively:

$$N_{step} = 2^{2n+1} - 1 \quad (1)$$

$$N_{switch} = 4n + 2 \quad (2)$$

$$N_{source} = 2n \quad (3)$$

IV.BEE ALGORITHM

The Bee algorithm is an optimization algorithm based on the natural foraging behaviour of honeybees to find the optimal solution[6]. A bee colony consists of three kinds of bees: employed bees on-looker bees, and scout bees. Employed bees carry information about place and amount of nectar in a particular food source. They transfer that form information to on-looker bees with dance in that of hive. The time of dance determines the amount of nectar in a food source An on-looker chooses a food source based on the amount of nectar in a food source A good food source attracts more on-looker bees to itself. Scout bees seek in search space and find new food sources. Scout bees control the exploring process, considered as possible solutions to a problem[5].The food source is a *D*- dimensional vector, where *D* is while employed and on-looker bees play an exploiting role. In this algorithm, food sources are the number of optimization variables.The amount of nectar in a food source determines the value of fitness.The basic flowchart of BA is shown in Fig. 3.

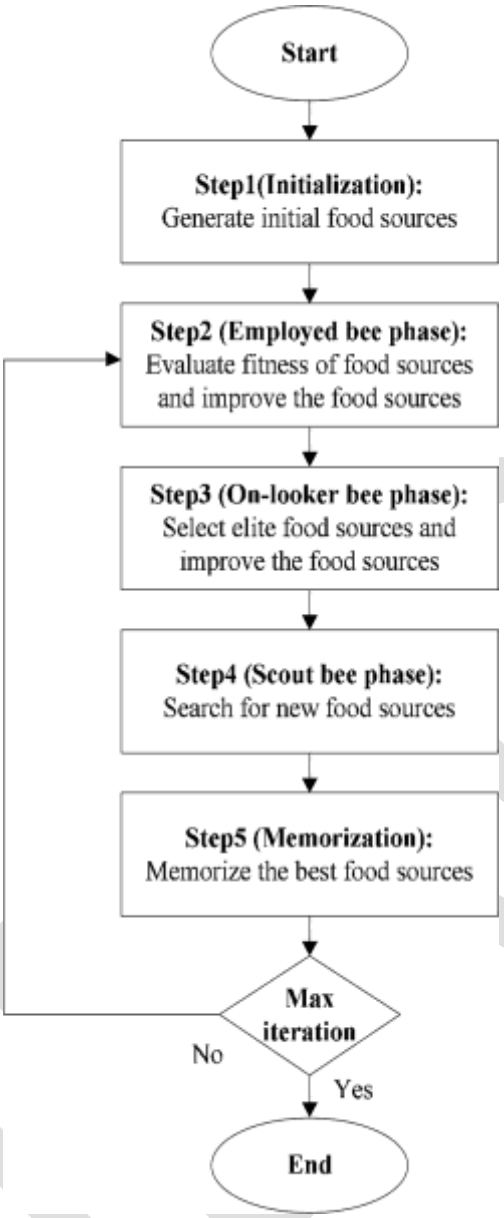

Fig.3.Basic Flowchart of BA

In step 1, random initial food sources are generated. The number of initial food sources is half of the bee colony. In step 2, employed bees are sent to the food sources to determine the amount of nectar and calculated to its fitness. For each food source, there is only one employed bee. So, the number of food sources is equal to the number of employed bees. In addition, the employed bees modify the solutions, saved in memory, by searching in the neighbourhood of its food source.The employed bees save the new solution if its fitness is better than the older one. Employed bees go back to the hive and share the solutions with the onlooker bees. In step 3, on-looker bees, which are another half of the colony, select the best food sources using a probability-based selection process. Food sources with more nectar attract more on-looker bees. On- looker bees are sent to the selected food sources. The on-looker bees improve the chosen solutions and calculate its fitness. Similar to employed bees, the on-looker bees save a new solution if its fitness is better than an older solution. In step 4, the food sources that are not improved for a number of iterations are abandoned. So, the employed bee is sent to find new food sources as a scout bee. The abandoned food source is replaced by the new food source. Finally, in step5, the best food source is memorized. The maximum number of iterations is set as a termination criterion which is checked at the end of iteration. If it is not met, the algorithm returns to step2 for the next iteration.

V.ADVANCED ALGORITHM TO DETERMINE MAGNITUDES OF DC VOLTAGE SOURCES

In this paper, the following algorithm is applie d to determine the magnitude of dc voltage sources. It is important to note that all voltage levels (even and odd) can be generated.

A. Proposed Seven-Level Inverter

The magnitudes of the dc voltage sources of the 7- level inverter shown in Fig.2(b) are determined as follows

$VL,1 = V\text{dc}$ (4)

$VR,1 = 2V\text{dc}.$ (5)

Considering (5), (6) Table I, the proposed 7level inverter can generate 0, $\pm 1V, \pm 2V, \pm 3V\text{dc}$ at output voltage.

B. Proposed 15-Level Inverter

The magnitudes of the dc voltage sources of the proposed15level inverter are recommended as follows:

$VL,1 = V\text{dc}$ (6)

$VR,1 = 2V\text{dc}$ (7)

$VL,2 = 5V\text{dc}$ (8)

The proposed inverter can generate all negative and positive voltage levels from 0 to $15V\text{dc}$ with steps of $V\text{dc}$.

C. Proposed General Multilevel Inverter

The magnitudes of the dc voltage sources of the proposed general multilevel inverter can be obtained as follows:

$VL,j = 5^{j-1}\ V\text{dc}$ for $j = 1, 2, 3, \ldots, n$ (9)

$VR,j = 2 \times 5^{j-1}\ V\text{dc}$ for $j = 1, 2, 3, \ldots,$. (10)

Considering (4) and (16), the values of Vo, max and Vblock, n of the proposed general multilevel inverter are as follows,respectively:

$\text{Vo,max} = \text{VL},n + \text{VR},n = 3 \times 5^{n-1}\text{Vdc}$ (11)

$\text{Vblock},n = 4(\text{VL},n + \text{VR},n) = 12(5^{n-1})\text{Vdc}$ (12)

VI. SIMULATION RESULTS

In order to verify the correct performance of the proposed multilevel inverter in generating all output voltage levels (even and odd), a 15 level inverter based on the topology shown in Fig.2.It has been used for the simulation and Table I shows the switching states of the 15-level inverter. The simulation is done by using PSCAD software. The simulated output voltage and current waveforms are shown in Fig.4.As Fig.4(a) shows, the proposed topology is able to generate 15 levels (15 positive levels, 15 negative levels, and 1 zero level) with the maximum voltage of 225 V. Comparing the output voltage and current waveform indicates that the output current waveform is more similar to the ideal sinusoidal waveform than the output voltage because the *R–L* load acts as a low-pass filter. In addition, there is a phase difference between the output voltage and current waveforms,

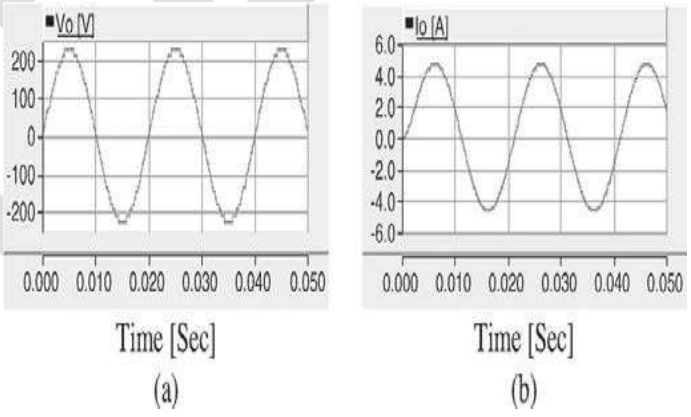

Fig.4.Proposed 15-level inverter.(a) Output voltage waveform. (b) Output current waveform.

which is caused by the inductive feature of the load. The total harmonic distortions of the output voltage and current are equal approximately below 3%,respectively.Considering the magnitude of the blocking voltage of the switches, the relations associated to the maximum voltage drop of the switches are well confirmed.Fig.5,6shows the simulation results of the implemented 15 level inverter.

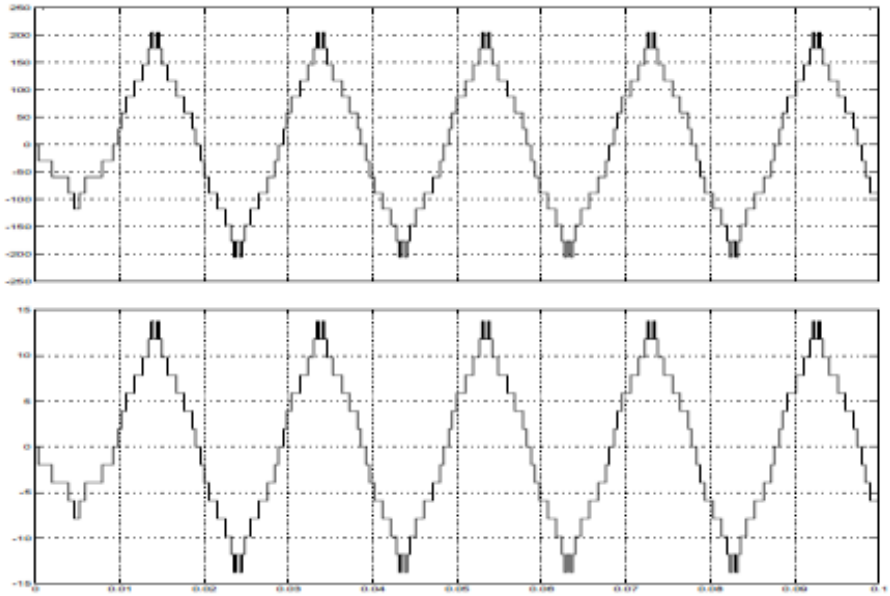

Fig.5.Simulation Output Of 15 level Inverter

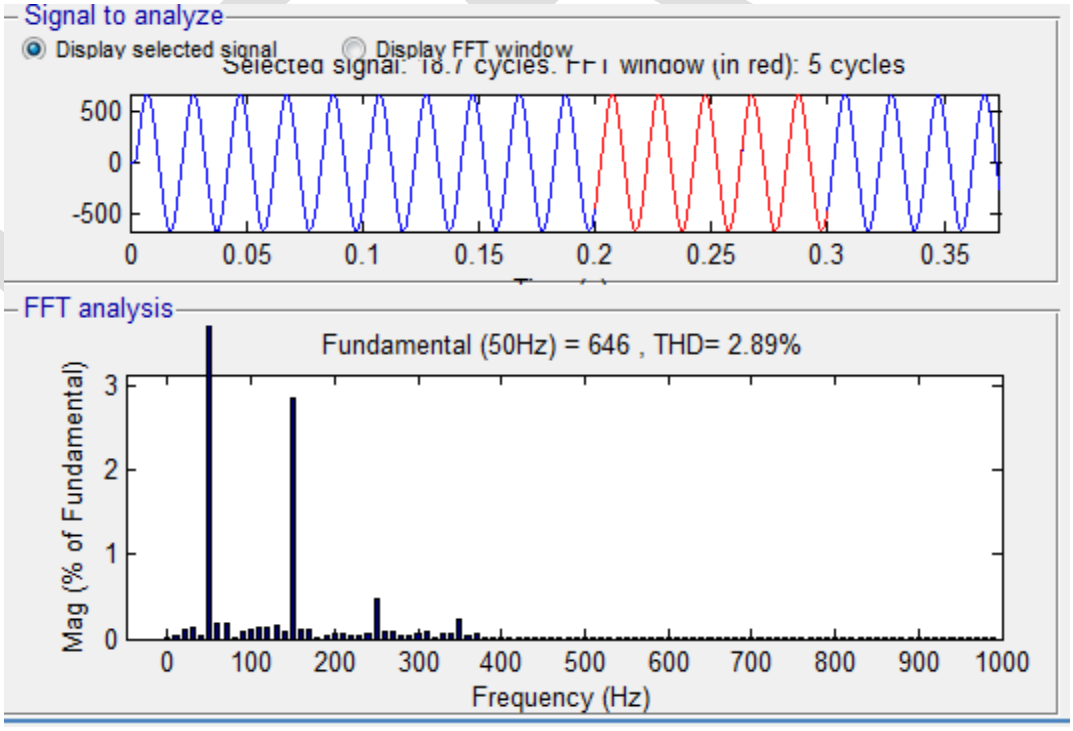

Fig.6.Proof for THD Result

VII.CONCLUSION

In this paper, an advanced topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 7-level, 15- level and general topologies are consequently presented. Therefore, in proposed system efficiency is about 97.2% and THD is below 3%.In addition, a bee algorithm to determine the magnitude of the dc voltage sources has been proposed. An advance topology was compared with the different kinds of presented in a topologies in literature from different points of this view. An according to the comparison results, hence advanced topology requires a lesser number of MOSFETs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies.

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