

# Low Power Design of Johnson Counter Using DDFF Featuring Efficient Embedded Logic and Clock Gating

Chandra shekhar kotikalapudi, Smt. P. Pushpalatha,

Dept. of Electronics and communications engineering

University College of engineering, JNTUK, Kakinada, India

E-Mail-[Sekhar2790@gmail.com](mailto:Sekhar2790@gmail.com)

**Abstract**—In this paper, we have proposed a power efficient design of a 4-bit up-down Johnson counter by using Dual Dynamic Node Pulsed Flip-flop(DDFF) featuring efficient embedded logic module(DDFF-ELM) and then clock gating is incorporated in order to reduce the power dissipation further. The proposed design employs a DDFF which mainly reduces the power consumption by eliminating the large capacitance present in the pre-charge node of several existing flip-flop designs by separately driving the output pull-up and pull-down transistors by following a split dynamic node structure. This reduces the power up to 40% compared to conventional architectures of the flip-flops. Then the Embedded logic module is an efficient method to incorporate complex logic functions into the flip-flop. Clock gating is applied to reduce the power consumption up to 50% due to unnecessary clock activities.

*Key words*—Johnson counter, DDFF, DDFF-ELM, clock gating, XCFF, CDMFF, low power.

## I. INTRODUCTION

Low power, high speed and area efficient circuit design is the major concern in now-a-day VLSI design. Designing a low power circuit involves a proper architecture of the sequential and combinational circuits used in the design by using minimum CMOS logic gates and then eliminating the redundant operations by using efficient techniques. In order to improve the performance of flip-flop architecture and reduce the power consumption extensive work has been carried out in the past few decades. With steady growth in clock frequency and chip capacity, power dissipation of the CMOS design has been increasing tremendously. This results in necessity for development of new techniques for reducing the power dissipation in VLSI design.

High speed can be achieved in synchronous systems by using advanced pipelining techniques. In all kinds of digital circuits flip-flops are used as basic storage elements. Design styles of flip-flops can be classified as static and dynamic. Static flip-flops are those which can preserve their stored values even if the clock is stopped.

Many static design flip-flop topologies have been proposed in the past. Classic transmission-gate latch based master-slave flip-flop (TGMS) and PowerPC 603 master slave latch are the examples of static design style. Basically dynamic flip-flops can achieve higher speed and lower power consumption. Dynamic flip-flops can be either purely dynamic or pseudo dynamic structures. Hybrid latch flip-flop (HLFF) and Semi-dynamic flip-flop (SDFF) are the examples of pseudo dynamic structures. Purely dynamic structures are Conditional data mapping flip-flop (CDMFF) and Cross charge control flip-flop (XCFF). To eliminate the drawback of the existing flip-flop architectures a Dual dynamic node hybrid flip-flop (DDFF) has been developed. And to reduce the pipeline overhead an embedded logic module (DDFF-ELM) has been developed. Both of these eliminate the drawbacks present in dynamic flip-flop architecture.

In this paper, we have proposed a power efficient design of 4-bit up-down Johnson counter using DDFF-ELM and applying clock gating. This design using DDFF-ELM reduces the power consumption up to 27% compared to conventional flip-flop architectures. Counter designed by applying clock gating has a maximum power reduction of up to 40%.

In section II, a brief introduction of conventional flip-flop architectures along with their disadvantages has been described and challenges in achieving high performance are also been discussed. Section III provides the details about the 4-bit synchronous up-down Johnson counter. Section IV provides the details of proposed 4-bit Johnson counter using clock

gating. In section V, we have provided simulation results of the proposed design. And finally, in section VI, we conclude with the improvements of the proposed design.

## II. FLIP-FLOP ARCHITECTURES

In order to improve the performance of the flip-flops to achieve higher speeds and low power consumption several flip-flop architectures have been designed over the past decade. All these architectures can be grouped under static and dynamic design styles. Static flip-flops are those which can preserve their stored values even if the clock is stopped. Many static design flip-flop topologies have been proposed in the past. Classic transmission-gate latch based master-slave flip-flop (TGMS) and PowerPC 603 master slave latch are the examples of static design style. TGMS is realized by using two transmission gate based latches operating on complementary clocks. PowerPC 603 master slave flip-flop is a combination of TGMS flip-flop and  $mC^2$ MOS flip-flop. Main features of the static designs are that they dissipate low power and also they have low clock-to-output (clock-Q) delay. But because of their large positive setup time static designs have large data to output delay. Whenever in the designs if the speed is not a concern static designs are more suitable.

Modern high performance flip-flops are considered under dynamic design style. Dynamic designs may be purely dynamic or pseudo dynamic. Pseudo dynamic design styles are also referred to as semi-dynamic or hybrid structures as they consist of static output and dynamic frontend. The flip-flops under this category are Hybrid latch flip-flop (HLFF) and Semi-dynamic flip-flop (SDFF). HLFF is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This sharp pulse is generated at the positive edge of the clock and delayed version of clock. Two main building blocks of SDFF are a pulse generator and a level sensitive latch. With an internally generated sharp pulse which is of short duration latch is clocked so as to make it behave like a flip-flop. Both HLFF and SDFF benefit from clock overlap to perform latching operation. Even though HLFF is not the fastest but it has low power consumption. The reason for being slow compared to SDFF is that HLFF has longer stack of nMOS transistors at the output node. SDFF is the fastest classic hybrid structure but because of the large clock load and large pre charge capacitance it is not efficient as far as power consumption is considered.

In hybrid structured designs redundant data transitions and large pre charge capacitance are the main sources of power dissipation. In order to eliminate these two problems different architectures have been designed. To reduce the redundant operations in the flip-flops Conditional data mapping flip-flop (CDMFF) is the most efficient architecture. Similarly Cross charge control flip-flop (XCFF) is considered as the best architecture to eliminate the large pre charge capacitance. In CDMFF unwanted transitions are eliminated by using an output feedback structure to conditionally feed the data to flip-flop. Thus when a redundant event is predicted this architecture reduces power dissipation by eliminating unwanted transitions. This flip-flop is bulky because of the presence of additional transistors in conditional and has more power consumption at higher data activities. In XCFF the large pre charge capacitance present at the output node is eliminated by driving output pull-up and pull-down transistors separately. Total power consumption is reduced considerably as only one of the two dynamic nodes is switched during one clock cycle. Main drawbacks in this design are conditional shutoff and charge sharing.

The Dual dynamic node hybrid flip-flop (DDFF) eliminates the large pre charge capacitance present in the output node of several conventional designs by following a split dynamic node structure to separately drive the output pull up and pull down transistors. Figure 1 shows the architecture of DDFF.

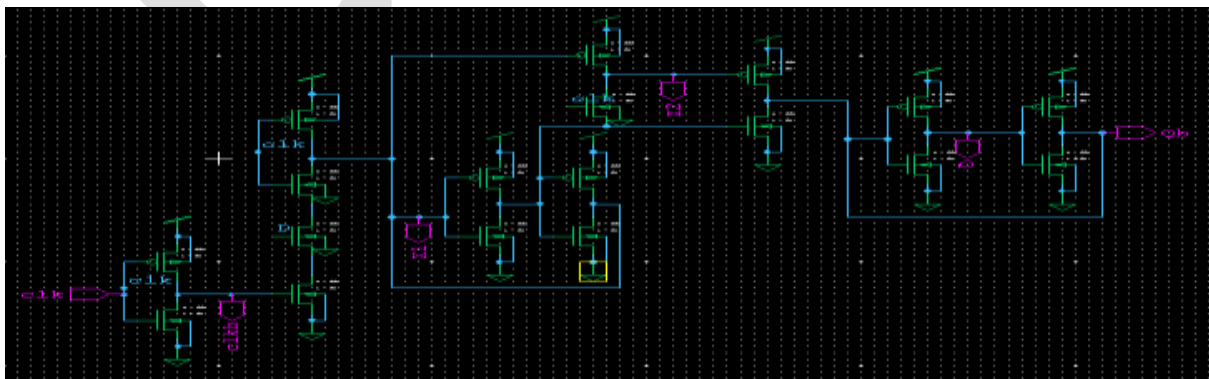


Fig 1: DDFF

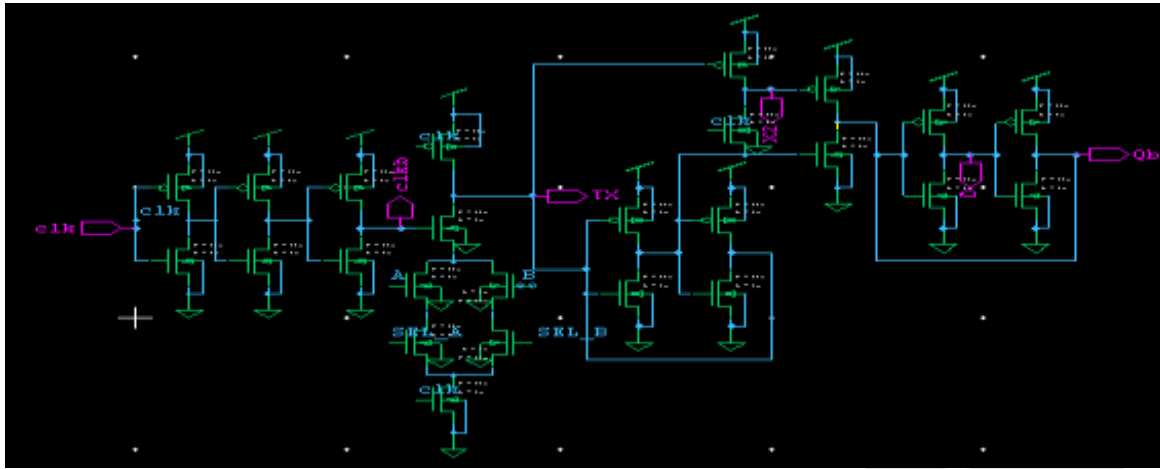


Fig 2: DDFF-ELM (MULTIPLEXER)

In the DDFF architecture, node X1 is pseudo-dynamic and X2 is dynamic. Instead of the conditional shutoff mechanism present in XCFF an unconditional one is present in DDFF. Its operation is based on whether the clock is high or low. The performance improvements show that the DDFF design is well suited for modern high performance designs where minimum delay and low power dissipation are required.

The figure 2 shows the architecture of DDFF-ELM. Complex logic functions can be efficiently embedded into the architecture of DDFF. The main advantages of DDFF-ELM over the other flip-flops that are having embedded logics are lower power consumption and capable of embedding complex logic functions.

### III. 4-BIT UP-DOWN JOHNSON COUNTER

Counter is a device that stores the number of times a particular event or process has occurred often in relation to a clock signal. Counters are used in almost all the digital circuits for counting operations. There are many types of counters used in digital circuits. Johnson counter also called as twisted ring counter is the modified form of a ring counter. Figure 3 shows the architecture of 4-bit synchronous up-down Johnson counter. In Johnson counter output of the last stage is complemented and connected to the input of the first stage.

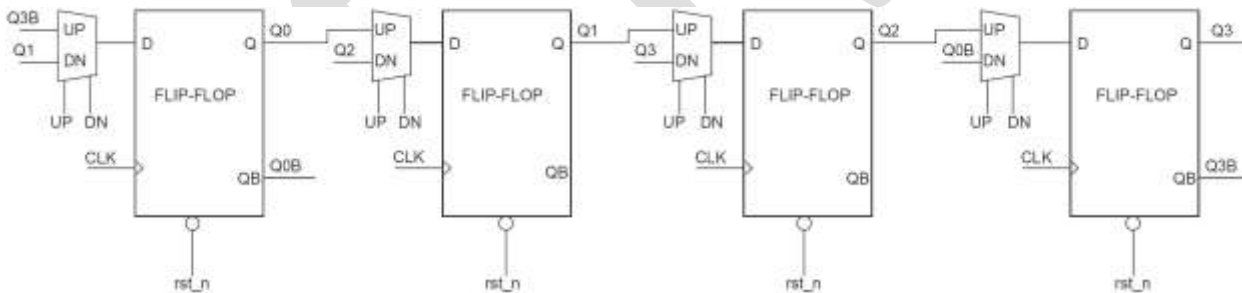


Fig 3:4-bit up-down Johnson counter

In the 4-bit up-down Johnson counter designed Dual dynamic pulsed hybrid flip-flop is used. By embedding a multiplexer into the flip-flop architecture as shown in the figure 2 counting operation can be performed in either up counting mode or down counting mode. Last stage output is complemented and connected to the input of the first stage for an up counter and first stage output is complemented and connected to last stage input as shown in the figure 3. The counting sequence repeats for every eight clock pulses. The counting sequences of the Johnson up and down counters are shown in table 1 and table 2.

clock	Q0	Q1	Q2	Q3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

Table 1: Johnson up counter

clock	Q0	Q1	Q2	Q3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0
8	0	0	0	0

Table 2: Johnson down counter

#### IV. JOHNSON COUNTER USING CLOCK GATING

Clock gating technique is used to reduce the dynamic power dissipation by stopping the clock signal to the segments of the circuit that are inactive at that instant of time. Clock transitions contribute to the major part of power consumption in a digital circuit. By eliminating the unwanted distribution of the clock signal to the segments that are not active power dissipation can be reduced in the digital circuits. For clock gating to the Johnson counter in this design XOR and NAND gates are used.

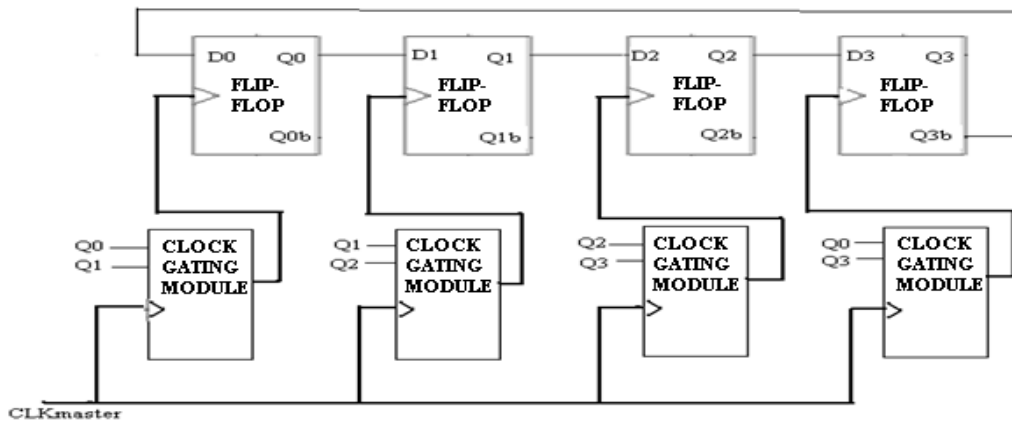


Fig 4: Clock gating to Johnson counter

Each of the Clock gating blocks in the figure 4 consists of combination of XOR and NAND gate. Clock gating module is shown in figure 5.

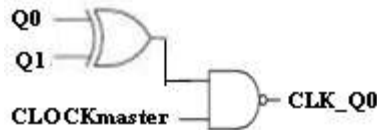


Fig 5: Clock gating module for generation of clock for Q0

## V. SIMULATION RESULTS

The existing and the proposed design are implemented in Tanner EDA tools in 250nm technology. Schematics for the design are designed in S-edit .Figure 1 shows the schematic design of the DDFF and figure 6 shows the timing diagram of the DDFF simulated using T-spice and resulting waveforms are obtained in W-edit.

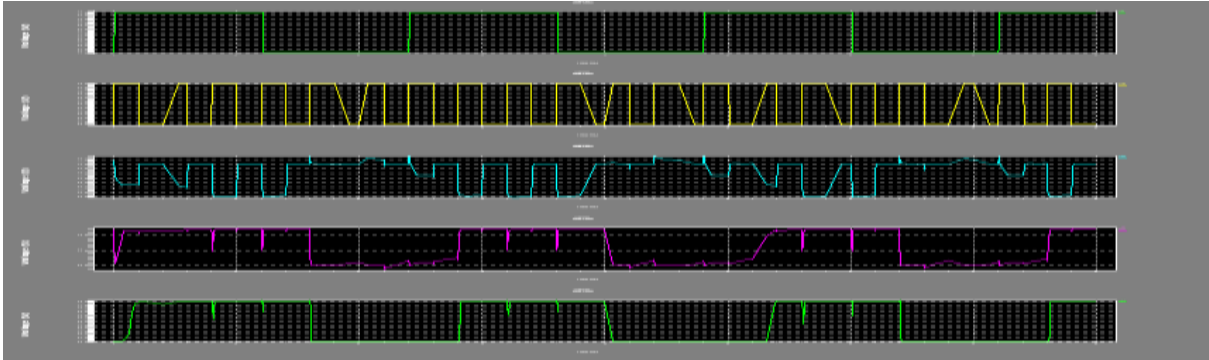


Fig 6: Timing diagram of DDFF

The simulated waveform of the Johnson counter is shown in figure 7.

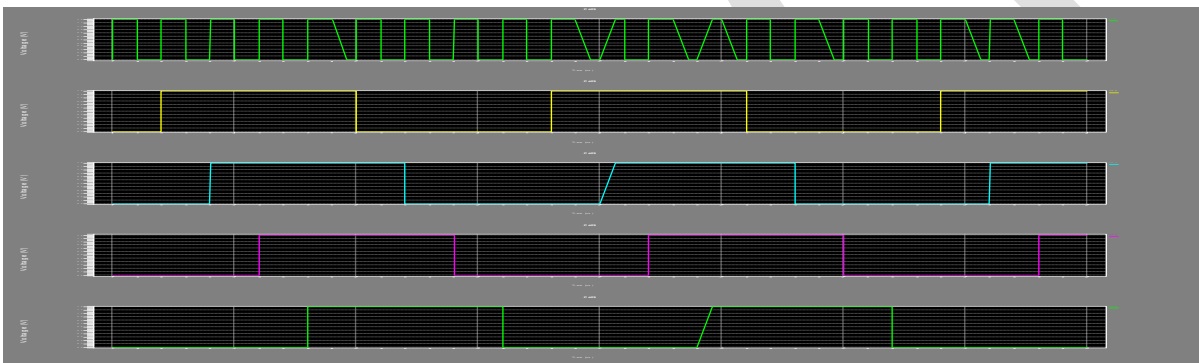


Fig 7: Timing diagram of Johnson counter

The layout designs of the DDFF, DDFF-ELM (MULTIPLEXER) and the Johnson counter are shown in the figures 8, 9 and 10 respectively. Layouts are designed and areas of the designs are calculated by using L-EDIT.

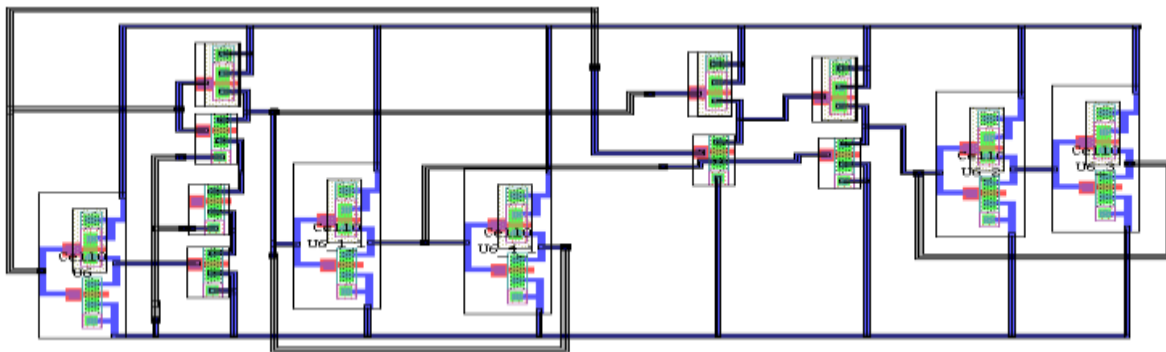


Fig 8: Layout design of the DDFF

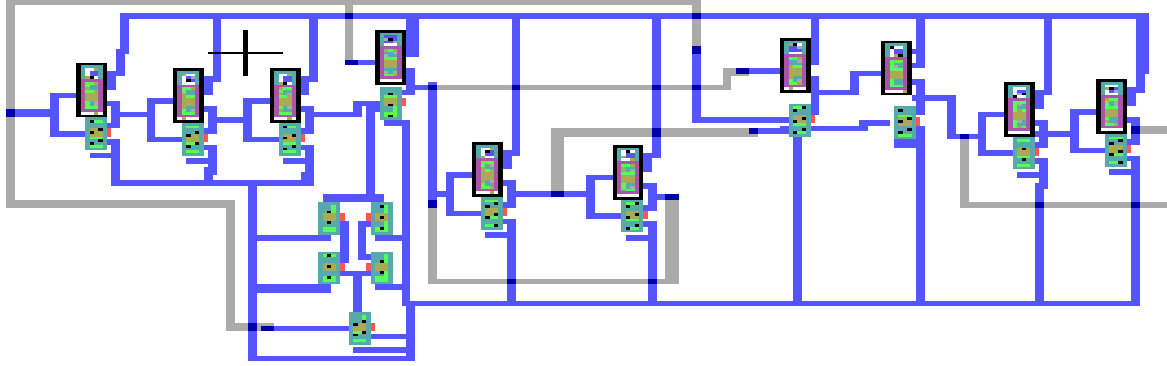


Fig 8: Layout design of the DDFF-ELM (MUX)

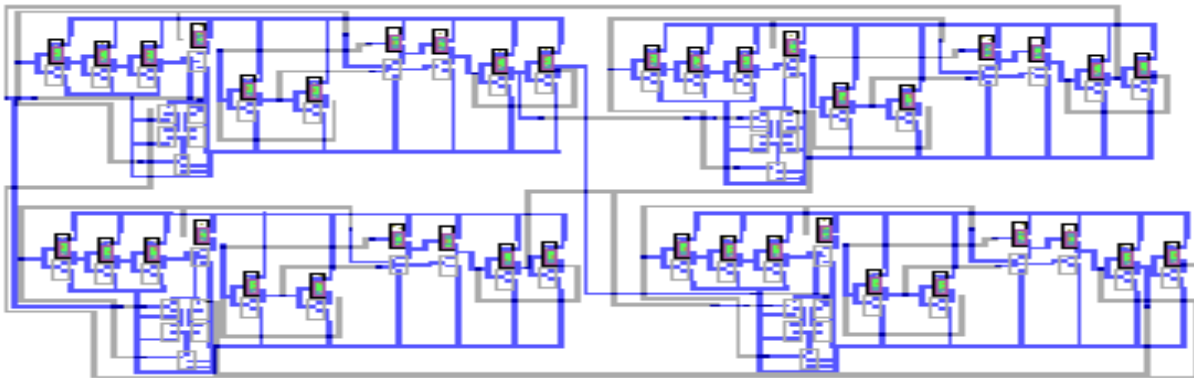


Fig 8: Layout design of the Johnson counter

Simulation results of the various dynamic flip-flops are shown in table3.

Flip-flop	Total Layout area ( $\mu\text{m}^2$ )	Total Power ( $\mu\text{w}$ )	Minimum D-Q (ns)	PDP (fJ)
CDMFF	540.67	62.34	1.37	85.40
XCFF	470.43	68.53	1.31	89.77
DDFF	430.01	59.62	1.34	79.89
DDFF-ELM	528.74	85.90	1.29	110.81

Table 3: Performance comparison of various dynamic flip-flops (250nm technology)

Area and power consumption comparison of the Johnson counter with and without clock gating are shown in table 4.

Johnson counter	Power consumption ( $\mu\text{w}$ )	Total Layout Area ( $\mu\text{m}^2$ )
Without Clock Gating	344.24	2820.32
With Clock Gating	160.56	2932.62

Table 4: Johnson counter with and without Clock gating

Power consumption of the 4-bit synchronous up-down Johnson counter is 344.24  $\mu\text{w}$ . Power consumption of the 4-bit synchronous up-down Johnson counter with clock gating is 160.56  $\mu\text{w}$ . So by using the clock gating power dissipation in the Johnson counter is reduced up to 50%.

## VI. CONCLUSION

In this paper, a dual dynamic node pulsed hybrid flip-flop (DDFF), an embedded logic module, a 4-bit synchronous up-down Johnson counter and clock gated Johnson counter are presented. Simulation results show improvements in power and speed. The dual dynamic node pulsed hybrid flip-flop (DDFF) shows improvement over the cross charge control flip-flop (XCFF) as it eliminates the redundant power dissipation. Further complex logic function can be incorporated efficiently in to the flip-flop. The 4-bit up-down Johnson counter with clock gating shows an improvement in terms of power consumption of up to 50% compared to the 4-bit up-down counter without clock gating though there is an increase in area. Thus in modern high performance designs where power consumption is a major concern the presented architecture is well suited.

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