High Speed CPL Adder for Digital Biquad Filter Design

Neva Agarwala[1]

[1]Lecturer, Department of EEE, Southeast University, Dhaka, Bangladesh

E-mail- mnagarwala@seu.ac.bd

Abstract— The project presents the comprehensive explanation of how to minimize the overall delay of a Digital Biquad Filter by comparing the time delay performance analysis among different adders. Finally, 8 bit CPL adder is used in the design methodology of this Biquad Filter for its excellent performance in timing delay calculation. At the end, it has been found that the design was fully functional and the time delay was less compare to others.

Keywords—Biquad Filter, CPL Adder, CMOS adder, ROM, Register, D Flip Flop. nmos, pmos, XOR.

1. INTRODUCTION

1.1 Review of full adder design of two different cmos logic style

Several variants of static CMOS logic styles have been used to implement low-power 1-b adder cells [1]. In general, they can be broadly divided into two major categories: the complementary CMOS and the pass-transistor logic circuits. The complementary CMOS full adder (C-CMOS) of Fig. 2 is based on the regular CMOS structure with pMOS pull-up and nMOS pull-down transistors. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. [2]

The complementary pass transistor logic (CPL) full adder with swing restoration is shownin Fig. 3. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (eitherpMOSor nMOS) is sufficient to implement the logic function, which results in smaller number of transistors and smaller input load. [3]

1.2 Aims and Objectives

The general objective of our work is to make a faster 8-bit adder and to investigate the area and power-delay performances of 1 bit full adder and 8 bit full adder cells in two different CMOS logic styles. Here, we compare the CMOS and CPL 1 bit and 8 bit full adder and use the CPL full adder in the Biquad filter because the delay is low compared to the CMOS adder.

1.3 One bit full adder

The one-bit full adder used is a three-input two-output block. The inputs are the two bits to be summed, and, and the carry bit , which derives from the calculations of the previous digits. The outputs are the result of the sum operation and the resulting value of the carry bit. More specifically, the sum and carry output are given by,

S = A xor B xor Cin ----------------------------- (1)

Co = AB+(A+B)Cin ----------------------------- (2)

From (2) it is evident that if the carry output is equal to their value. If we have (the full adder is said to be in propagate mode), and, hence, the full adder has to wait for the computation of Co.[4]

18
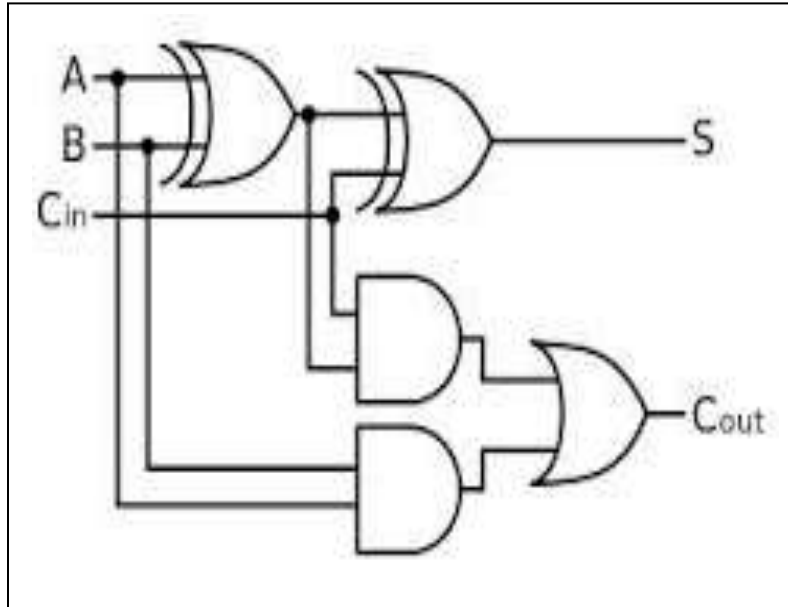
Fig 1: A full adder [4]

2. DESIGN AND SPECIFICATION

The sizing used are based on the inverter size (nmos = 3:2 and pmos = 6:2). Below are the details of 8-Bit CPL Adder modules:
- 8-bit CPL Adder
- Reference sizing from inverter with size 3:2 for nmos transistor and 6:2 for pmos transistor
- Using 1-bit CPL Adder
- 1-bit CPL Adder sizing: 6:2 for all nmos transistor and 6:2 for all pmos transistor

3. RESULTS AND ANALYSIS

We simulate the 1 bit and 8 bit full adders by using IRSIM and get different delay from these two different adders. From the simulation waveform we can easily calculate the delay

For 1 bit full adder:

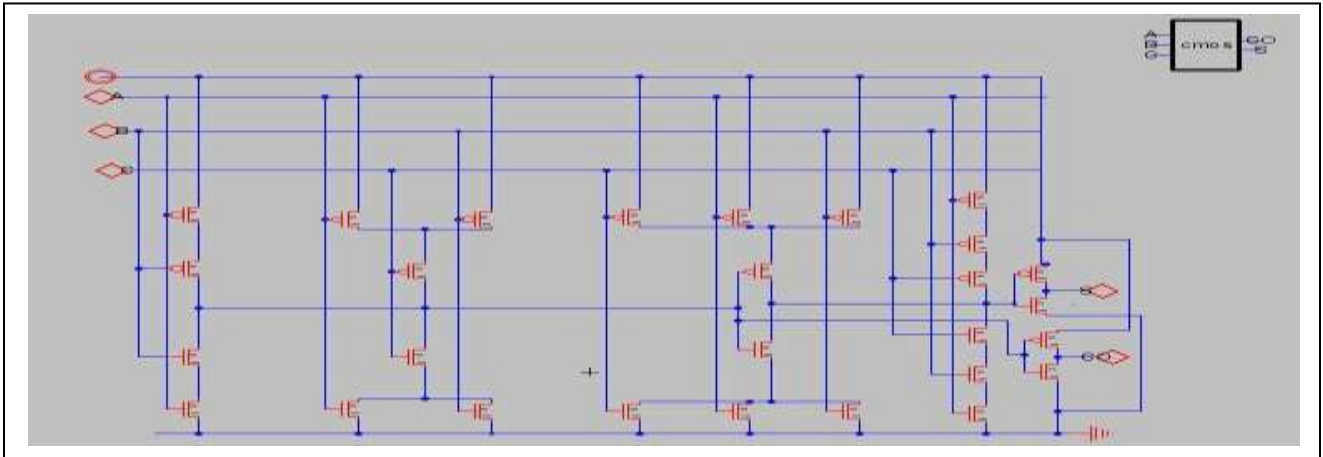CPL: 0.179ns   0.537ns (Layout)
CMOS: 0.53ns   0.893ns (Layout)

For 8 bit:

CPL: 2.02ns 2.268ns (Layout)

From these above result we come to know that CPL 1 bit adder is faster than CMOS adder. For this reason we use this adder in the biquad filter design to get the minimum delay from the whole design and get a better performance.
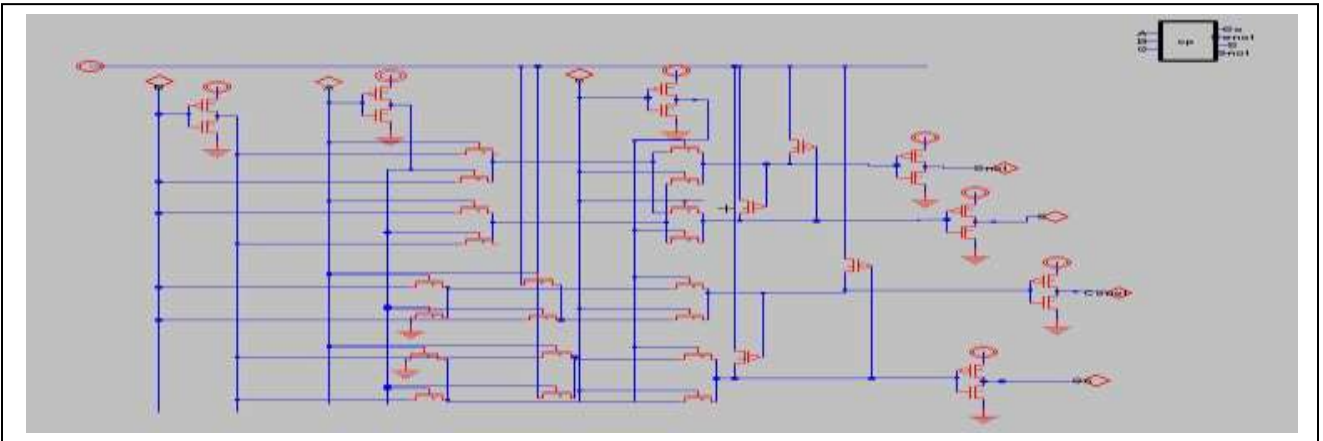
- **A. SCHEMATIC DIAGRAM**
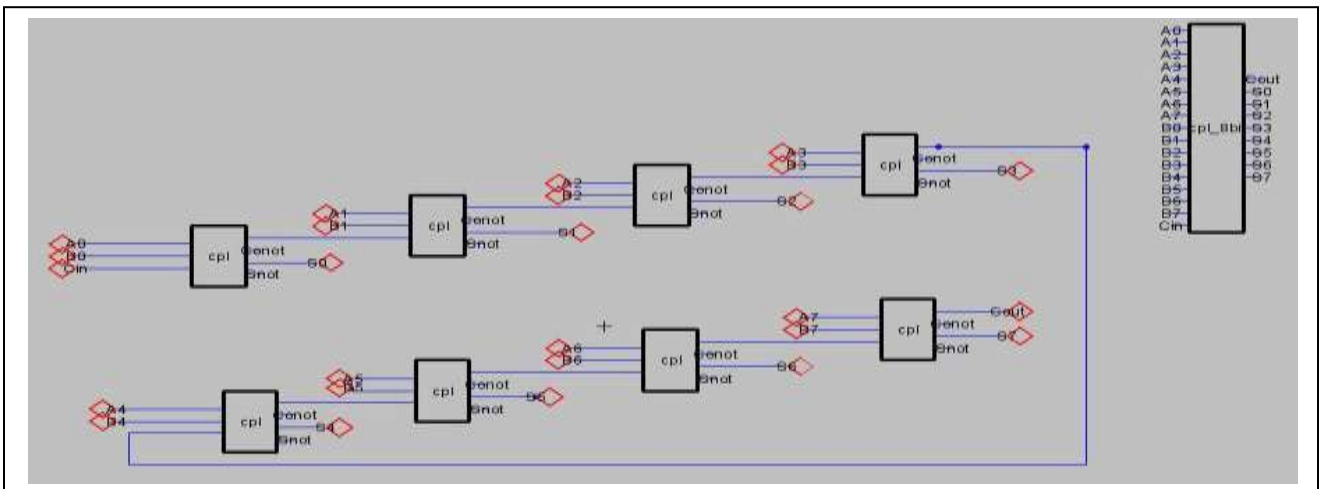
  - CMOS 1-bit Adder

Fig 2: CMOS 1 bit Adder (Schematic)

  - CPL 1-bit Adder

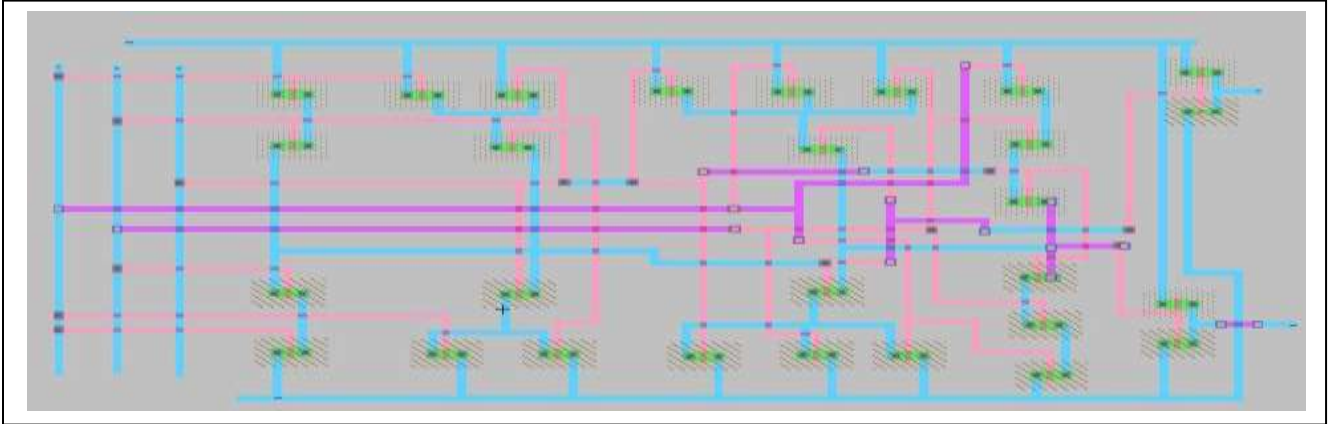**Fig 3: CPL 1 bit Adder (Schematic)**

  - CPL 8-bit Adder

Fig 4: CPL 8 bit adder (Schematic)
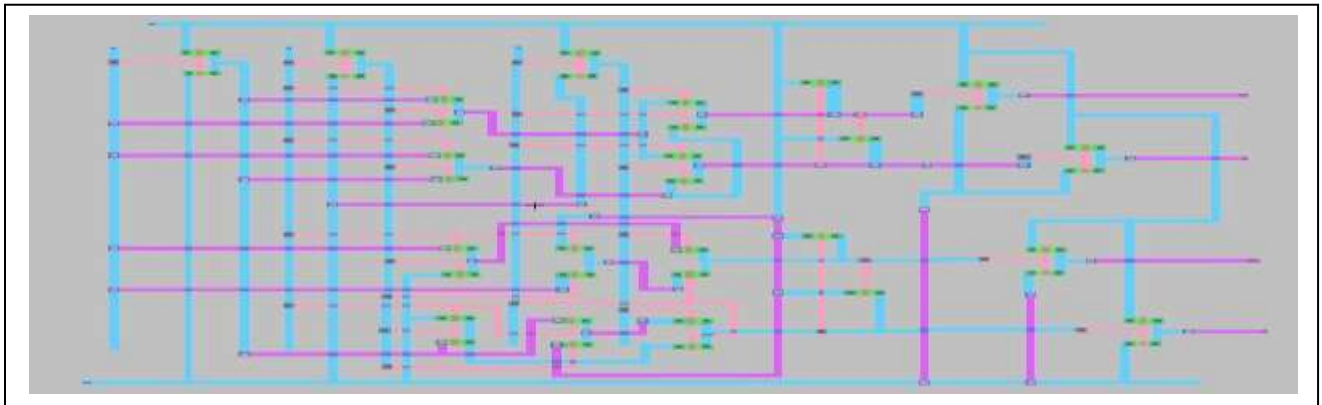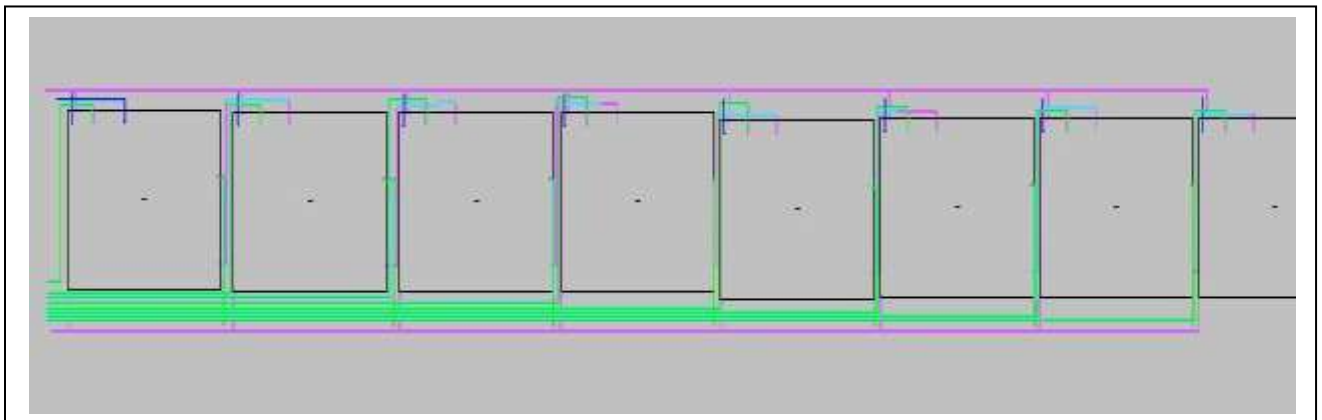
20

B. LAYOUT VIEW

- CMOS 1-bit Adder

Fig 5: CMOS 1 bit Adder (Layout)

- CPL 1-bit Adder

Fig 6: CPL 1 bit Adder (Layout)

- CPL 8-bit Adder

Fig 7: CPL 8 bit adder (Layout)
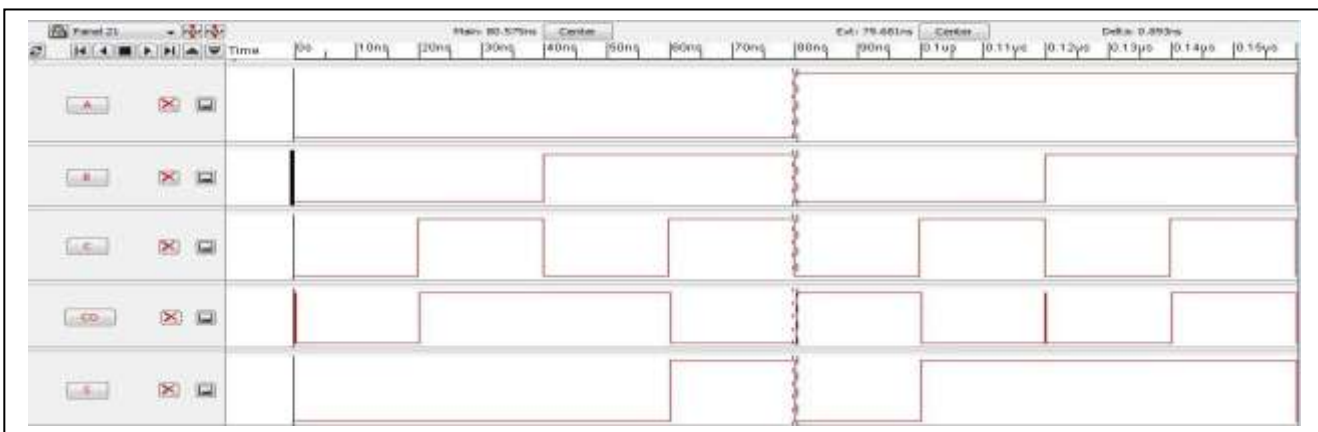
C. TIMING SIMULATION:

1) CMOS 1-bit Adder
   a. Schematic
      $\Delta d = 0.536$ns

Fig 8: Simulation of CMOS 1 bit Adder (Schematic)

   b. Layout
      $\Delta d = 0.893$ns

Fig 9: Simulation of CMOS 1 bit Adder (Layout)

2) CPL 1-bit Adder
   a. Schematic
      $\Delta d = 0.179$ns

Fig 10: Simulation of CPL 1 bit Adder (Schematic)

b. Layout
$\Delta d = 0.537ns$

Fig 11: Simulation of CPL 1 bit Adder (Layout)

3) CPL 8-bit Adder
   a. Schematic
      $\Delta d = 2.024ns$
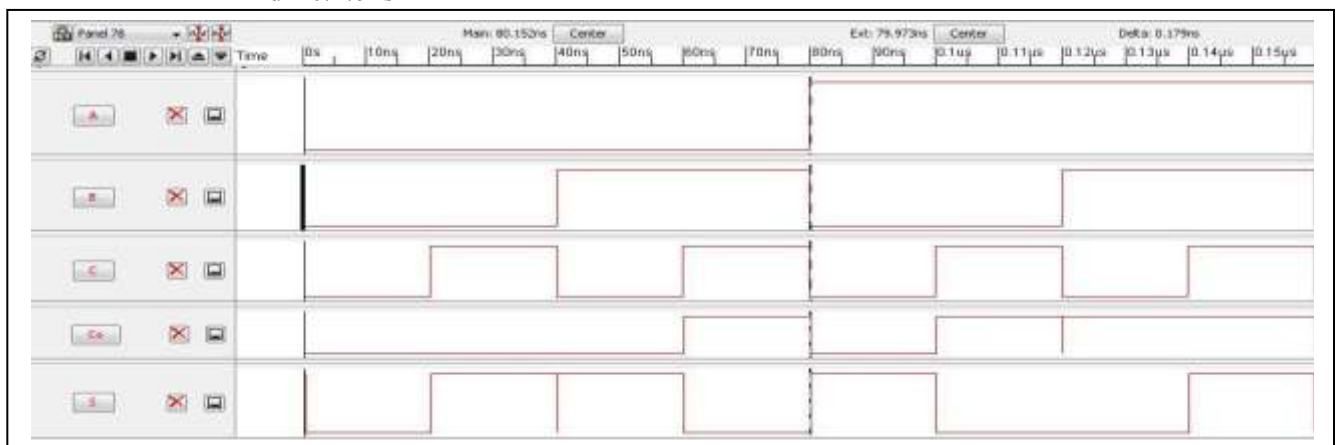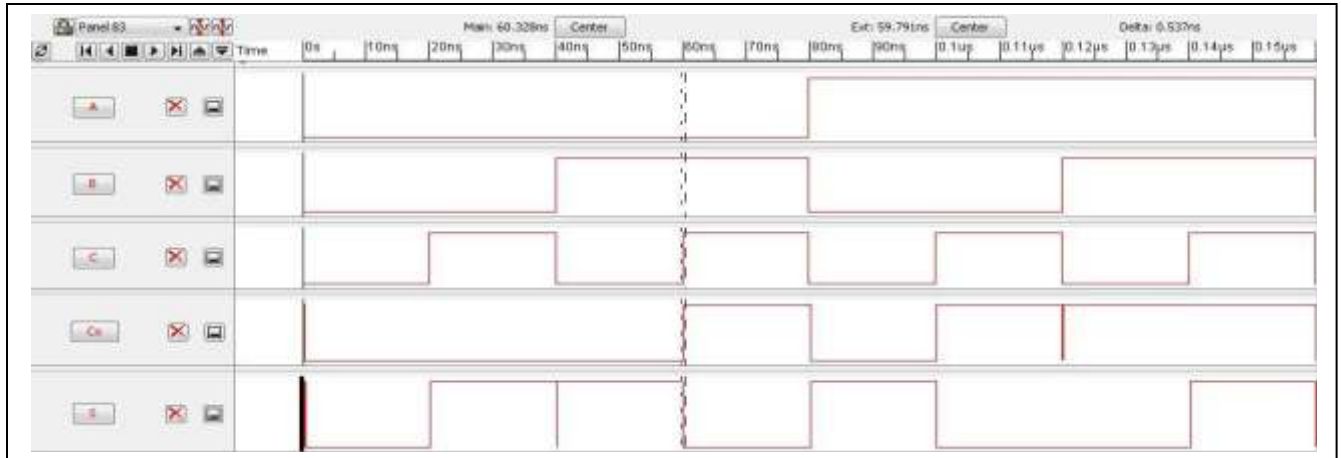

Fig 12: Simulation of CPL 8 bit adder (Schematic)

b. Layout
$\Delta d = 2.268ns$

Fig 13: Simulation of CPL 8 bit adder (Layout)

4. OUTPUT

TABLE 1: 8 BIT FULL ADDER

A0	A1	A2	A3	A4	A5	A6	A7	B0	B1	B2	B3	B4	B5	B6	B7	Cin	S0	S1	S2	S3	S4	S5	S6	S7	Cout
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

5. CONCLUSION

For full adder cell design, pass-logic circuit is thought to be dissipating minimal power and have smaller area because it uses less number of transistors. Thus, CPL adder is considered to be able to perform better than C-CMOS adder. Based on the SPICE net list generated for all modules were compared and found similarity for both schematic and layout. The same goes for the timing simulation ran using Build-in IRSIM. The delay found for the layout greater than the schematic but still in the acceptable range. Below are tables of delay observed:

TABLE 2: TIME DELAY

Modules	Delays	
	Schematic	**Layout**
1-bit CMOS Adder	0.536ns	0.893ns
1-bit CPL Adder	0.179ns	0.537ns

ACKNOWLEDGEMENT

REFERENCE

[1] S. Wairya, R. K. Nagaria, S. Tiwari, "New Design Methodologies for High-Speed Mixed Mode Cmos Full Adder Circuits" International Journal of VLSI Design & Communication Systems, Vol. 2, No. 2, pp. 78-98, June 2011.

[2] S. Wairya, R. K. Nagaria, S. Tiwari, S. Pandey, "Ultra Low Voltage High Speed 1-Bit CMOS Adder", IEEE Conference on Power, Control and Embedded Systems (ICPCES), pp.1-6, December 2010.

[3] R. Zimmermann, W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", IEEE Journal of Solid-State Circuits, Vol. 32, No.7, pp. 1-12, July 1997.

[4] Fordham University, "The Binary Adder", Fordham College Lincoln Center, Spring, 2011