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SNM Analysis of Sram Cells at 45nm, 32nm and 22nm Technology

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Abstract: High Read and Write Noise Margin is one of the important challenges of SRAM design. This paper analyzes the read stability and write ability of 6T and 7T SRAM cell structures at different technologies. SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation and SNM affects both read and write margin. This paper represents the simulation of both SRAM cells and their comparative analysis on the basis of RNM and WNM. The 7T SRAM cell provide higher read and write noise margin as compared to 6T SRAM cell at different technologies. All simulations of SRAM cells have been carried out on 45nm, 32nm and 22nm CMOS technology at Tanner EDA tool.

Keywords: 6T Memory, 7T Memory, Static Noise Margin (SNM), read stability, read noise margin (RNM), write noise margin (WNM)

1. INTRODUCTION

Static random access memory (SRAM) is a type of semiconductor memory that uses bistable circuitry to store each bit. The memory circuit is said to be static if the stored data can be retained indefinitely (as long as sufficient power supply voltage is provided), without any need for a periodic refresh operation An SRAM (Static Random Access Memory) is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. The second driving force for SRAM technology is low power applications. Figure 1 shows a typical PC microprocessor memory configuration [2].

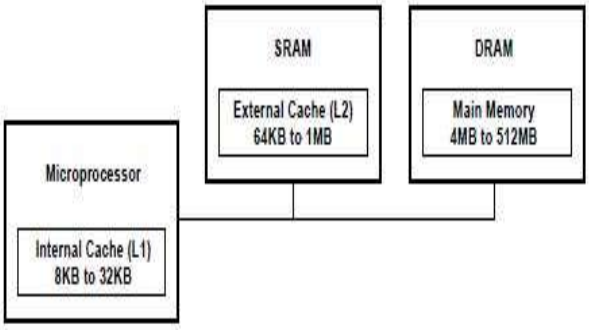

Figure 1 Typical PC Microprocessor Memory Configuration

2. LITERATURE REVIEW OF SRAM CELLS

2.1.6T SRAM CELL

Figure 2 shows the Schematic of 6T SRAM cell. This SRAM cell is composed of six transistor; four transistors (Q1 – Q4) comprise two cross coupled CMOS inverters plus two NMOS transistors (Q5 and Q6) for access. This configuration is called a 6T cell. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote either 0 or 1. Two access transistors (Q5 and Q6) serve to control the access to a storage cell during read and write operations. Access to cell is enabled by the word line (WL in Figure 2) which controls the two access transistors which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and QB. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD. A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low voltage operation.

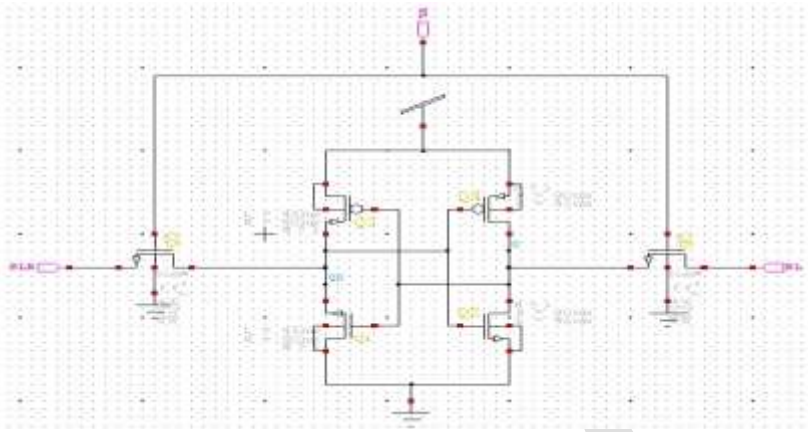

Figure 2 Schematic of 6T SRAM Cell

i. Write Operation

The write operation is similar to a reset operation of an SR latch. The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we apply a 0 to the bitlines, i.e. setting BL to 0 and BLB to 1. Similarly, a 1 is written by inverting the values of the bitlines, i.e. setting BL to 1 and BLB to 0.WL is then asserted and the value that is to be stored in latch in. Suppose we want to write 1 to this SRAM cell, we apply a 1 to BL, 0 at BLB and the word lines (WL) is VDD. At the same time, WL is turned ON; current is flowing from bit lines to the storage nodes (Q and QB). At the same time, transistor Q4 is turned ON as soon as the potential at the inverse storage node (QB), current will flow from VDD to the node and transistor Q1 is turned ON as soon as the potential at storage node (Q), current will flow to inverse node to ground. Figure 3 shows the simplified model of a 6T CMOS SRAM cell for write 1. In this case, transistor Q5 has to be stronger than transistor Q4 to change its state. The transistor Q4 is a PMOS transistor and inherently weaker than the NMOS transistor Q5 (the mobility of NMOS is higher than the mobility of PMOS). Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation [5].

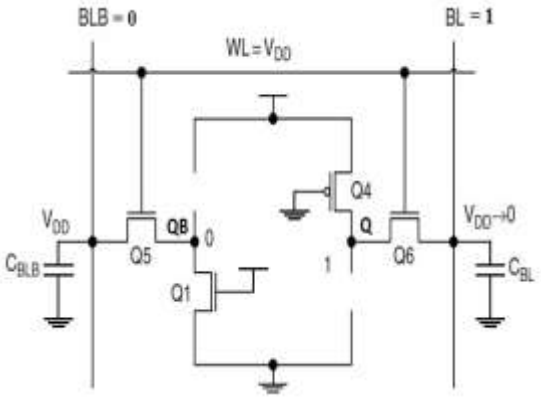

Figure 3 Simplified model of a 6T CMOS SRAM cell during for write 1

ii. Read Operation

Assume that the content of the memory is a 1; stored at Q. Figure 4 shows the simplified model of a 6T CMOS SRAM cell to read 1. The read cycle is started by precharging both the bit lines (BL and BLB) to logical 1, then asserting the word line WL, enabling both the access transistors (Q5 and Q6). Upon read access, the bit line voltage V_{BL} remains at precharge level. And the complementary bit lines voltage V_{BLB} is discharged through transistors Q1 and Q5 to logical 0 (i.e. eventually discharging through the transistor Q1 as it is turned on because the Q is logically set to 1) connected in series. On the BL side, the transistors Q4 and Q6 pull the bit line towards VDD, a logical 1 (i.e. eventually being charged by the transistor Q4 as it is turned on because Q is logical set to 0). Then these BL and BLB will have a small difference of delta between them and then these reach a sense amplifier, which will sense which line has higher voltage and thus will tell 1 was stored. If the sensitivity of the sense amplifier, the speed of read operation is faster. Similarly, if the content of the memory was a 0, the opposite would happen and BLB would be towards 1 and BL towards 0 [5].

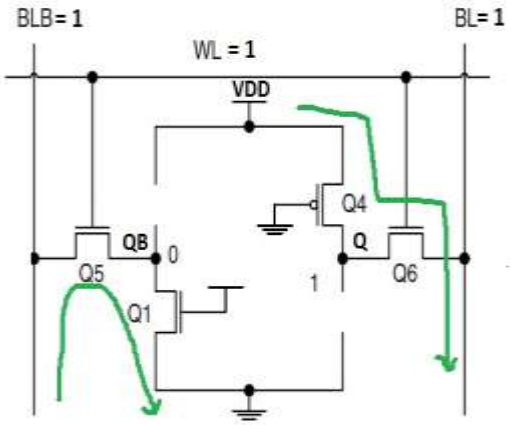

Figure 4 Simplified model of a 6T CMOS SRAM cell during to read 1

2.2.7T SRAM CELL

The circuit of 7T SRAM cell consists of two CMOS inverters (Q1-Q4) that connected to the cross coupled to each other with additional NMOS transistor (Q7) which connected to write line (w) and having two access NMOS transistors (Q5 and Q6) connected to bit lines (BL) and bit lines bar (BLB) respectively. Figure 5 shows Schematic of 7T SRAM Cell, where the access transistor Q5 is connected to the word line (WL) to perform the access write and Q6 is connected to the read line (R) to perform the read operations. Bit lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write in the memory cells during write operations. The proposed 7T SRAM cell depends on cutting off the feedback connection between the two inverters, inv1 and inv2, before a write operation. The feedback connection and disconnection is performed by an extra NMOS transistor Q7 and the cell only depends on BLB to perform a write operation [7].

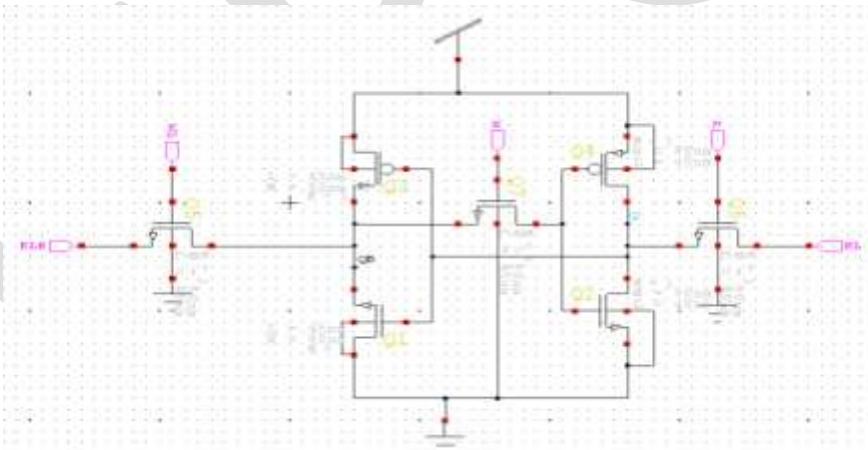

Figure 5 Schematic of 7T SRAM Cell

i. Write Operation

The write operation of 7T SRAM cell starts by turning transistor Q7 off, this cut off the feedback connection. BLB carries complement of the input data, Q5 is turned ON, while is Q6 off. This type of 7T SRAM cell looks like two cascaded inverters connected in series, inv2 followed by inv1, access transistor Q5 transfers the data from BLB to which drives inv2, Q1 and Q3, to develop Q, the cell data. Similarly, Q drives inv1, Q2 and Q4, to develop QB. Then, the word line (WL) is turned off and transistor Q7 is turned ON to reconnect the feedback connection between the two inverters to stably store the new data.

ii. Read Operation

In the read operation of 7T SRAM cell, both word line (WL) and read signal R are turned on, while transistor Q7 is kept ON. When Q = 0, the read path consists of transistor Q1 and Q6 and it behaves like a conventional 6T cell. When Q = 1, the read path consists of

transistor Q2, Q7 and Q5, which represents a read path. In this, the three transistors are connected in series, which reduces the driving capability of the cell unless these transistors are carefully sized.

3. STATIC NOISE MARGIN

The stability of SRAM circuits depends on the static noise margin. There are two methods to measure the SNM of SRAM cell. First method is a graphical approach in which SNM can be obtained by drawing and mirroring the inverter characteristics and then finding the maximum possible square between them. Figure 6 shows the standard setup of SNM. The second approach involves the use of noise source voltages at the nodes.

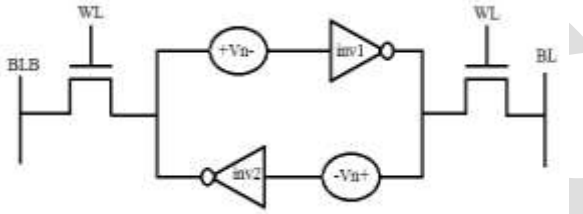

Figure 6 The standard setup for SNM

In a graphical technique, Plot the Voltage Transfer Characteristic (VTC) of Inverter 2 (inv2) and inverse VTC 1 from Inverter 1 (inv1). The resulting two lobed curves are called a "butterfly curve" and are used to determine the SNM. Figure 7 shows the general SNM characteristics during Standby. The SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve [6].

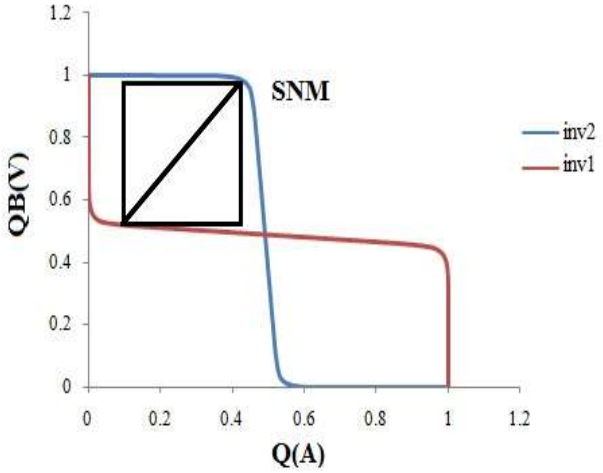

Figure 7 General SNM characteristics during Standby

SNM calculation: We have done the SNM calculation by this way with respect to above butterfly curve:
SNM = 'Maximum Side of the square'.
Maximum side of the Square = Maximum lengths of diagonal of Square / √ 2.
So, SNM = Maximum length of diagonal of square / √ 2.

i. Read Noise Margin

The cell is most vulnerable when accessed during a read operation because it must retain its state in the presence of the bit line precharge voltage. If the cell is not designed properly, it may change its state during a read cycle which results in either a wrong data being or a destructive read where the cell changes state. Thus, the worst noise obtained during access. Figure 8 shows VTC curve for RSNM characteristics. During write operation, the situation is reversed; the requirement is to switch the content of Q and Q' easily. Read margin (RM) is calculated based on transistor current model. The read margin defines the read stability of the SRAM cell.

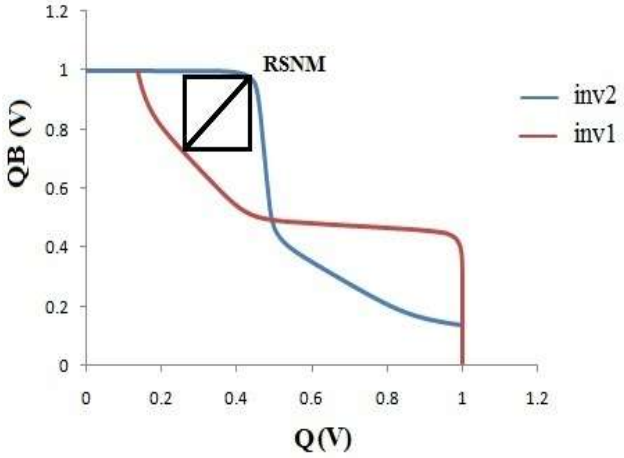

Figure 8 VTC curve for RSNM characteristics

ii. Write Noise Margin

The write noise margin is defined as the minimum bit line needed to flip the state of cell. The value of the write margin depends on the cell design, SRAM array size and process variation. Write SNM (WSNM) is measured using butterfly or VTC curves as shown in Figure 9, which are obtained from a dc simulation sweeping the input of inverters (QB and Q). WSNM for writing '1' is the width of the smallest square that can be embedded between the lower right half of the curves. WSNM for writing '0' can be obtained from a similar simulation.

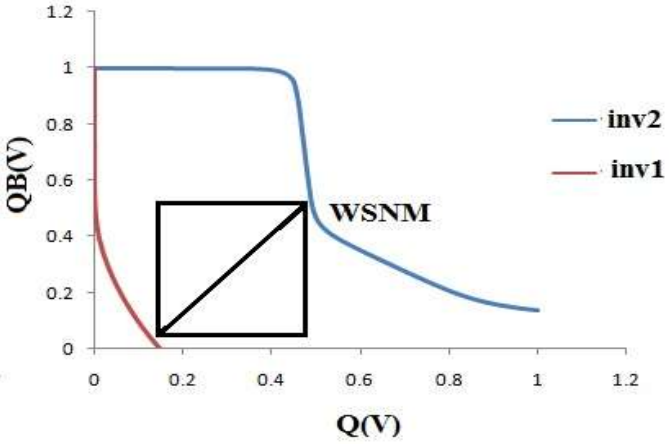

Figure 9 VTC curve for WSNM characteristics (writing 0)

4. SIMULATION AND RESULTS

Table 1-3 presents the static noise margin of 6T and 7T SRAM cell at 45nm, 32nm and 16nm technology. Results show that RSNM and WSNM of 7T SRAM cell has higher than 6T SRAM cell. In Figure 10-12, the profiles of the Read and Write Margin for both cells are shown at different technologies. To make the impartial testing environment all the circuits has been simulated on the sane input patterns. All the circuits have been simulated in 45nm, 32nm and 22nm technology on Tanner EDA tool with supply voltage 1v.

i. AT 45nm TECHNOLOGY

Table 1 Static Noise Margin of SRAM Cells at 45nm

SRAM CELLS	READ SNM (mV)	WRITE SNM (mV)
6T	170.97	282.84
7T	206.56	301.72

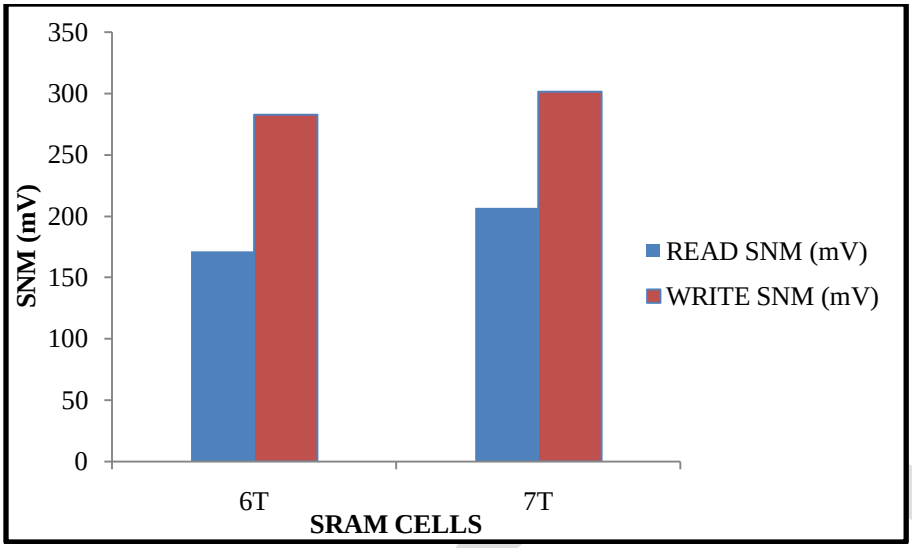

Figure 10 Calculation of SNM at 45nm technology

ii. AT 32nm TECHNOLOGY

Table 1 Static Noise Margin of SRAM Cells at 32nm

SRAM CELLS	READ SNM (mV)	WRITE SNM (mV)
6T	153.21	268.70
7T	202.71	290.49

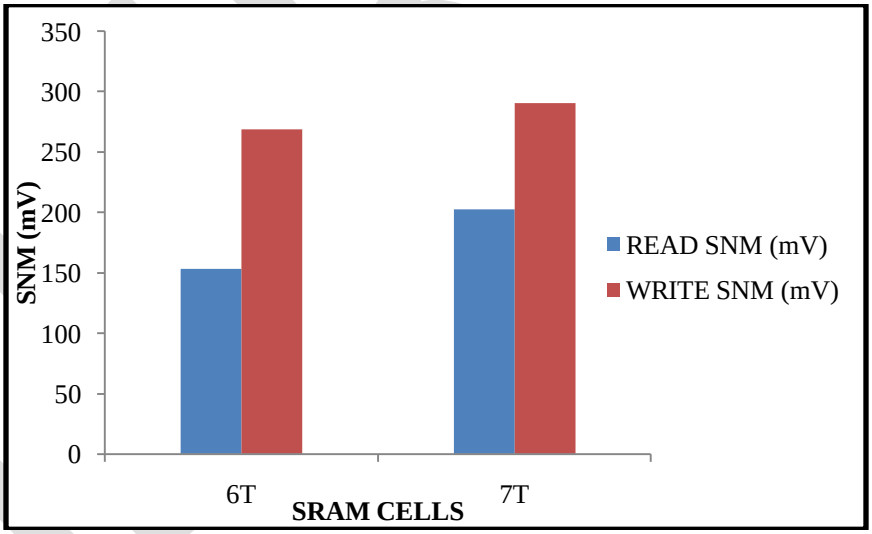

Figure 11 Calculation of SNM at 32nm technology

iii. AT 22nm TECHNOLOGY

Table 1 Static Noise Margin of SRAM Cells at 22nm

SRAM CELLS	READ SNM (mV)	WRITE SNM (mV)
6T	145.32	261.62
7T	180.67	270.97

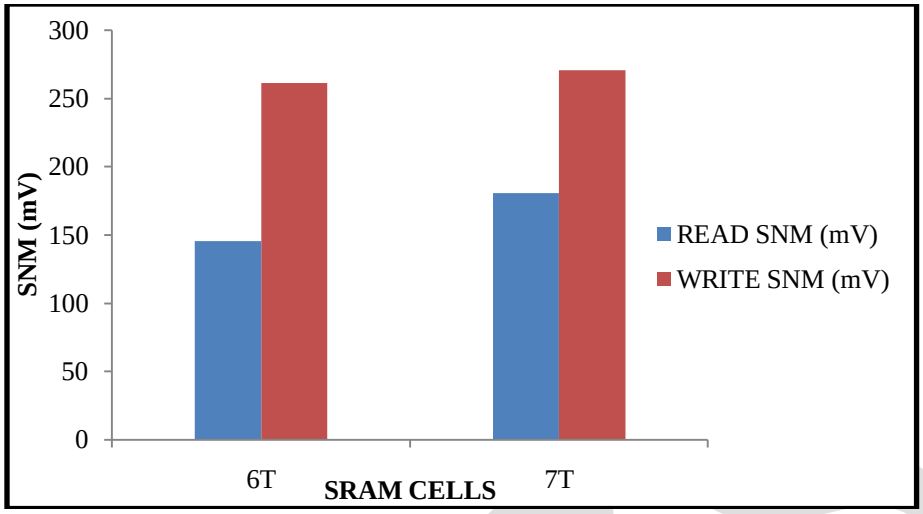

Figure 12 Calculation of SNM at 22nm technology

5. CONCLUSIONS

In this paper, stability analyses of 6T and 7T SRAM cell topologies have been presented. The 6T SRAM cell provides very less RNM and WNM. The 7T SRAM cell provide higher read and write noise margin as compared to 6T SRAM cell at different technologies. The main reason of read and write stability improvement in 7T SRAM cell is that it depends on cutting off the feedback connection between the two inverters, inv1 and inv2, before a write operation. The feedback connection and disconnection is performed by an extra NMOS transistor and the cell only depends on BLB to perform a write operation. All the above figures depict that 7T SRAM cell at 45nm, 32nm and 22nm technology shows better read and write stability than conventional 6T SRAM cell. This paper tries to find out an efficient SRAM memory cell with higher read and write stability at different technologies.

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