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Design of Low Area and Low Power Modified 32-BIT Square Root Carry Select Adder

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Abstract-In digital circuitry, a compact and fast adder is required to carry out computations in large chips.
Carry Select Adder (CSLA) is one of the fast adders used in many data-processing processors to perform fast arithmetic functions. Although carry select adder is slower than carry look-ahead adder but area is lesser. From the structure of the CSLA, there is scope for reducing the area and power consumption in the CSLA. The thesis uses a simple and efficient gate -level modification to significantly reduce the area and power of the CSLA. Based on this modification 32-bit square-root CSLA (SQRT CSLA) architecture has been developed and compared with the 32-bit conventional SQRT CSLA architecture.

The modification is the use of Binary-To-Excess-1Converter logic instead of the chain of full adder when carry is 1.This logic has less number of gates as compared to the design without using binary to excess 1 converter logic. The design is checked on Modelsim 6.4 (a) and synthesized on Xilinx ISE design suite 14.3.The power is calculated on Xilinx Power Estimator tool. The area comparison is done in respect of LUTs .Proposed design has reduced area and power as compared with the conventional SQRT CSLA with only a slight increase in the delay. The thesis evaluates the performance of the design in terms of area and power. The result analysis shows that the modified SQRT CSLA structure is quantitatively superior over conventional SQRT CSLA in terms of area and power.

Keywords- SQRT CSLA, Modified CSLA, BEC-1, RCA, XILINX ISE Design Suite 14.3, Verilog, VLSI, Modelsim 6.4 a. XILINX Power Estimator.

INTRODUCTION

In today's digital circuitry, an adder in the data path is required which consumes less area and power with comparable speed. Carry select adder has less area than carry look-ahead adder but it is slower than carry look-ahead adder. Carry select adder requires more area and consumes more power as compared to ripple carry adder but offers good speed. Adders in circuits or systems acquire huge area and consume large power as large additions are done in advanced processors and systems. Adder is one of the key hardware blocks in Arithmetic and logic unit (ALU) and digital signal processing (DSP) systems. The DSP applications where an adder plays an important role include convolution, digital filtering like in Discrete Fourier transform (DFT) and Fast Fourier Transform (FFT), digital communications and spectral analysis. The performance depends on the power consumed while addition operation [2][3].

There is a need in the VLSI market for the low area and low power consumption adders. So, a modified adder is needed. A new adder i.e., SQRT CSLA is used in many digital systems, here independently generating multiple carries and then selects a carry to generate the sum. Although the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers as proposed by O.bedriji [1].
The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5][6].The purpose of having low area and power is solved by using Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the conventional CSLA to achieve lower area and power consumption. The advantage of BEC-1 logic is the lesser number of logic gates than the n-bit Full Adder (FA) structure. Due to less logic gates used in BEC, there will be less power consumption. The SQRT CSLA has been chosen for comparison with the conventional design as it has a more balanced delay, and requires lower power and area.

Section II deals with the various types of adders and the delay area calculation methodology in carry select adder with BEC-1 being used. Section III describes area analysis before and after modification done in adder. Section IV deals with results and their

comparison of 32 – bit conventional square root carry select adder with the modified square root carry select adder. Section V describes the simulation and synthesis results of both architectures. Section VI is the conclusion.

CARRY SELECT ADDER

Internal architecture of 4 bit carry select adder:-

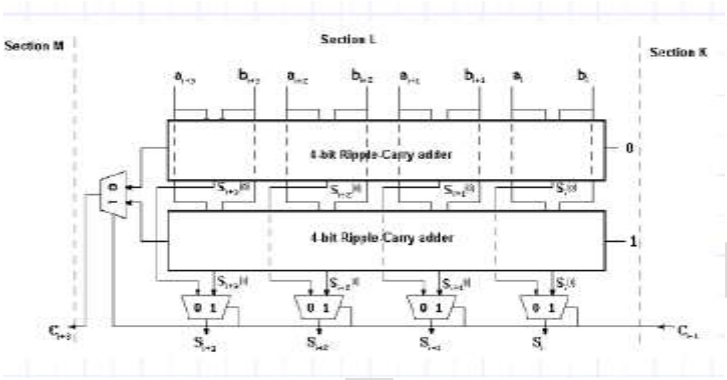

Figure 1: 4-bit Carry select adder

In the fig 1 following are the operations done:

- Two ripple carry adder chains are used in parallel to calculate sum for carry 0 and carry1.
- Previous carry will select the carry in of next stage and thus sum is calculated. Next stage depends on previous carry so carry propagation is serially.

Delay and Area Evaluation Methodology of the Basic Adder Blocks

The AND, OR and Inverter (AOI) implementation of an XOR gate is shown in Fig 2. The gates between the dotted lines are doing the operations in parallel and the numeric representation of each gate indicates the delay contributed by the gate. The delay and area evaluation considers all gates to be made up of AND, OR, and Inverter, each having delay of 1 unit and area equal to 1 unit.

We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. An area evaluation is done by counting the total number of AOI gates required for each logic block. The CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table 1

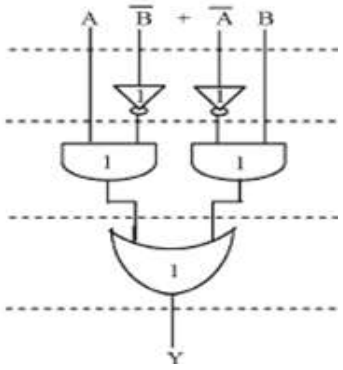

Figure 2: Delay and Area evaluation of an XOR gate

Table 1
Delay and Area count of the basic blocks of adder

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

BINARY TO EXCESS-1 CONVERSION TECHNIQUE

As stated above the main idea of this work is to use BEC-1(Binary to Excess-1 Converter) instead of the RCA with Cin=1 in order to reduce the area and power consumption of the conventional CSLA. To replace the n-bit RCA, an n+1bit BEC-1 is required. The structure and the functional table of a 4-bit BEC-1 are shown in Fig3 and Table2 respectively.

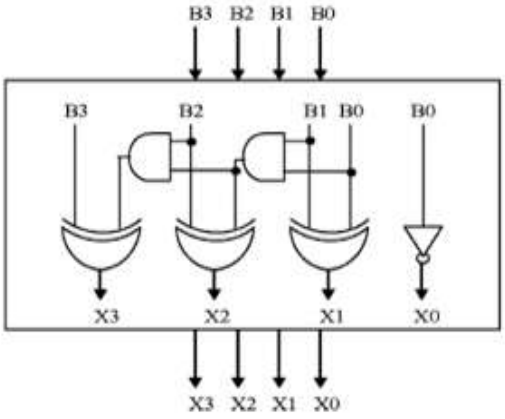

Figure 3: 4-bit BEC-1circuit

Table 2
Functional table of 4-bit BEC-1

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

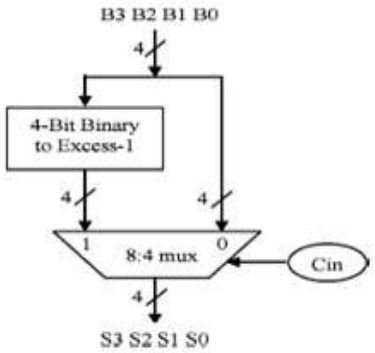

Figure 4: 4-bit BEC-1 with 8:4 Mux

Fig 4 describes how the basic function of the CSLA is obtained by using the 4-bit BEC-1 together with the mux. Inputs of the 8:4 mux are (B_3, B_2, B_1, and B_0) or input of the mux is the BEC-1 output. This produces the two possible partial results in parallel and the mux is used to select either the BEC-1 output or the inputs according to the control signal Cin. The importance of the BEC-1 logic results the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC-1 is listed as (note the functional symbols ~NOT, &AND, ^XOR).

$X0 = \sim B0$
$X1 = B0 \wedge B1$
$X2 = B2 \wedge (B0 \,\&\, B1)$
$X3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2)$

DELAY AND AREA EVALUATION OF CONVENTIONAL 32-BIT SQRT CSLA

The structure of the 32-b conventional SQRT CSLA is shown in Fig 5. It has 4 groups of different sizes RCA and 9 stages. The delay and area evaluation of each group are shown in Fig 6, in which the numerals within [ ] shows the delay values.

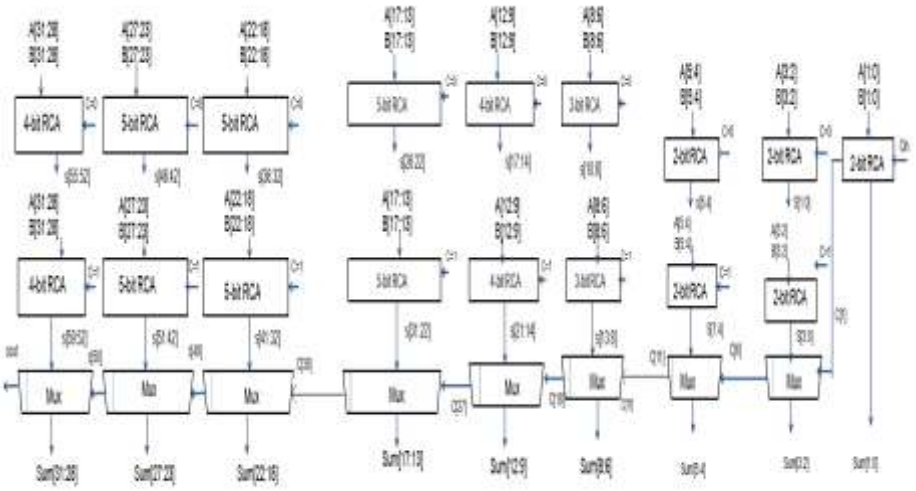

Figure 4: Structure of 32-bit conventional SQRT CSLA

Here second and third stage has group 2 which has 57 logic gates each. Fourth stage has group 3.Fifth and ninth stage has group 4 and sixth, seventh and eighth has group 5.Area evaluation of each group is same as mentioned in the case of 8 bit, but total area is different. The steps leading to the evaluation are as follows:

1) The group2 [see Fig 6(a)] has two sets of 2-b RCA. Depends on the consideration of delay values, the incoming time of selection input c1 [time (t) = 7] of 6:3 mux is earlier than s3 [t = 8] and later than s2 [t = 6]. Thus, sum3 [t = 11] is addition of s3 and mux [t = 3] and sum2 [t = 10].

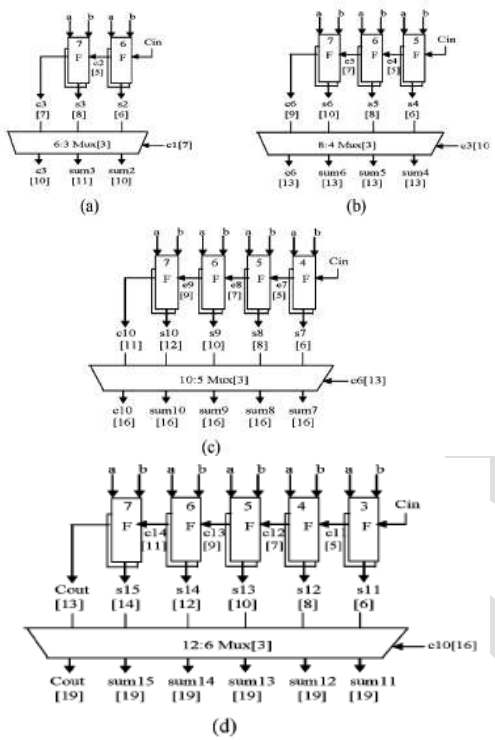

Figure 6: Delay and Area Evaluation of conventional 32-bit SQRT CSLA: (a) Group2, (b) Group3, (c) Group4, and (d) Group5. F is a Full Adder

2) Except for group2, the incoming time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:

$$\{c6, \text{sum}\,[06:04]\} = c03\,[t = 10] + \text{mux}$$
$$\{c10, \text{sum}\,[10:07]\} = c06\,[t = 13] + \text{mux}$$
$$\{\text{Cout}, \text{sum}\,[15:11]\} = c10\,[t = 16] + \text{mux}$$

3) The one set of 2-b RCA in group2 has 2 FA for Cin = 1 and the other set has 1 FA and 1 HA for Cin = 0. Based on the area count, the total number of gate counts in group2 is determined as follows:

$$\text{Gate count} = 57(\text{FA} + \text{HA} + \text{Mux})$$
$$\text{FA} = 39(3 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{Mux} = 12(3 * 4)$$

Similarly for group 4

$$\text{Gate count} = 117(\text{FA}+\text{HA}+\text{MUX})$$
$$\text{FA}=91(7*13)$$
$$\text{HA}=6(1*6)$$
$$\text{MUX}=20(5*4)$$

4) Similarly, the approximate maximum delay and area of the other groups in the conventional SQRTCSLA are evaluated and listed in table 3.

Table 3
Delay and Area count of groups of conventional SQRT CSLA

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

Total gate count for conventional 32-bit sqrt Csla is 833.

PROPOSED DESIGN

Delay and Area Evaluation of Modified 32-bit SQRT CSLA

The structure of the proposed 32-bit SQRT CSLA using BEC-1 for RCA with Cin=1 to optimize the area and power is shown in Fig 8. We again divide the structure into four groups. The delay and area estimation of each group are shown in Fig 8. The group2 [see Fig 8(a)] has one 2-bit RCA which has 1 FA and 1 HA for Cin=0. Instead of another 2-bit RCA with Cin=1 a 3-bit BEC-1 is used which adds one to the output from 2-bit RCA.

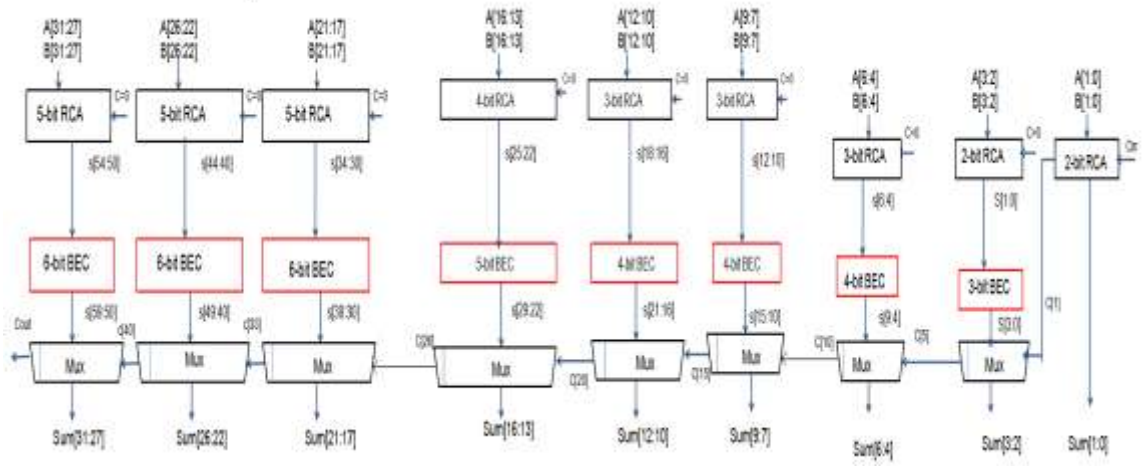

Figure 7: Structure of 32-bit modified SQRT carry select adder

The steps leading to the evaluation are:

1) The group2 [see Fig 8(a)] has one 2-bit RCA which has 1 FA and 1 HA for Cin= 0. Instead of another 2-bit RCA with Cin = 1 a 3-bit BEC is used which adds one to the output from 2-bit RCA. Depend on the consideration of delay values of table 2, the incoming time of selection input c1 [time (t) = 7] of 6:3 mux is earlier than the s3 [t = 9] and c3 [t = 13] and later than the s2 [t = 4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

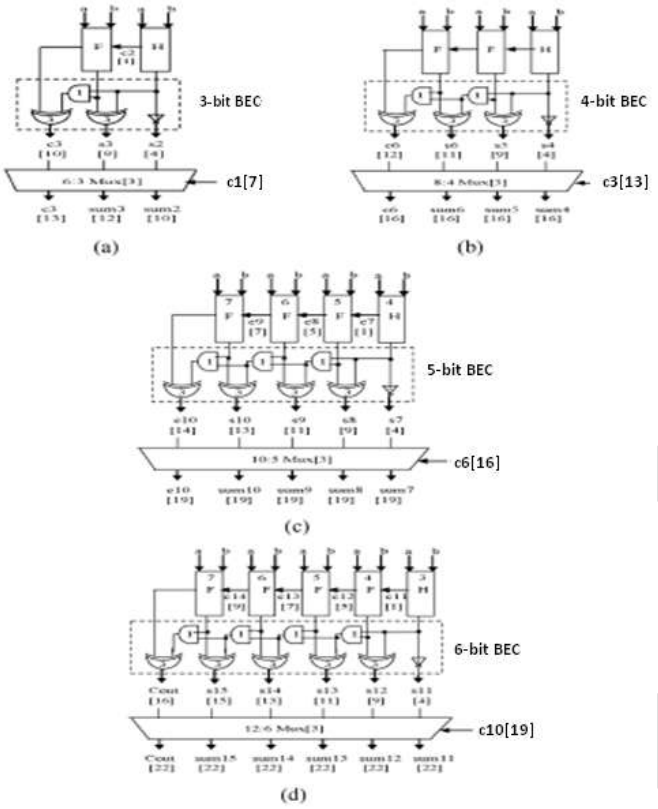

Figure 8: Delay and Area Evaluation of modified 8-bit SQRT CSLA: (a) Group 2 (b) Group 3 (c) Group 4 (d) Group5. H is a half adder

2) For the remaining group's the incoming time of mux selection input is always greater than the incoming time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the incoming time of mux selection input and the mux delay. The area count of group 2 is:

$$\text{Gate count} = 43(\text{FA} + \text{HA} + \text{Mux} + \text{BEC})$$
$$\text{FA} = 13(1 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{AND} = 1$$
$$\text{NOT} = 1$$
$$\text{XOR} = 10(2 * 5)$$
$$\text{Mux} = 12(3 * 4)$$

Similarly for group 4

$$\text{Gate count} = 84(\text{FA}+\text{HA}+\text{MUX}+\text{BEC})$$
$$\text{FA}=39(3*13)$$
$$\text{HA}=6(1*6)$$
$$\text{MUX}=20(5*4)$$
$$\text{XOR}=5(1*5)$$
$$\text{AND}=6(6*1)$$
$$\text{OR}=3(3*1)$$
$$\text{NOT}=4(4*1)$$

Total gate count is 674.We can see here that area is minimized by 833-674=159, i.e. 159 times less area overhead. Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in table 4.

Table 4

Delay and Area count of groups of modified SQRT CSLA

Group	Delay	Area
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

RESULTS AND COMPARISON

We have simulated our design using ModelSim-Altera 6.4a. Coding is done using Verilog. The simulation results of 4-bit, 8-bit and 32-bit adders are shown in Figure 9, Figure 10, and Figure 11 respectively. We have synthesized our designs using Xilinx ISE suite 14.3 and obtained the power using Xilinx Power Estimator, the results are shown in Table 5. For 4-bit and 8 bit design we have used Spartan 3E XC3S100E and for 32-bit Spartan 6 is used.

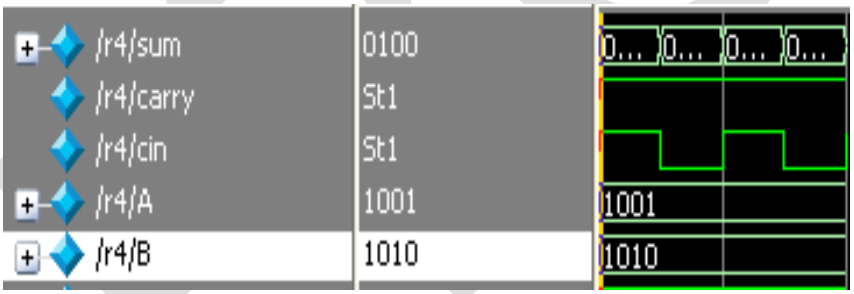

Figure 9: Simulation result of 4-bit modified SQRT CSLA

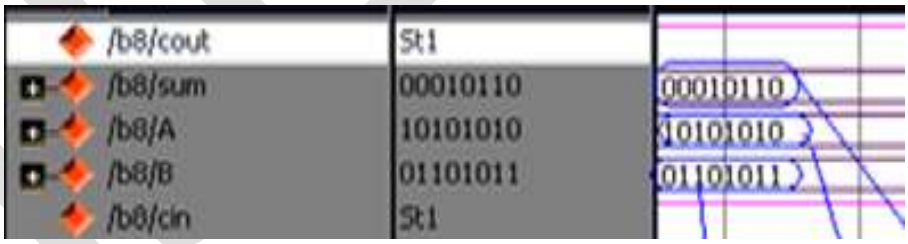

Figure 10: Simulation result of 8-bit modified SQRT CSLA

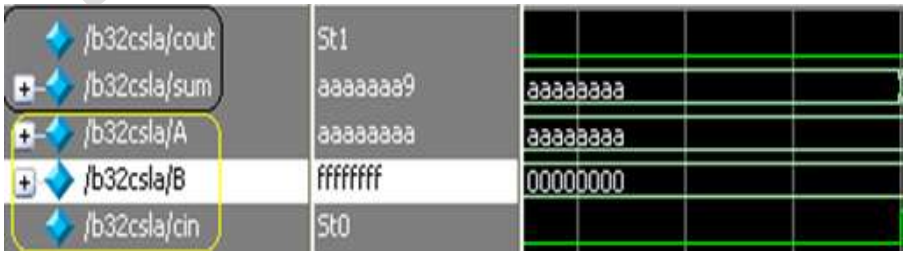

Figure 11: Simulation result of 32-bit modified SQRTCSLA

Table 5
Synthesis Result of Proposed Design

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	75	11,776	1%
Number of occupied Slices	46	5,388	1%
Number of Slices containing only related logic	46	46	100%
Number of Slices containing unrelated logic	0	46	0%
Total Number of 4 input LUTs	75	11,776	1%
Number of bonded IOBs	98	372	26%
Average Fanout of Non-Clock Nets	2.52		

We have compared the Modified results with conventional design. The results, as shown in Table 6, report that our adder design is compact than other conventional design. Its power is much less compared to the conventional 32-bit SQRT CSLA .

Table 6
Comparison of area of both the designs

Logic Utilization	Used (Conventional)	Used (Modified)	Available
No. of 4-input LUTs	89	75	11,776
No. of occupied slices	51	46	5,888
No. of bonded IOBs	98	98	372
Average Fan-out of Non-clock nets	2.19	2.52	

Power results are shown in fig 12 and 13 for Conventional and Modified design respectively.

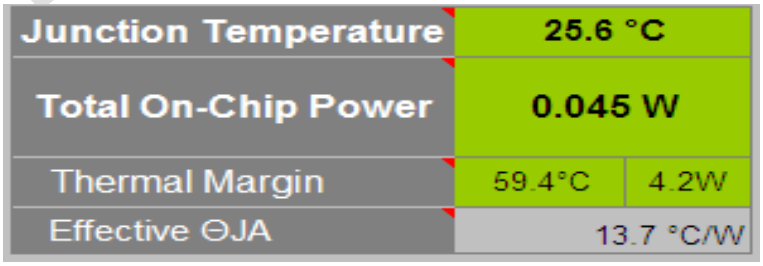

Figure 12: Power result of 32-bit Conventional SQRT CSLA

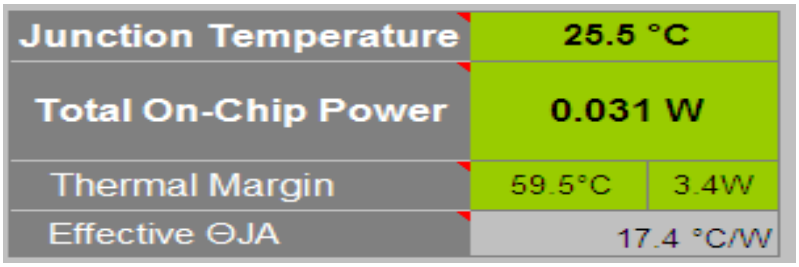

Figure 13: Power result of 32-bit Modified SQRT CSLA

CONCLUSIONS

The area and power is successfully reduced with the help of a method called as BEC-1 technique. With the help of Modelsim 6.4 a, outputs of conventional and the modified design has been checked and getting the correct and the same result. The working is same and modified design is correct. With the help of ISE Design Suite 14.3, design is synthesized and area report in terms of LUT's and slices are obtained. Modified 32-bit SQRT carry select adder is using 75 LUTs in comparison to Conventional SQRT carry select adder, which uses 89 LUTs. Modified 32-bit SQRT carry select adder is using 36 SLICES in comparison to Conventional SQRT carry select adder, which uses 51 SLICES. Modified 32-bit SQRT carry select adder consumes 0.031W as compared to 0.045W which is consumed by Conventional 32-bit Sqrt Csla.

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