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Design of Universal Shift Register Using Pulse Triggered Flip Flop

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ABSTRACT – Universal shift registers, as all other types of registers, are used in computers as memory elements. Flip-flops are an inherent building block in Universal shift registers design. In order to achieve Universal shift registers, that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops. Several fast low power flip flops, called pulse triggered flip flop (PTFF), design is analyzed and designed the universal shift registers.. The paper presents a modified design for explicit pulse triggered Flip-flop with reduced transistor count for low power and high performance applications. HSPICE simulation results of Shift Register at a frequency of 1GHz indicate improvement in power-delay product with respect to the Existing pulse triggered flip flop configurations using CMOS technology.

Keywords: MOSFET, Pulse triggered flip flop, universal shift registers, low power, delay, power delay product

INTRODUCTION

Flip Flops are the basic storage elements used in all types of digital circuit designs. Conventional master slave flip flops are made up of two stages and are characterized by hard edge property. But pulse triggered flip flops reduce the two stages into one stage and are characterized by soft edge property [10]. Nowadays Pulse triggered flip flops have been considered as an alternative to the conventional master-slave [7]. A pulse triggered flip flop consists of a pulse generator for strobe signal and a latch for data storage. Since the pulses are generated on the transition edges of the clock signals and very narrow pulse width, the latch acts like an edge triggered flip flop [3]. PTFF uses a conventional latch design clocked by a short pulse train and it also acts as a flip flop. Advantages of pulse triggered flip flop are that it is simpler in circuit complexity and leads to higher toggle rate for high speed operations and also allows time borrowing across cycle boundaries. To achieve low power in high speed regions, the different low power techniques are conditional capture, conditional precharge, conditional discharge, conditional data mapping and clocking gating technique [3]

EXISTING PULSE TRIGGERED FLIP FLOP

An explicit type pulse triggered structure and a modified true single phase clock latch based on a signal feed through scheme as shown in Fig 1

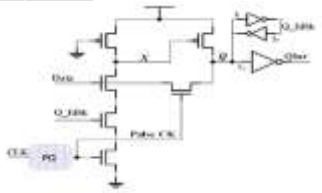

Fig 1 Existing pulse triggered flip flop

The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor and the delay can be greatly shortened.[3]

PROPOSED PULSE TRIGGERED FLIP FLOP

The proposed system is designed with signal feed through scheme without feedback circuits that is only capable of designing the sequential circuits that does not have feedback operation as shown in Fig.2. Added to the pass transistor in the existing system, a pMOS transistor is used controlled by clock signal to reduce power

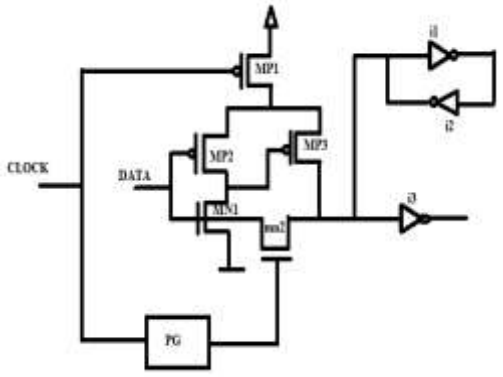

Fig 2 Proposed Pulse Triggered Flip Flop

UNIVERSAL SHIFT REGISTER

A universal shift register is an integrated logic circuit that can transfer data in three different modes designed using pulse triggered flip flop as shown in the Fig 3. Like a parallel register it can load and transmit data in parallel.Like shift registers it can load and transmit data in serial fashions, through left shifts or right shifts. In addition, the universal shift register can combine the capabilities of both parallel and shift registers to accomplish tasks that neither basic type of register can perform on its own.

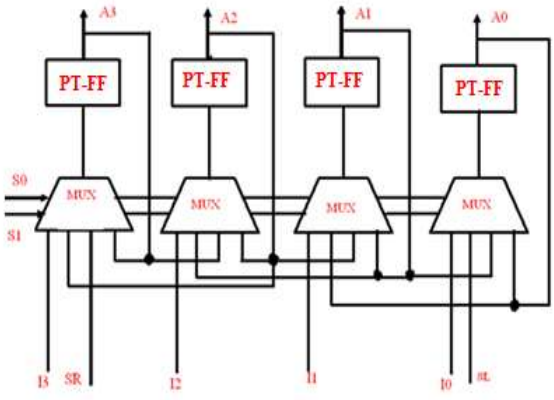

Fig 3: Universal Shift Register

For instance, on a particular job a universal register can load data in series and then transmit/output data in parallel. Universal shift registers, as all other types of registers, are used in computers as memory elements.[11] Although other types of memory devices are used for the efficient storage of very large volume of data, from a digital system perspective when we say computer memory we mean registers. In fact, all the operations in a digital system are performed on registers. Examples of such operations include multiplication, division, and data transfer. Due to increasing demand of battery operated portable handheld electronic devices like laptops, palmtops and wireless communication systems (personal digital assistants and personal communicators) the focus of the VLSI industry has been shifted towards low power and high performance circuits. Flip-flops and latches are the basic sequential elements used for realizing digital systems like Universal shift Register

PERFORMANCE ANALYSIS

In CMOS design, analysis of the average power, delay and power delay product of the ExistingPulse Triggered Flip Flop based universal shift register using 130nm technology is shown in Table.1.

Table 1 Universal Shift Register Using Existing Pulse Triggered Flip Flop In 130nm Technology

DESIGN	PULSE TRIGGERED FLIP FLOP		
	POWER (µW)	DELAY (ps)	POWER DELAY PRODUCT (fJ)
UNIVERSAL SHIFT REGISTER	684.4	113.70	77.816
		119.38	81.703
		119.09	81.505
		111.75	76.481

In CMOS design, analysis of average power, delay and power delay product of the Existing Pulse Triggered Flip Flop based Universal shift register using 22nm technology is shown in Table 2.

Table 2 Universal Shift Register Using Existing Pulse Triggered Flip Flop In 22nm Technology

DESIGN	PULSE TRIGGERED FLIP FLOP		
	POWER (µW)	DELAY (ps)	POWER DELAY PRODUCT (fJ)
UNIVERSAL SHIFT REGISTER	13.46	14.399	0.1938
		14.825	0.1995
		15.089	0.2030
		13.839	0.1862

In CMOS design, analysis of the average power, delay and power delay product of the existing Pulse Triggered Flip Flop based Universal shift register using 16nm technology is shown in Table 3.

Table 3 Universal Shift Register Using Existing Pulse Triggered Flip Flop In 16nm Technology

DESIGN	PULSE TRIGGERED FLIP FLOP		
	POWER (µW)	DELAY (ps)	POWER DELAY PRODUCT (fJ)
UNIVERSAL SHIFT REGISTER	6.473	10.699	0.0069
		12.012	0.0077
		13.416	0.0086
		12.239	0.0079

CONCLUSION

The pulse triggered flip flop based on signal feed through scheme is used to design universal shift registers. The universal shift registers are designed using existing and proposed pulse triggered flip flop using CMOS design with nanometer Technology to achieve low power, less delay and power delay product

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