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Comparative Analysis of Improved Domino Logic Based Techniques for VLSI Circuits

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ABSTRACT - In modern VLSI design, Domino logic based design technique is widely used and in which power ignites the speed of circuit. The Dynamic (Domino) logic circuit are often favored in high performance designs because of the high speed and low area advantage. But in integrated circuits, the power consumed by clocking gradually takes a dominant part, and therefore our research work in this paper is mainly focused on to study the comparative performance of various domino logic based techniques proposed recently in last decade viz. basic logic domino technique, domino with keeper, high speed leakage tolerant domino, low swing domino logic and domino logic with variable threshold voltage keeper, sleep switch dual threshold voltage domino.

This work evaluates the performance of the different domino techniques in terms of delay, power and their product on BSIM4 model using Agilent Advanced Design System tool. The domino techniques compared in this work were found to have optimized area, power, delay and hence better power delay product (PDP) as compared with standard domino.

The main focus of this research work is to find the best possible trade off that would optimize multiple goals viz. area, power, speed and noise immunity at the same time to meet the multi-objective goal for our future research work.

Keywords - Domino logic circuit, Domino logic with keeper, High speed and leakage Tolerant Domino, Low Swing Domino, Domino Logic with Variable Voltage Threshold Keeper, Sleep Switch Dual Threshold Voltage Domino.

INTRODUCTION

Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of dynamic CMOS circuits as compared to static CMOS circuits. High-speed operation of domino logic circuits is primarily due to the lower noise margins of domino circuits as compared to static gates [1,2]. Domino logic offers speed and area advantages over conventional static CMOS and is especially useful for implementing complex logic gates with large fan-outs. A limitation of the domino technique is that only non-inverting gates are possible. This limits the logic flexibility and implies that logic inversion has to be performed at the inputs or outputs of blocks of domino logic [2]. In this paper, we explored the various domino logic based techniques for combinational circuit design for high fan in and high speed application in deep submicron VLSI technology.

DOMINO LOGIC TECHNIQUES

A. Basic Domino Logic

Domino CMOS was proposed in 1982 by Krambeck. It has same structure as dynamic logic gates, but adds static buffering CMOS inverter to its output. The introduction of the static inverter has the additional advantage of the output having a low-impedance output, which increases noise immunity and drives the fan-out of the gate. The buffer furthermore reduces the capacitance of the dynamic output node by separating internal and load capacitance. The buffer itself can be optimized to drive the fan-out in an optimal way for high speed. This logic is the most common form of dynamic gates, achieving a 20% to 50% performance increase over static logic [3].

In Basic Domino logic family evolved from PMOS and NMOS transistors and therefore retained two phase of operation. A single clock is used to both precharge and evaluation phase. This circuitry incorporates a static CMOS buffer into each logic gate as shown in Figure.1 During the precharge phase input is low (CLK=0), PMOS transistor is ON and NMOS transistor is OFF, Node Vo is charged up to Vdd and the output from the inverter is at close to the 0 voltage level. In this phase no path between pull down network to Vo.[9]

Next, during the evaluation phase, NMOS transistor is ON creating the path node Vo through to pull down network to the ground. Node Vo is discharged and inverter make output one.. It should be noted that in Domino logic the transition of nodes Y is always from low to high and it is rippled through the logic from the primary inputs lo the primary outputs.

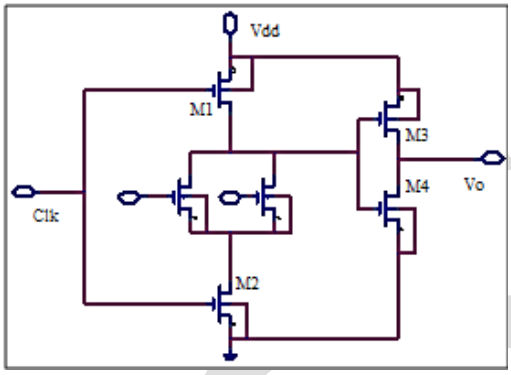

Fig. 1 Basic Domino logic circuit

B. Domino Logic Circuit with keeper

The Keeper technique improves the noise immunity and avoids the problem of charge sharing of Domino logic circuit.

The keeper is a weak pMOS transistor that holds the output at the correct level when it would otherwise float. When the dynamic node is high, the output is low and the keeper is ON to prevent from floating (Figure.2). When the dynamic node (Y) falls, the keeper initially opposes the transition so it must be much weaker than the pull down network. Eventually Z rises, turning the keeper OFF and avoiding static power dissipation.

The keeper must be strong enough to compensate for any leakage current drawn when the output is floating and the pull down stack is OFF.If increase the width of keeper transistor then increase delay, so keeper transistor are order of 1/10 the strength of the pull down stack.[5]

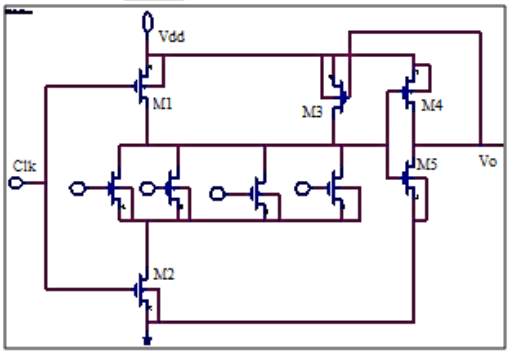

Fig. 2 Domino logic circuit with keeper

C. High Speed Leakage Tolerant Domino

The HSLTD circuit scheme is shown in Figure3. Transistor M3 is used as stacking transistor. Due to voltage drop across M3, gate-to-source voltage of the NMOS transistor in the PDN (Pull down network) decreases. M7 causes the stacking effect and makes gate-to-source voltage of M6 smaller (M6 less conducting). Hence circuit becomes more noise robust and less leakage power consuming. But performance degrades because of stacking effect in mirror current path. This can be increased by widening the M2 (high W/L) to make it more conducting.[6]

If there is noise at the inputs at the onset of evaluation, the dynamic node can be discharged resulting in wrong evaluation.

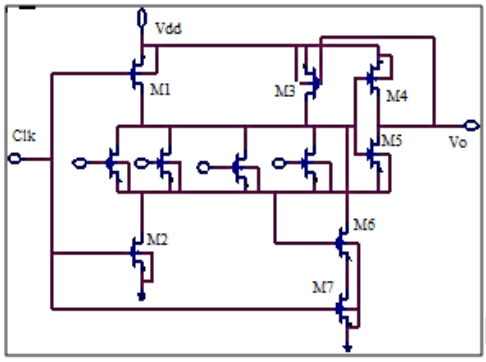

Fig. 3 High Speed Leakage Tolerant Domino Circuit

D. Low Swing Domino Logic

Low swing domino technique applied to reduce dynamic switching power. Two techniques are under the low swing domino circuit. The first technique is low swing domino with fully driven keeper (LSDFDk). The output voltage swing between ground and VDD-Vtn. And second is low swing domino circuit with weakly driven keeper (LSDWDK).

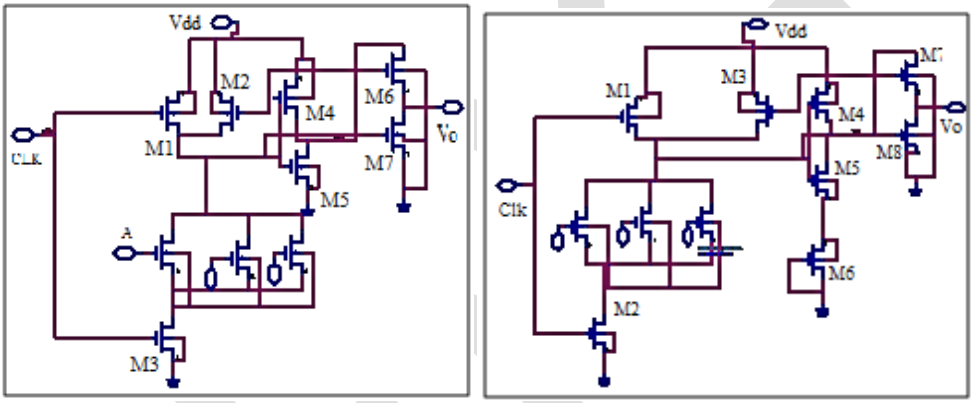

Fig. 4.a: LSDFDK Fig. 4.b: LSDWDK

Fig. 4 Low Swing Domino Logic

These techniques reduce the voltage swing at the output node using the NMOS transistor as a pull up transistor. The first technique is improved the delay and power while maintaining robustness against noise. The second technique reduces the contention current by reducing the gate voltage swing of keeper transistor. LSDWDK generate two different voltage swings. The output voltage swing between ground and VDD-Vtn. The gate voltage swing between |Vtp| and VDD[2].

E. Domino Logic with Variable Voltage Threshold Keeper (DVTVK)

The operation of the DVTVK circuit behaves in the following manner. When the clock is low, the pullup transistor is on and the dynamic node is charged to VDD1. The substrate of the keeper is charged to VDD2 (VDD2 > VDD1) by the body bias generator, increasing the keeper threshold voltage. The value of the high threshold voltage (high-Vt) of the keeper is determined by the reverse body bias voltage (VDD2 - VDD1) applied to the source-to-substrate p-n junction of the keeper. The current sourced by the high-Vt keeper is reduced, lowering the contention current when the evaluation phase begins. A reduction in the current drive of the keeper does not degrade the noise immunity during precharge as the dynamic node voltage is maintained during this phase by the pullup transistor rather than by the keeper.

When the clock goes high (the evaluation phase), the pullup transistor is cut-off and only the high-Vt keeper current contends with the current from the evaluation path transistor(s). Provided that the appropriate input combination that discharges the dynamic node is applied in the evaluation phase, the contention current due to the high-Vt keeper is significantly reduced as compared to standard domino logic. After a delay determined by the worst case evaluation delay of the domino gate, the body bias voltage of the keeper is reduced to VDD1, zero biasing the source-to-substrate p-n junction of the keeper. The threshold voltage of the keeper is lowered to the zero body bias level, thereby increasing the keeper current. The DVTVK keeper has the same threshold voltage of a standard domino (SD) keeper, offering the same noise immunity during the remaining portion of the evaluation phase.

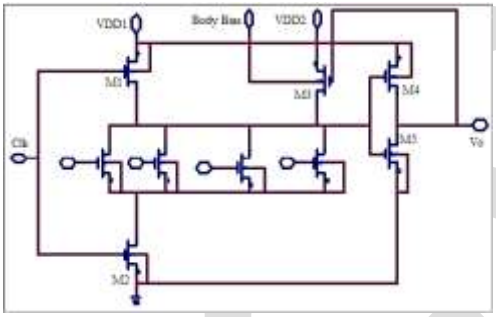

Fig. 5 Domino Logic with variable Voltage Threshold Keeper

The threshold voltage of the keeper transistor is dynamically modified during circuit operation to reduce contention current without sacrificing noise immunity.

F. Sleep Switch Du al Threshold Voltage Domino Logic

The operation of this transistor is controlled by a separate sleep signal. During the active mode of operation, the sleep signal is set low, the sleep switch is cut-off, and the proposed dual-Vt circuit operates as a standard dual-Vt domino circuit. During the standby mode of operation, the clock signal is maintained high, turning off the high-Vt pull-up transistor of each domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, thereby turning off the high-Vt NMOS transistor within the output inverter. The output transitions high, cutting off the high-Vt keeper.

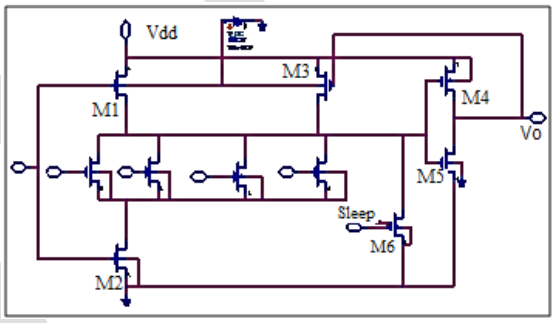

Fig. 6 Sleep Switch Dual Threshold Voltage Domino Logic

After a sleep switch dual-Vt domino gate is forced to evaluate, the following gates (fed by the non-inverting signals) also evaluate in a domino fashion. After the node voltages settle to a steady state, all of the high-Vt transistors in the circuit are strongly cut-off, significantly reducing the subthreshold leakage current.

The sleep switch circuit technique exploits the scalable of the dual-Vt transistors to reduce the subthreshold leakage current by strongly cutting off all of the high-Vt transistors.

POWER DISSIPATION

The power consumed by CMOS circuit classified in two type.

- Static power dissipation
- Dynamic power dissipation

i. Static Power Dissipation:- This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. static power dissipation in CMOS inverter is negligible.[6]
ii. Dynamic Power Dissipation:-The PMOS and NMOS transistors are on during the perform operation simultaneously. the duration of changing inputs low to high and discharging high to low pMOS and nMOS turn on respectively. During this time a current flows between Vdd to GND (make short path) and Dynamic Power produce. The dynamic power dissipation is proportional to the square of voltage supply.[7-8]

SIMULATION AND RESULT

In this work, the OR and AND logic gates had used for implementation of six techniques. The power consumption (Pavg), propagation delay (Tpd) and power delay product (PDP)are used to compare these techniques. The circuits implemented are OR gate for 4 input, 6 input and AND gate for 4 input and 6 input. These design styles are compared by performing detailed transistor-level simulations on circuits using Advance Design System (ADS). The results of the circuits for all techniques are given below. Table1 showed the comparison for all the techniques for four input OR gate. Table2 shows the comparison of all the six techniques with that of standard domino circuit for six input OR gate.Table3 shows the comparison of all the six techniques for four input AND gate. Table4 shows the comparison of all the six techniques with that of standard domino circuit for six input AND gate.

From the results, it can be observed that the Domino logic techniques, viz., Domino logic circuit with keeper, High speed leakage tolerant domino and Low Swing Domino, Domino Logic with Variable Voltage Threshold Keeper, Sleep Switch Dual Threshold Voltage Domino techniques provide lower values of power dissipation, propagation delay and PDP when compared to the standard domino logic structure. The propagation delay (Tpd-Sec), power consumption (Pavg-Watt) and power delay product (PDP-Watt-Sec) calculated and plotted in the form of graph.

Table.1: Comparison for four input OR gate

Technique	Tpd	Pavg	PDP
Domino	3.77E-08	3.77E-06	1.42E-13
Keeper	3.76E-08	4.22E-06	1.59E-13
HSLDT	3.78E-08	2.19E-06	8.21E-14
LSDFDK	3.77E-08	5.85E-06	2.20E-13
DVTVK	3.77E-08	2.72E-05	1.02E-12
SLS	3.77E-08	4.69E-05	1.77E-12

Table.2:Comparison for six input OR gate

Technique	Tpd	Pavg	PDP
Domino	1.05E-07	4.45E-06	4.67E-13
Keeper	1.03E-07	6.46E-05	6.68E-12
HSLDT	1.06E-07	6.67E-06	7.07E-13
LSDFDK	1.05E-07	7.55E-06	7.91E-13
DVTVK	3.61E-08	2.31E-04	8.37E-12
SLS	1.06E-07	6.70E-05	7.07E-12

Table.3: Comparison for four input AND gate

Technique	Tpd	Pavg	PDP
Domino	5.09E-09	1.057E--6	5.38E-15
Keeper	1.01E-08	8.11E-07	8.19E-15
HSLDT	5.00E-09	5.73E-07	2.87E-15
LSDFDK	1.01E-08	6.10E-07	6.16E-15
DVTVK	5.00E-09	4.68E-05	2.34E-13
SLS	1.02E-08	3.95E-05	4.01E-13

Table.4: Comparison for four input AND gate

Technique	Tpd	Pavg	PDP
Domino	5.09E-09	1.48E-06	7.52E-15
Keeper	1.01E-08	8.09E-07	8.17E-15
HSLDT	1.34E-09	2.99E-06	4.00E-13
LSDFDK	5.12E-09	3.01E-07	1.54E-15
DVTVK	1.00E-08	5.19E-05	5.19E-13
SLS	1.02E-08	3.64E-05	3.71E-13

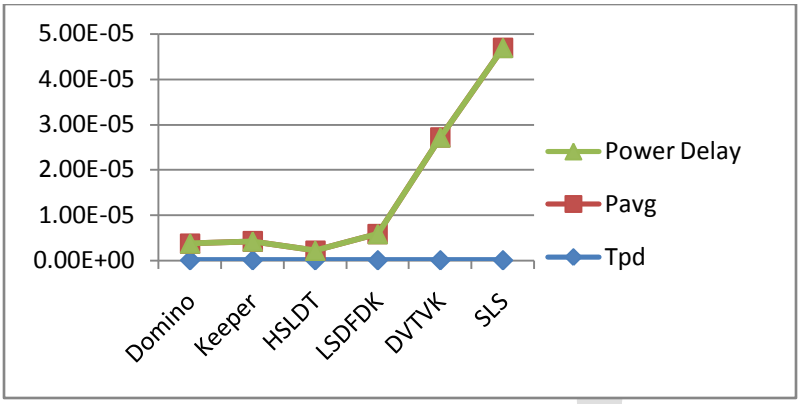

Chart.1: Comparison for four input OR gat

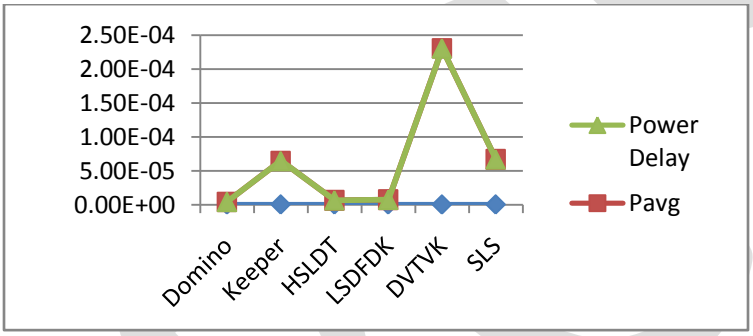

Chart.2 Comparison for six input OR gate

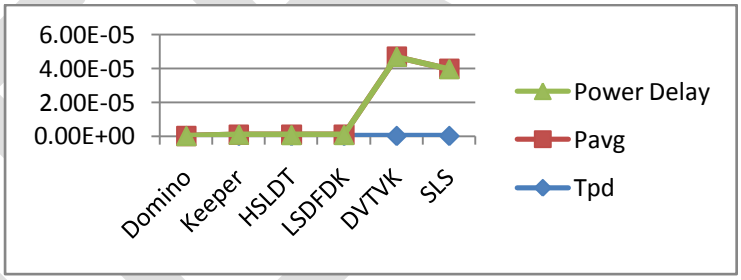

Chart.3 Comparison for four input AND gate

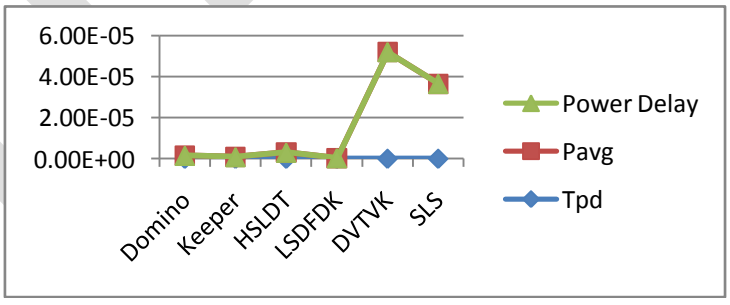

Chart.4 Comparison for six input AND gate

CONCLUSION

In this work, an attempt had been made to simulate OR gate and AND gate for four and six inputs by using six domino based techniques including basic domino (standard domino).

The comparative analysis from table.1 for 4 input OR gate showed HSLDT had less power, less Tpd and low PDP compared to other domino techniques.

The comparative analysis table.2 showed the maximum number (six) of input for OR gate Basic domino logic technique is better because it had low power consumption, PDP but DVTVK had less Tpd.

Similarly comparison for the four input AND gate table.3 showed HSLDT had less power, less Tpd and low PDP compare to other techniques. The table also showed propagation delay of DVTVK had equal to the HSLDT.

The comparative analysis table.4 showed the maximum number (six) of input for AND LSDFDK technique is better because it had low power consumption and less PDP but HSLDT had less Tpd.

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