Performance Analysis of Buck Power Converter Using Fuzzy Logic Controllers

Zeeshan Ali, Muhammad Khalid and Shakil Ahmad

Abstract- In this paper the performance and design comparison of conventional fuzzy logic controller (CFLC) and the single input fuzzy logic controller (SIFLC) to regulate the output voltage of the buck power converter has been proposed. The CFLC is the two term controller it has two inputs error and the change of error it uses the 2-dimensional rule table, by using the idea of the signed distance method in the designing of the SIFLC, the 2-dimensional rule table for the CFLC can be converted into 1-dimensional rule table or linear control surface. The important feature is by means of signed distance method the two inputs CFLC can be converted into SIFLC with no significant change in the performance also as the rule table is reduced so SIFLC takes less time to execute its algorithm. To demonstrate that the performance of both controllers CFLC and SIFLC are identical a MATLAB simulation is carried out.

Index Terms: Buck Power, Converter, Fuzzy Logic Controllers, Defuzzification

I. INTRODUCTION

Buck converters are the most widely used DC-DC converter in the portable devices to provide power from the battery. They are often used in the microprocessor voltage regulation (VRM) applications. The DC-DC converter needs to regulate its output voltage to lower voltage and must quickly respond to fast load current transients to keep their output voltage within a limited range [1]. Buck regulators are also used as the switch mode power supplies for the base band digital core and the RF power amplifiers (PA) [2].

Traditionally the linear controllers are used for the buck converters to regulate its output voltage among of which, PI and PID controllers are most popular. But due to the parasitic parameters changing with the switching frequency the performance of the converters gets degraded [3], due to which the controlling of the buck converter is quite challenging for the linear controllers. Also the linear controllers are the 'modeled based' controllers, which merely depends on the mathematical model of the converter system.

Recently, a new class of the controllers has been introduced that does not depend on the model of the system to be controlled. These types of controllers are called the 'non-modeled' based controllers. Among of which the fuzzy controllers are most popular. Fuzzy controllers are robust and have excellent immunity to the external disturbances.

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The conventional fuzzy logic controllers (CFLC) performance depends on the number of inputs to the controllers, its corresponding rule table, and the other fuzzy processes like fuzzification, defuzzification and the rule base evaluation. Due to all these processes the overall structure of the CFLC becomes complex, and its hardware implementation is quite challenging. Furthermore, as the number of inputs increases the rule table increases square of the time of inputs.

So due to which the computational burden for the computer on which CFLC is to be implemented also increases. For the implementation of CFLC many researchers went to the DSP [4]. But the DSP is costly and in some applications it is not justifiable. Another way to reduce the computational burden is two reduce the rule table but as we reduced the rules the performance of the CFLC degraded.

So in this paper the SIFLC design is proposed which simply reduces the two dimensional rule table of the CFLC into the single dimensional rule table with number of rules significantly less as compared to conventional fuzzy logic controller. The method used for the SIFLC is the signed distance method which reduces the 2-dimensional control surface to linear piece wise control surface. Due to signed distance method the number of rule to control the buck converter is reduced and secondly, we find that the performance of both the controllers is identical.

In the starting of the paper the signed distance method for the SIFLC is proposed also the derivation of the 1-dimensional rule table is given after that brief average modeling for the buck power converter is driven. In the last section of the paper the MATLAB/SIMULINK simulation is carried out that demonstrate that the performance of both the controllers is identical.

II. SIGNED DISTANCE METHOD FOR SIFLC DESIGN

The CFLC have generally two inputs error (e) and the change of the error (é). The rule table for the CFLC can be designed based on the general behavior of the buck power converter when the controller is applied on it. This can be summarized as follow: When the error (e) is small and the change of error (ė) iszero then the output of the controller i.e. the duty cycle is changing slowly. When the error is large and the derivative of the error is also large then the duty cycle is changing very rapidly. When the error signal and its derivative is zero then there is no need to change in the duty cycle

In the similar way we can design the rules when the error and its derivative both are negative. By using these known

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facts based on the performance of the buck converters when subjected to the controller a two dimensional phase plane rule table can be constructed as shown in the Table 1. Such kind of rule table for the FLC is known as the linear rule table [5]. This type of rule table as shown in Table 1 is also called the Toeplitz structure [6]. The main feature of this structure is that it has the same output membership function in the dimension along the diagonal and each point on the diagonal has the certain magnitude of distance from the main diagonal P_Z. For the CFLC instead of using the two inputs (e, ė) to obtain the output (ů), we can use the single input (d) to obtain the same output (ů). The input (d) represents the absolute value of the distance of each non-zero i.e. P_{NM}, P_{NB}, P_{NM} etc diagonal to the main one (P_Z).

To derive for the distance (d) let S (e_1, e_1) and T (e_2, e_2) are the two points on the main diagonal (P_Z) and the diagonal (P_{NS}) respectively. Now as all the diagonals are parallel to each other so for all the points on the diagonal (P_Z) and that of (P_{NS}) the distance remains same by the geometry. So to find the distance (d_{NS}) between the two diagonals (P_Z) and (P_{NS}) we have to first find out the equation for the main diagonal (P_Z) and after that by using point to line distance formula we can calculate the distance (d_{NS}). The mathematics for the calculation of the distance (d_{NS}) is shown below.

TABLE 1 TOEPLITZ STRUCTURE

e \ ė	PB	PM	PS	Z	NS	NM	NB
NB	Z	NS	NM	NB	NB	NB	NB
NM	PS	Z	NS	NM	NB	NB	NB
NS	PM	PS	Z	NS	NM	NB	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PB	PB	PM	PS	Z	NS	NM
PM	PB	PB	PB	PM	PS	Z	NS
PB	PB	PB	PB	PB	PM	PS	Z

P_{NB} P_Z P_N P_{NS} P_{PB} P_{PM} P_{PS}

The equation of the main diagonal is of the form of

$$\dot{e} + \alpha e = 0 \qquad (1)$$

Where α is the slope of the main diagonal P_Z which is -1 in this case because diagonal is the bisector of the 2nd and 4th quadrants as shown by Table 1. The Fig.1 shows the complete derivation for the signed distance method.

Now the distance between the points S (e_1, e_1) and T (e_2, e_2) can be formulated in Equation (2).

$$d = \frac{\dot{e}+\alpha e}{\sqrt{1+\alpha^2}} \qquad (2)$$

The derivation for 'd' corresponds to the new one dimensional rule table as shown in Table 2. The diagonals P_{NB}, P_{NM}, P_{NS}, P_Z, P_{PS}, P_{PM}, P_{PB} in Table 1 now becomes the inputs for the Table 2. Whereas the NB, NM, NS, Z, PS, PM, PB are the corresponding outputs for the input diagonal lines.

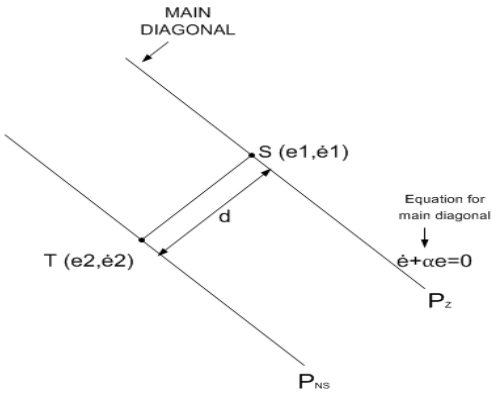

Fig.1. Derivation for signed distance method

TABLE 2 REDUCED RULE TABLE FOR SIFLC

	P_{NB}	P_{NM}	P_{NS}	P_Z	P_{PS}	P_{PM}	P_{PB}
	NB	NM	NS	Z	PS	PM	PB

The Table 2 shows that the control action is now taken with the help of single input (d). Due to this single input d it is appropriate to called it a single input fuzzy logic controller (SIFLC). The only limitation in reducing the 2-dimensional rule table is that the table should be Toeplitz in nature. Fortunately in power converters most of the rule table used are usually of Toeplitz in structure. With the reduction to the one dimensional rule table the control surface for the SIFLC is the linear piece wise function as shown in fig.2 this can be obtained by using the input (d) and output (ů) as triangular membership function, the fuzzification and defuzzification uses the centre of gravity (COG) method [7]. Due to the linear piece wise control surface of SIFLC the computational speed to execute the algorithm is increased. The input and the output memberships function for the SIFLC are shown in Fig.3. The main advantage of the SIFLC is that it can be implemented through a single dimensional lookup table so the process involved in the fuzzy control that are fuzzification , rules inferences and defuzzification are no longer required so due to which the computational speed for SIFLC become fast. In the next section average modeling for the buck power converter is carried out.

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III. BUCK DC-DC CONVERTER AVERAGE MODELLING

The circuit diagram of the buck power converter is illustrated in the fig 4. The circuit given in fig 4 has two states i.e. when the switch (SW) is closed and when it is opened. When the switch is in the 'on' state (closed) the diode 'D' is reversed biased and the current in the inductor 'L' increases linearly and when the switch is in 'off' state (opened) the energy stored in the inductor release through the output RC circuit. The current is not allowed to reach to zero because the converter is assumed to work in the continuous conduction mode (CCM).

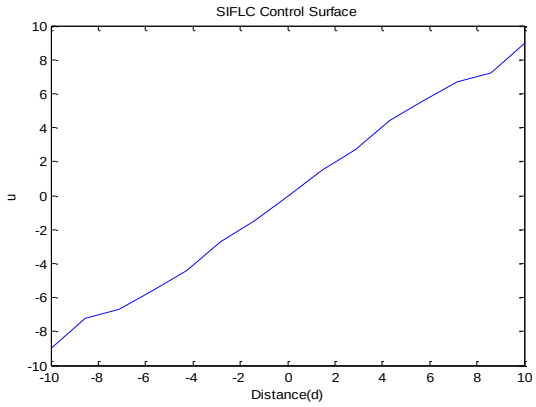

Fig. 2. SIFLC linear control surface

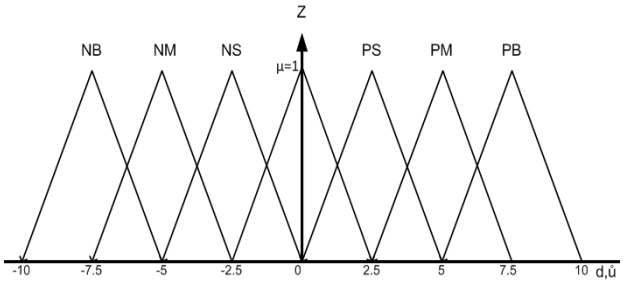

Fig. 3. Input and output membership for SIFLC

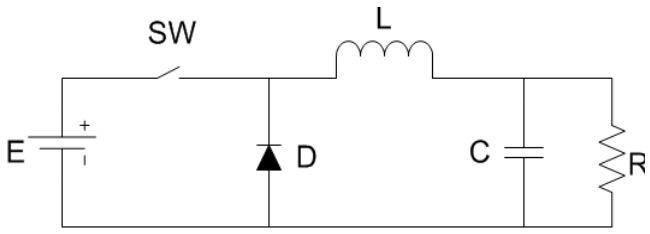

Fig. 4. Buck converter

In order to obtain the overall average model of the buck power converter we assumed that the inductor current i_L and the capacitor voltage V_o as a state variable. If the converter switch SW is in the 'on' (closed) state the following equations holds

$$\frac{di_L}{dt} = \frac{E}{L} - \frac{V_O}{L} \qquad (3)$$

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_O}{RC} \qquad (4)$$

When the switch is 'off' (opened) then the following equations hold

$$\frac{di_L}{dt} = -\frac{V_O}{L} \qquad (5)$$

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_O}{RC} \qquad (6)$$

Let the duty cycle of the converter operation is donated by 'd' and its period is by T. Then the duration for the switch to be closed and opened are donated by dT and (1-d) T respectively. Then multiply each expression by their respective duration. Let suppose the average value of $\frac{di_L}{dt}$ can be obtained by multiplying Equation (3) by dT and Equation (5) by (1-d)T and then add the two equations after that dividing the overall equation by T, i.e.

$$\frac{di_L}{dt} = \frac{dT\left(\frac{E}{L}-\frac{V_O}{L}\right)+(1-d)T\left(-\frac{V_O}{L}\right)}{T} \qquad (7)$$

After simplifying equation (7) yields

$$\frac{di_L}{dt} = \frac{dE}{L} - \frac{V_o}{L} \qquad (8)$$

The similar operation perform for $\frac{dV_o}{dt}$ we obtain the below expression

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_o}{RC} \qquad (9)$$

The equation (8) and (9) describes the complete average model of the buck power converter. The SIMULINK model of these equations is shown in Fig. 5.

IV. CFLC DESIGN FOR THE BUCK CONVERTER

Since the CFLC have two inputs for the control of the buck power converter error (e) and its derivative (ė). The universe of discourse for the input and output membership functions

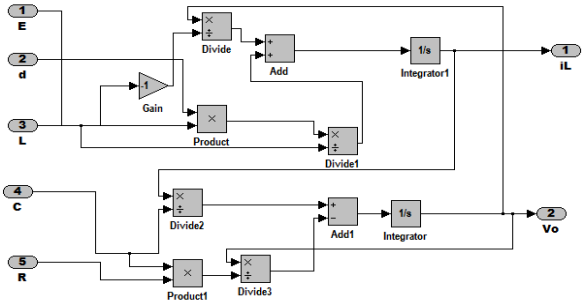

Fig. 5. SIMULINK average model of buck power converter

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are so adjusted so that it do not goes into saturation for any value of error (e) and its derivative (ė). The inputs and output membership functions (MF) used for the CFLC are the triangular MF's shown in fig.6 and the inference mechanism for the controller is of Mamdani type [8]. The rule table constructed based on the performance of the converter when subjected to the controller. Such that if error (e) is small and the derivative of error (ė) is also very small then the output (ů) changes very little, in such a way the 2-dimensional rule table can be constructed as shown in Table 3.

TABLE 3 CFLC RULE BASE

ė / e	NB	NM	NS	Z	PS	PM	PB
NB	-10	-10	-10	-10	-5	-2.5	0
NM	-10	-10	-10	-5	-2.5	0	2.5
NS	-10	-10	-5	-2.5	0	2.5	5
Z	-10	-5	-2.5	0	2.5	5	10
PS	-5	-2.5	0	2.5	5	10	10
PM	-2.5	0	2.5	5	10	10	10
PB	0	2.5	5	10	10	10	10

The control surface for the CFLC is shown in fig. 7. The control surface for the CFLC is the 3-dimensional nonlinear control surface. The overall simulation setup is shown in Fig. 8. The CFLC has the two inputs error and its derivative the output of the CFLC is the change in duty cycle (ů) so an integrator is used to obtain the output as a duty cycle (u) to control the switching of the converter switch in order to regulate the output voltage at the reference point. Furthermore a duty cycle limiter is also used that limits the duty cycle within the range of [-0.8 0.8]. The function of this is to avoid the converter instability [9]. The scaling gains are also used in order to optimize the performance of the converter system heuristically.

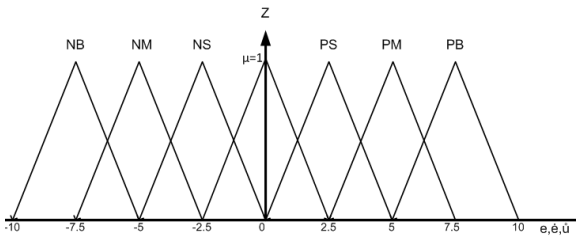

Fig.6 .Input, change in input and output membership for CFLC

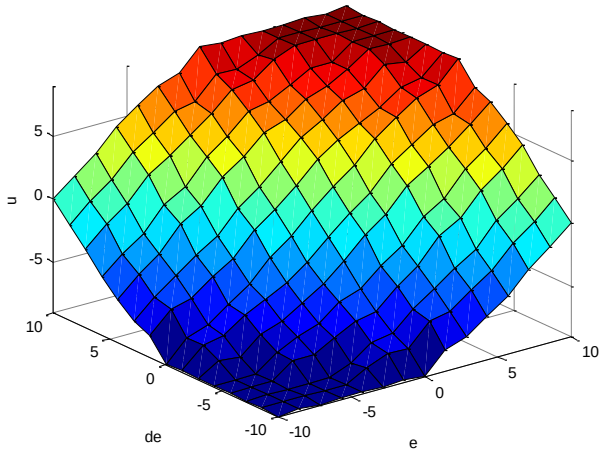

Fig. 7. CFLC 3D control surface

The proposed SIFLC can also be implemented with the help of the lookup table as the work [12] suggest. The simple lookup table minimize the time issues of inference and the time involve in that of the fuzzification and defuzzification.

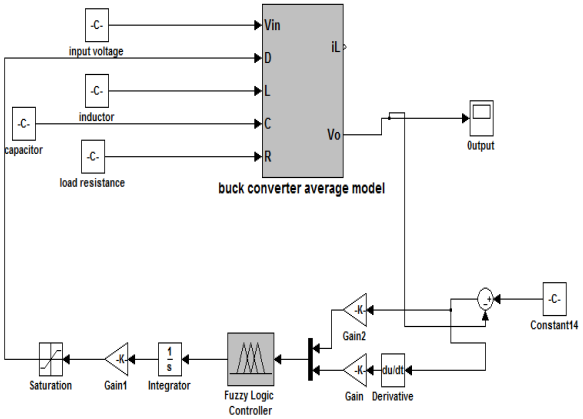

Fig. 8. Simulink/MATALB block diagram for the CFLC with buck converter

V. PERFORMANCE COMPARISON BETWEEN CFLC AND SIFLC

In this section of the paper the performance of both the controller can be judged by using a MATLAB/SIMULINK [10] simulation. The parameters used for the buck converters used in the simulation are indicated in the Table 4. The rule base used for the SIFLC is shown in table 5. The fig.9 shows the simulation setup for the SIFLC with the buck power converter system.

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TABLE 4 BUCK CONVERTER PARAMETERS

PARAMETER	SYMBOL	VALUE
INPUT VOLTAGE	E	15V
INDUCTOR	L	4.1e-6H
CAPACITOR	C	376e-6F
LOAD RESISTANCE	R	1Ω

TABLE 5 SIFLC RULE BASE

d	P_{NB}	P_{NM}	P_{NS}	P_Z	P_{PS}	P_{PM}	P_{PB}
ů	-10	-5	-2.5	0	2.5	5	10

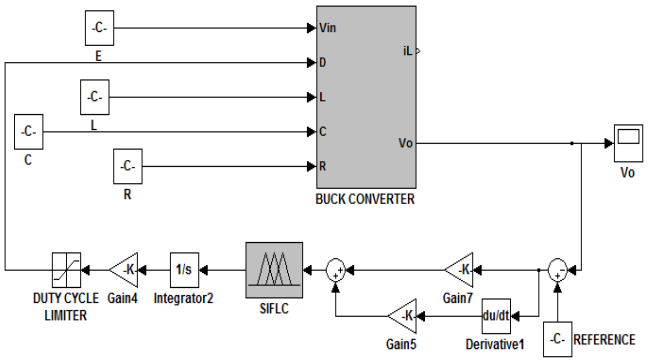

Fig. 9. Simulink/MATALB block diagram for the SIFLC with buck converter

The Fig. 10 and Fig.11 shows the performance of the CFLC and the SIFLC controller respectively when the load is stepped change from 1Ω to 0.5Ω. The Fig.12 shows the difference in their responses upon the load changes.

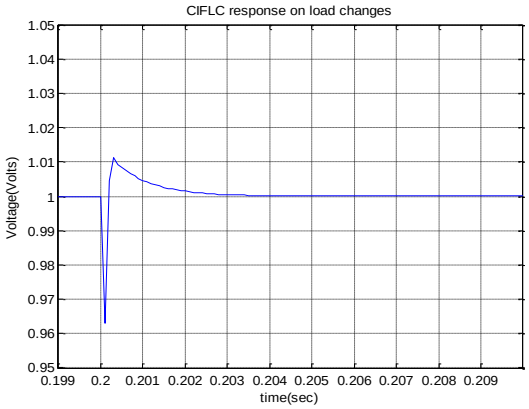

Fig.10. CFLC response when load changes

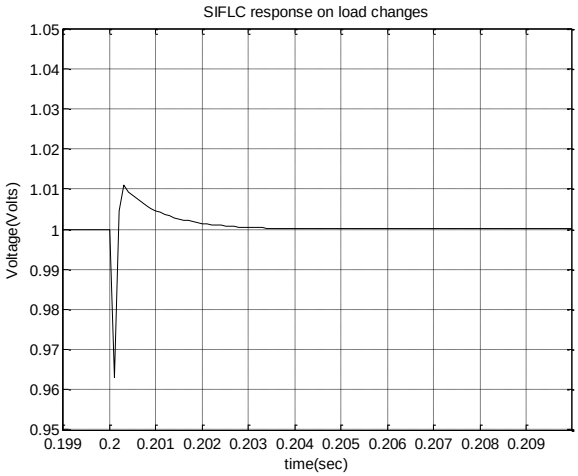

Fig.11. SIFLC response when load changes

The Fig 13 and Fig.14 shows the performance of the CFLC and the SIFLC controller respectively when the input voltage is stepped change from 15V to 10V. The Fig.15 shows the difference in their responses upon the input voltage changes.

The results from Fig.12 and 15 shows that there is no significant difference between the performance of the SIFLC and the CFLC upon changing load resistance and the input voltage respectively. Next the execution time for both SIFLC and CFLC algorithms has been compared. For this an appropriate bench mark is the total CPU run time elapsed by the SIMULINK [10] program. To do this the simulation parameters for both the controllers are kept same. 20 sets of

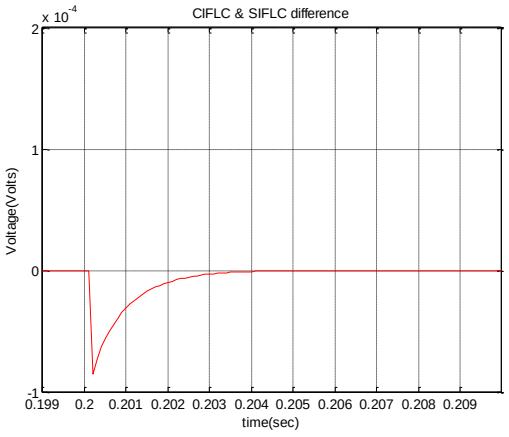

Fig.12. Difference in the Responses of SIFLC and CFLC when load resistance stepped change

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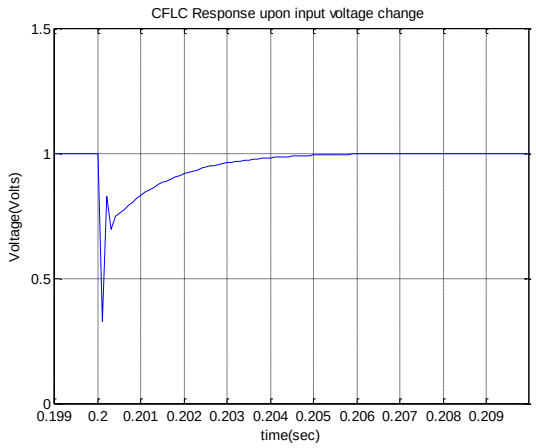

Fig.13. CFLC response when input voltage changes

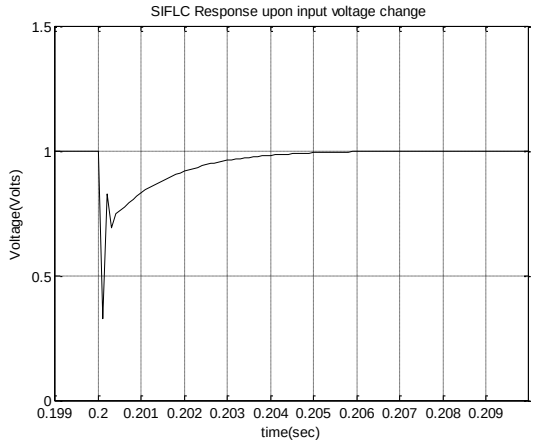

Fig.14. SIFLC response when input voltage changes

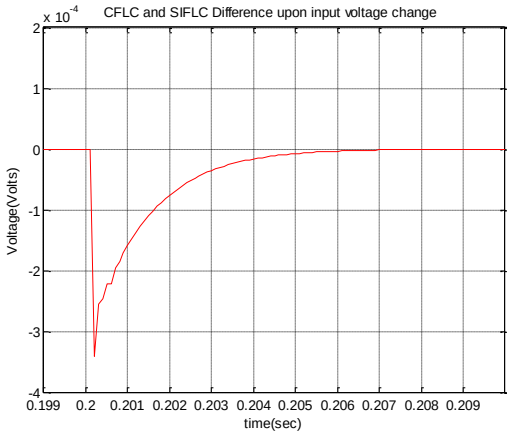

Fig.15, Difference in the Responses of SIFLC and CFLC when input voltage stepped change

simulation are then carried out and the mean execution time for the both controllers is shown in fig. 13. From the bar graph of fig. 13 it is vivid that the SIFLC takes less time to execute its algorithm which is in this case is 6.12 seconds whereas for the CFLC it is 18.34 seconds.

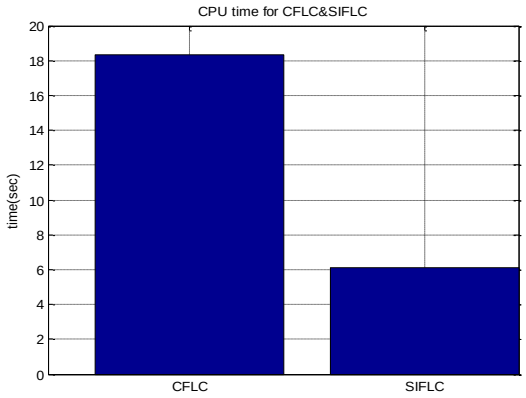

Fig. 16. CPU time consumed by SIFLC and CFLC

VI. CONCLUSIONS

Due to the signed distance method used in the SIFLC design the overall CPU time and the rule table for the CFLC are reduced. The performance of the SIFLC is also same as to the CFLC to regulate the output voltage of the buck power converter. This performance suggests that SIFLC can replace the CFLC with no significant change in the response of controllers.

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