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Design of Low Noise PLL by Improving Supply Sensitivity of VCO

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ABSTRACT : This paper describes the noise reduction for fully integrated CMOS PLL. Since the Switching of large digital system introduces power supply or substrate noise which perturb the more sensitive blocks in a PLL. Which work as dominant jitter for VCO. This paper describes designs for both a PLL and a clock buffer that reduce sensitivity to supply noise for low-power applications. The supply noise rejection can be done by using active or passive filter and improving supply sensitivity. We are using both method for reduce noise to improve performance of PLL. By designing of low noise PLL, the high static and dynamic supply noise rejection have been achived. Design uses static CMOS Inverter as a building block of VCO and clocking buffering. The design is fabricated at 0.125 m technology.

Keywords: CMOS, Phase lock loop, Voltage controlled oscillator, Noise rejection, low power.

I. INTRODUCTION

For high performance digital system PHASE-LOCKED LOOPS (PLLs) are widely used. PLLs multiply low-frequency reference clocks to produce low-jitter high-frequency clocks that drive large capacitive loads. For many applications, clock jitter and power dissipation are two important design criteria. Switching activity in large digital systems introduces power-supply or substrate noise which perturb the more sensitive blocks in a PLL. In particular, any noise injected onto the voltage-controlled oscillator (VCO) elements and the clock buffers is the dominant source of jitter in these systems. Power dissipated by PLLs is often a small fraction of the total active power. However, during sleep modes where the PLLs must remain in lock, it can be a significant fraction of the power dissipated. This paper describes designs for both a PLL and a clock buffer that reduce sensitivity to supply noise for low-power applications. The PLL operates over a wide frequency range to accommodate testability and further system power optimization.

Two common strategies improve supply-noise rejection. The first strategy is to filter the supply voltage using either a passive or active filter. The second strategy is to improve the supply sensitivity of the buffer elements. Differential delay elements for a VCO have been favored because they reject common-mode noise. Both methods are often jointly used for higher performance.We are describing the proposed design of the PLL with a new filtering strategy. The design focuses on improving the power performance while achieving both high static and dynamic supply-noise rejection. The delay sensitivity to supply noise using the second strategy have been described.

II. THEORY OF LOW NOISE PLL DESIGNING

We will present the circuit-level low phase noise design methods for LC VCO. Because LC VCO exhibitsmuch lower phase noise than ring oscillator based VCO, it is dominated in low phase noise PLL design. therefore, we concentrated on low phase noise design methods for LC VCO. In principle, phase noise is traded off by power consumption for VCO and PLL design.

The phase noise of LC VCOs are normally expressed by Leeson's equation :

$$L(\Delta\omega) = \frac{1}{V_0^2}\frac{KT}{C}\frac{\omega_0}{Q}\frac{2}{\Delta\omega^2}F \qquad \ldots (1)$$

Where V_0 is the VCO output amplitude, C is the tank capacitance, Q is the tank quality factor that is mainly determined by the quality factor of the on-chip inductor, and F is the noise factor that is the constant proportionality of the noise contributions from various circuit elements. Being circuit specific, the noise factor is dependent on oscillator topology in terms of device sizes, current, and other circuit parameters. Equation (1) reveals that doubling the tank capacitance while keeping the oscillation frequency and amplitude constant, gives a 3 dB reduction in phase noise. In practical VCO designs, power budget is normally specified, which means a maximum current value cannot be exceeded with a fixed supply voltage. In these cases, doubling the tank inductance while keeping the oscillation frequency and the current, gives a 3 dB reduction in phase noise. The oscillation amplitude is given by :

$$V_0^2 \propto I_0 R_p = I_0 Q\omega L \qquad \ldots (2)$$

The current have set at maximum value i.e. P_max/ VDD for having an oscillation amplitude as high as possible. With a doubled tank inductance value L, the effective tank resistance Reff and the oscillation amplitude are also doubled, assuming the quality factor is independent on the inductance value. For a constant oscillation frequency, the tank capacitance value should be halved. To reduce the phase noise, it is necessary to reduce the circuit noise

factor F. Design techniques to reduce the phase noise due to the circuit have been widely studied and investigated in recent years. We are reducing noise by following methods.

A. Noise filtering

The use of an on-chip LC filter can effectively suppress the noise from the tail transistor. Fig. 1 shows the schematic of a VCO with the noise filter to suppress the noise of the tail current transistor. The capacitor C_f provides a low impedance path for the noise at $2f_0$ of the tail current transistor. The inductor L_f ensures a high impedance common node for the differential pair. The big off-chip inductor L_{If} degenerates the low frequency noise by the factor $|1+ jg_m\omega L_F|^2$, where g_m is the transconductance of the tail transistor.

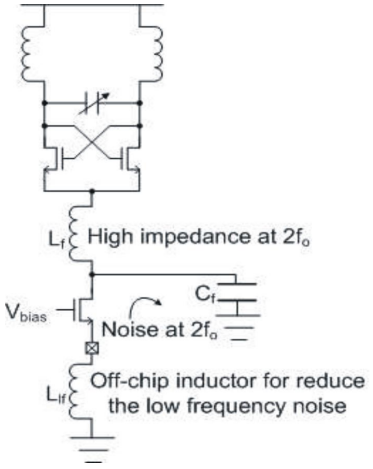

Fig. 1. A LC VCO with the noise filter.

B. Harmonic tuned LC tank

As described by Hajimili'e phase noise model, the most noise-sensitive moment of VCOs is the zero crossing point of the VCO output voltage. The phase noise resulting from a noise injected around the zero crossing point is proportional to the voltage slope at the zero crossing point. Therefore, increasing the slope of VCO output voltage can reduce phase noise. Therefore, increasing the slope of VCO output voltage can reduce phase noise.

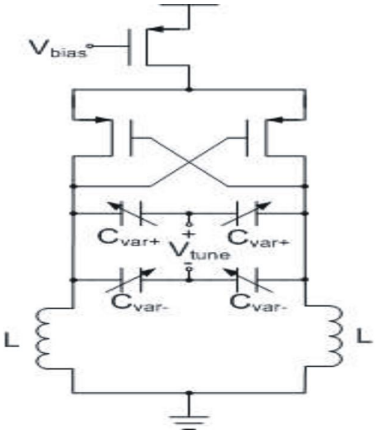

Fig. 2. A differential tuning LC VCO.

Fig. 3 shows a LC VCO with harmonic tuned LC tank and its output voltage waveform. The output voltage of a VCO with harmonic tuned LC include both the fundamental and the third harmonic frequency component and has a waveform more like a square wave. Therefore, the slope of the output voltage of a VCO with harmonic tuned tank is steeper than that of a standard LC VCO and the phase noise is reduced.

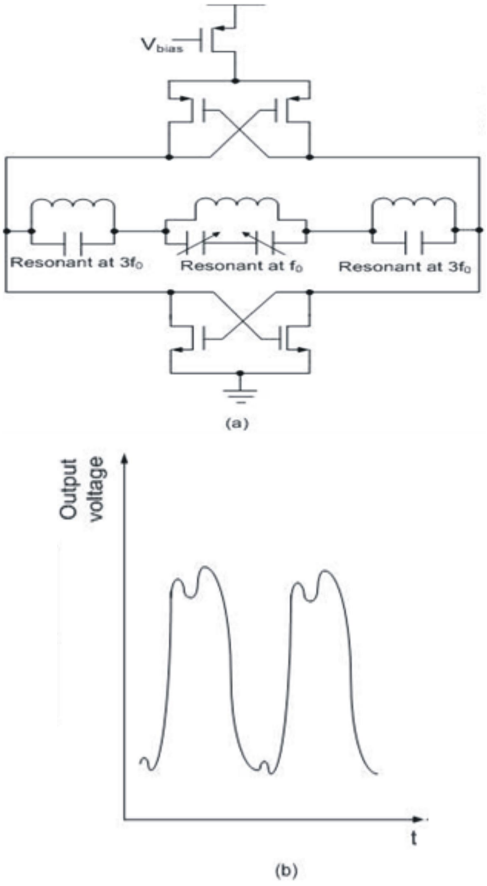

Fig. 3. A complementary VCO with LC tuned tank: (*a*) schematic and (*b*) output voltage waveform.

III. CMOS LAYOUT DESIGNING

A. Layout of Noise filtering circuit

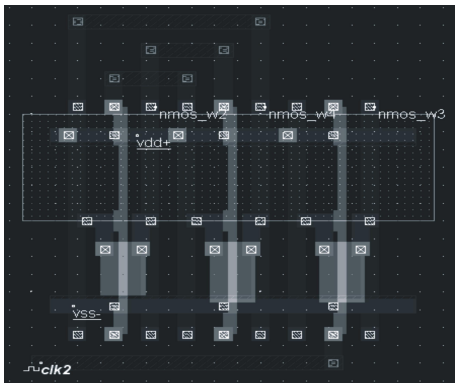

Fig. 4. Layout of Noise filtering circuit.

B. Layout of Harmonic tuned circuit

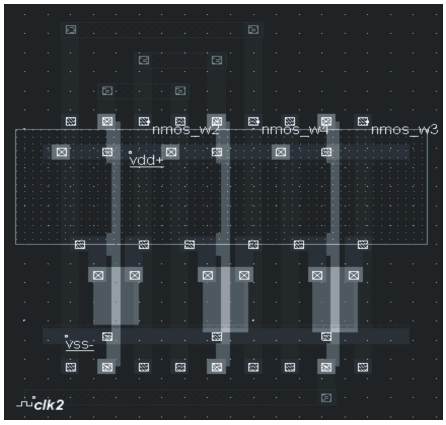

Fig. 5. Layout of Harmonic Tuned Circuit.

III. RESULTS AND ANALYSIS

Two method for reducing noise have been studied. For low noise PLL we designed filter noise circuit and Harmonic tuned circuit. Since PLL were presented which simultaneously achieve high operating frequency and good phase noise through the use of several innovative architectural and circuit design techniques. These circuits, through simulation, measurement, demonstrated performance and speed in a gigahertz range which till date has not been realized in a conventional CMOS process. The designed circuit have analysed with required parameter for reducing the noise of PLL.

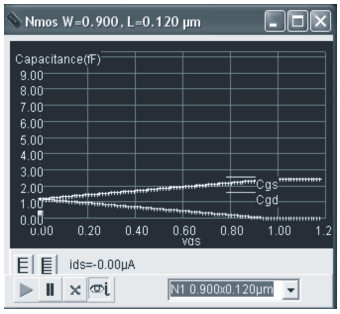

Fig. 6. Nmos W = 0.900, L = 0.120 m

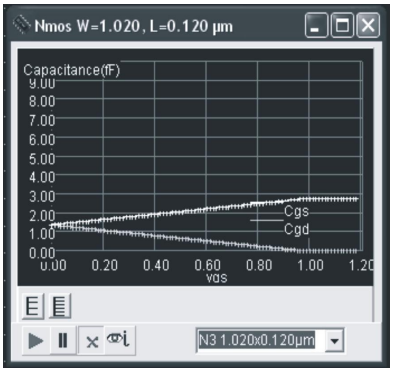

Fig. 7. Nmos W = 1.020, L = 0.120 m

In both simulation results, the variation in capacitance value is shown as the dimension is reducing and the value of capacitance is increasing. Due to which the value of L is decrasing. Reduction in L will help to decrease the noise across PLL. All the results are taken at W = 0.1 µm and L = 0.01 µm.

IV. CONCLUSION

The main focus of this paper was to design the low noise CMOS PLL. The dominated phase noise source in a PLL are different type of block like VCO, Tuned Circuit etc. Understanding the generating mechanism of phase noise in VCO and other PLL blocks is the theoretic basis to design low phase noise PLLs. In this paper, the phase noise mechanism of VCOs, including both of ring oscillator based VCO and LC tank based VCO, were deeply studied and analyzed.

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