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Design and Development of Phase Locked Oscillator at UHF and L-Band

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ABSTRACT : Line of Sight (LOS) Communication between airborne platform and ground control station is generally provided at C-Band. The RF front end Unit is using for frequency translation to make it enable for transmission in the air efficiently with reasonable antenna size. Phased Locked Loop (PLL) is used to provide frequency source used as Local oscillator for frequency translation. Fixed Frequency PLL is known as Phased locked Oscillator (PLO).

To design PLO we mainly required 10MHz Oscillator, Phase Frequency Detector Chip, Loop filter and Voltage controlled Oscillator (VCO). The Critical part of the PLO design is loop filter design.

The Aim to design Separate PLO at 1430 MHz for UP-Conversion Chain and at 760 MHz for DOWN-Conversion Chain. The additional 90 MHz Signal is required in 1430 MHz PLO Module for tracking purpose which is further up converted at 5000±100 MHz.

I. INTRODUCTION

The phase locked loop concept was first developed in 1930s.It has since been used in communication systems of many types, particularly in satellite communications systems. Until recently, however, phase locked systems have been too complex and costly for use in most consumer and industrial systems, where performance requirements are more modest and other approaches are more economical. The PLL is particularly amenable to monolithic construction, however, and integrated-circuit phase locked loops can now be fabricated at very low cost. Their use has become more attractive for many applications such as FM demodulators, stereo demodulators, tone detectors, frequency synthesizers, and others.

II. DESIGN OF LOOP FILTER

The loop filter is one place where the designer really gets to shape the loop. Unfortunately, most filters are passive in that they do not amplify the signal. An active filter is one that provides amplification in addition to filtering. These types of filters are used in equalizers and of course in PLLs where relative gains are important. The only difference between active and passive filter is 1 or less where the gain of active filter is KL. Both filters have same frequency response except for the linear gain. Three filter types that are used in PLLs are :

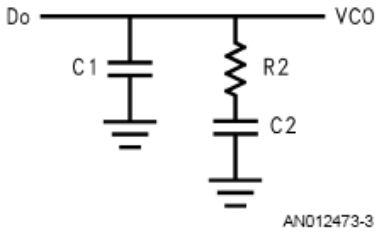


FIGURE 3. 2nd Order Passive Filter

$$Z(s) = \frac{s \cdot C2 \cdot R2 + 1}{s^2 \cdot C1C2 \cdot R2 + s \cdot C1 + s \cdot C2} \quad \text{... (1)}$$

Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T1 = R2\frac{C1.C2}{C1 + C2} \quad \text{... (2)}$$

$$T2 = R2.C2 \quad \text{... (3)}$$

A. Required specification for VCO

Oscillation frequency range : 1410-1440 MHz

Phase niose @ 10 KHz offset : –111 dBc/Hz

Tuning Voltage : 1-5 Vdc

Supply Voltage : 5 Vdc

Operating temp. range : –40 to 85 °C

Oscillation frequency range : 734-804 MHz

Phase niose @ 10 KHz offset : –110 dBc/Hz

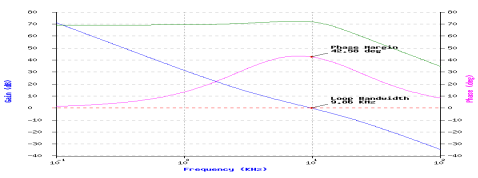
Tuning Voltage : 0.5-4.5 Vdc

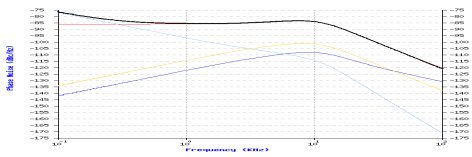
Supply Voltage : 5 Vdc

Operating temp. range : –40 to 85 oC

III. SIMULATION OF PLL LOOP

Simulation of the PLL loop is carried out with the help of tool provided by National Semiconductor Website "WEBBENCH". It helps me to finalize the values of loop filter components and analyze my design for Lock time, phase noise and loop stability consideration.





Phase Noise

IV. DESIGN OF PHASE LOCK OSCILLATOR

The RF front end is using for frequency translation. Phase locked oscillator (PLO) is providing Local oscillator (LO) frequency for frequency translation. Design includes two local oscillator frequencies at 1430 MHz and at 760 MHz for up-down converter. During the technical survey, it is found that instead of designing one separate PLO, both the LO frequencies by using single integer PLL chip Supplied by National Semiconductor which reduce size as well as power also. By this approach, a single reference oscillator can be used to generate both the LO frequencies

A. Required specifications for PLO

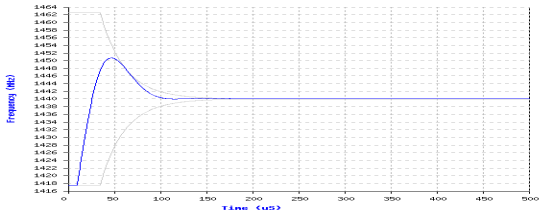
Freq. Range : 1430 Mhz fixed

Power Output : 8 dBm typical

Stability: 0. 1 ppm

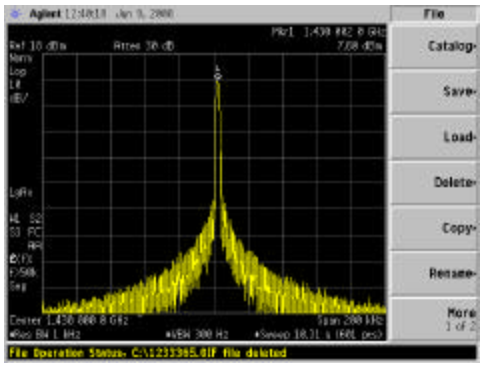
Phase noise: 80 dBc/Hz

Supply voltage: 12V

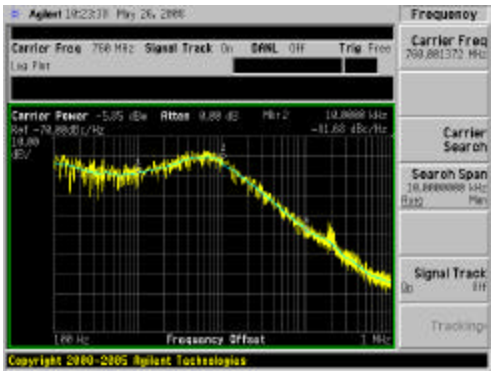


Lock Time

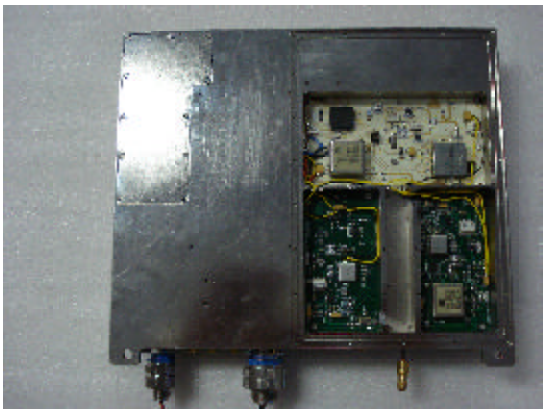
Output of spectrum analyzer for IF PLL



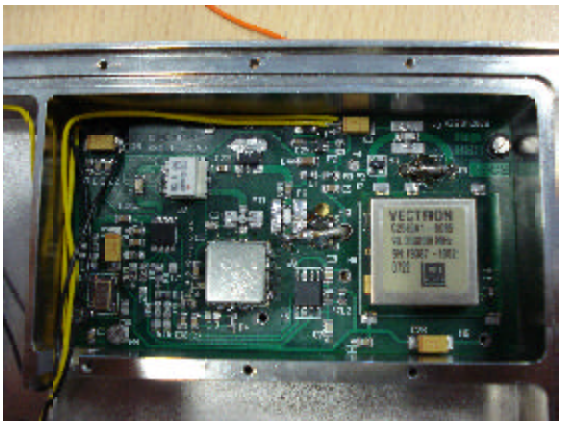
Output of spectrum analyzer for PLL



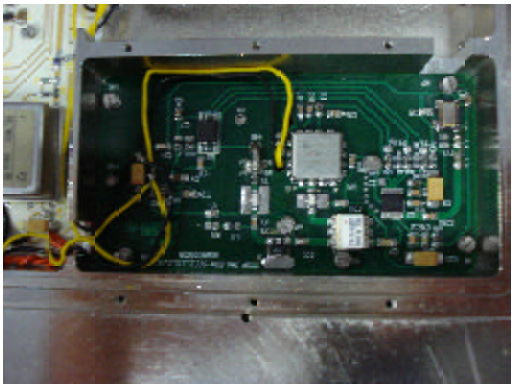
Combined inbuilt module of updown converter



Hardware for PLO at 1430 MHz



Hardware for PLO at 760 MHz



V. CONCLUSION

The aim was what the present day, and future, technology is intended to be; smaller and simpler. In contrast to the present day systems, the airborne system designed is of a much greater caliber. Today where bulky communication systems end up taking a lot of space on the aircraft, this system promises to reduce the load and provide a more reliable and efficient means of monitoring the communication system.

To design a frequency synthesizer for airborne application using surface mount components. Code loader software was used to load the registers of the PLL chip. The output obtained through the spectrum analyzer measured the phase noise –81 dBc/Hz at 10 kHz away from the carrier. Power output obtained was 7.5 dBm. The test results show suppressed reference spurs.

We have substituted the code loader software with a Microcontroller ATtiny13, which includes source code program developed using Code Vision C Compiler so that this PLL chip can be used in embedded systems for communication applications. Potential applications of the PLL include up-converters and down-converters to provide local oscillator frequency to the mixer. These mixers up-convert the IF signal to RF signal in up-converters and down convert the RF signal to IF signal in down converters in satellite communication systems.

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