IMPACT: International Journal of Research in Engineering & Technology (IMPACT: IJRET)
ISSN(E): 2321-8843; ISSN(P): 2347-4599
Vol. 2, Issue 3, Mar 2014, 121-128

ANALYSIS OF LEAKAGE CURRENT IN EXTREMELY SCALED HfO_2 GATE STACK DEPOSITED BY ALD

SAVITA MAURYA, B. R. SINGH & M. RADHAKRISHNA

Division of Electronics & Microelectronics, Indian Institute of Information Technology, Allahabad, Uttar Pradesh, India

ABSTRACT

It has been observed that the atomic layer deposition (ALD) and electrical properties of high-K oxides are strongly influenced by interfacial sub oxide formation, making pre and post deposition surface preparation and annealing conditions important. In this paper, we present a systematic experimental study on the leakage behaviour of extremely scaled HfO2 gate stack on silicon, deposited using atomic layer deposition process. The impact of deposition temperature, pre and post annealing parameters and surface conditions on the leakage behaviour in both accumulation and inversion regions is presented.

KEYWORDS: ALD, Pre-Deposition Annealing, Post-Deposition

INTRODUCTION

The introduction of the paper should explain the nature of the problem, previous work, purpose, and the contribution of the paper. The contents of each section may be provided to understand easily about the paper. The ever increasing demand for high performance and low power CMOS integrated circuits has been met through evolutionary device scaling and/or increase in chip area. For scaling of classical MOS transistor, the critical dimensions that need to be engineered are the gate length, the gate oxide thickness, the depletion depths under the gate, the source/drain junction depths and steepness of source/drain profile for each new generation of technology. Although all these parameters must be scaled together in order to reduce various short channel effects (SCE) and to achieve reliable MOSFET performance, the one that requires immediate attention is the scaling of gate dielectric. Practical MOSFET's structures generally require that the gate dielectric thickness to be few percent of the channel length.

This means that for sub 45nm technology generation, the effective oxide thickness (EOT) of the traditional SiO_2 dielectric should be less than 1nm. In this miniscule regime, direct tunnelling, channel mobility, gate electrode material penetration and oxide breakdown become dominating factors in the device performance [1-3]. Direct tunneling of electrons through gate is so high that the power dissipation is inadmissible. Therefore it is necessary to replace SiO_2 as gate oxide. Replacing conventional SiO_2 gate oxides with higher dielectric constant is one of the best solutions. The elementary concept for using high dielectric constant materials is increasing the physical thickness of the oxide to reduce the direct tunnelling leakage current and improve the reliability as validated by different research groups [4-7].

Amongst the variety of high-k materials available hafnium based oxide family (HfO_2, $HfSiO_4$, and HfSiON) is most suitable for replacing SiO_2 as gate dielectric [3-12]. However, there are several other issues such as carrier mobility degradation in the Si [7, 12], shift in threshold voltages, control of interfacial layers, high electronic defect density and tunnelling in extremely scaled interfacial layer, long term compatibility with Si and fixing of dielectric constant of oxide[1,12] needs to be addressed while replacing SiO_2 with hafnium based oxide family.

The present paper deals with the optimization of HfO_2 deposition by ALD process. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics have been used to characterize MOS capacitors. The impact of various process parameters like deposition temperature, surface treatment, and pre and post deposition annealing on leakage behaviour of HfO2/Silicon interface is presented. The structural characterization of HfO_2 /Si interface has been carried out using SEM/TEM to support our findings.

EXPERIMENTAL

P-type <100> silicon wafers with resistivity of 0.1–0.5Ω cm were used in the present investigation. Standard RCA process was used for cleaning the substrates. In view of the dependence of atomic layer deposition (ALD) process on surface conditions, various surface treatments such as thermal annealing in nitrogen and HF-treatment of the Si-wafers immediately prior to the ALD were tried. High-k hafnium di-oxide films were deposited in a commercial ALD reactor (Beneq TFS200). Tetrakis [Ethyl Methyl Amino] Hafnium, $Hf[N(CH_3)(C_2H_5)]_4$ (TEMAHf) was used as organic precursor. The temperature of water source and metal precursor were maintained at 25°C and 80°C respectively. Deposition chamber pressure was maintained around 5 mbar and all depositions were carried out at this pressure. Nitrogen (N_2) was used as a carrier and purging gas.

The deposition was carried out at 300˚C. Deposition rate of HfO_2 oxide film was 1A˚/cycle. Number of reaction cycle was chosen in order to achieve HfO_2 thickness in the range of 7nm to 20nm. After the deposition film thicknesses were measured using Sopra GES 5E spectroscopic ellipsometer. Metal oxide semiconductor (MOS) capacitors were fabricated with different electrode sizes varying from 40 X 50 μm^2 to 120 X 130 μm^2 using Al as top electrode and AlSi (1%) as backside metal contact. DC magnetron sputtering technique (Pfeiffer SPIDER 600) was employed to deposit aluminum electrodes using 99.9995% pure aluminum target. Argon (Ar) gas flow was maintained around 5 sccm during all sputtering depositions. Scanning electron microscope (Zeiss LEO 1550), and a Dual Beam SEM / FIB combined with ultra-high resolution field emission Scanning Electron Microscopy (SEM) and precise Focused Ion Beam (FIB) etch (Nova 600) were used to study the interfacial layer formed at the interface of Si wafer and HfO_2. Tencor Alpha-Step 500, surface profiler and AMBios XP 100 were used for measuring surface profile and step coverage.

The current-voltage (I-V) and capacitance–voltage (C–V) at 1 MHz were measured in a Cascade probe station using Agilent Semiconductor Parameter Analyzer, Keithley 4200 semiconductor-analysis systems. For crystalline structural studies we have used grazing incidence X-ray diffraction (GI XRD) analysis. CuKα radiation with a wavelength of 0.154nm was used for analysis. In the case of very thin films and/ or weaker crystalline states, grazing incidence geometry improves the sensitivity of measurements. Incidence angle is small and fixed. By fixing small incidence angle along with 2θ scan facilitate high signal from the thin film material and eliminates signal from the substrate material. In this study GI XRD scans were performed at incidence angles of 0.3°–0.5°.

RESULTS AND DISCUSSIONS

ALD is a film deposition technique based on sequential use of self-terminating gas-solid precursors and requires a minimum number of deposition cycles to achieve the desired oxide film thickness. Cross sectional SEM/FIB image of the HfO_2/ Si interface is shown in “Figure 1”. A clean interface between silicon and HfO_2 can be seen from the microphotograph. However there appears to be monolayer in between the HfO_2 and Si, its composition cannot be predicted on the basis of only SEM characterization. It is seen and verified by many authors [13, 14] that there is formation of

interfacial layer during ALD deposition of HfO_2, presumably formed by chemical interaction between ALD deposited HfO_2 and the Si Substrate [15].

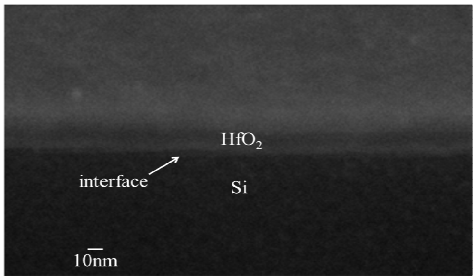


Figure 1: Cross-Sectional SEM/FIB Image of HfO_2/ Si Interface

Silicon wafer surface preparation plays an important role during initial phase of the film deposition. In view of this, various surface treatments have been attempted to investigate its role on the ALD process and electrical behaviour of the deposited film. In this sequence, various pre deposition annealing of the Si wafer have been performed to prepare the surface for ALD deposition. We first examined the effect of different pre-deposition annealing treatments for the HfO2 oxide film having physical thickness in the range of 7-20 nm. Three different pre-annealing temperatures 150°C, 350°C and 500°C and two different post annealing temperatures 350°C and 500°C have been used in the experimental study. To analyze the effect of different annealing temperatures, the deposition temperature of 300°C was kept constant and the leakage current was measured with positive and negative bias voltages. Three positive bias voltages i.e. 0.5, 1.0, 1.5V and three negative bias voltages i.e. -0.5, -1.0 and -1.5V have been used to measure the current.

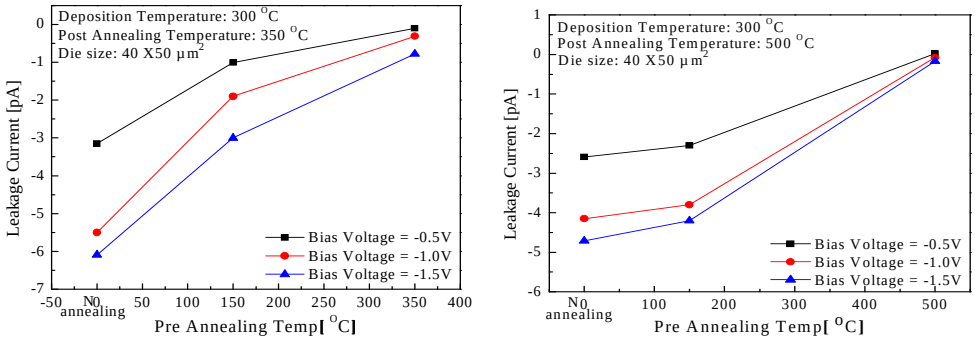


Figure 2: Comparison in Negative Voltage Bias Region of No Annealing with Pre-Deposition Annealing (a) at 150°C and 350°C (Post Deposition Anneal at 350°C) (b) at 150 °C and 500 °C (Post Deposition Anneal at 500°C)

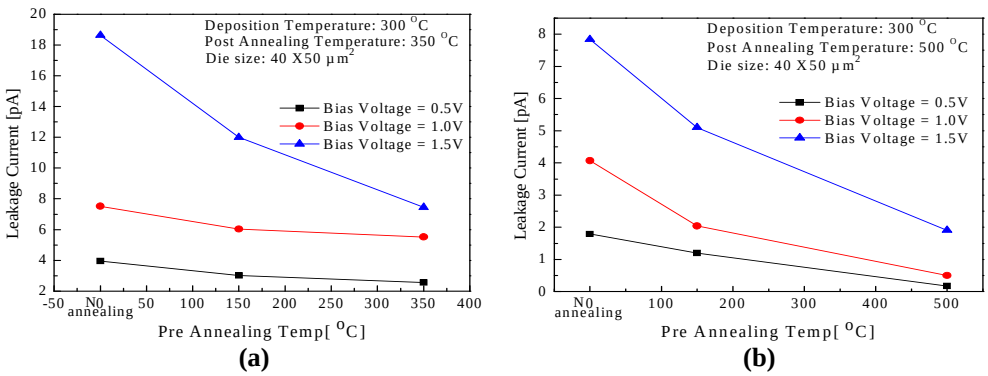


Figure 3: Comparison in Positive Voltage Bias Region of No Annealing with Pre-Deposition Annealing (a) at 150°C and 350°C (Post Deposition Anneal at 350°C) (b) at 150 °C and 500 °C (Post Deposition Anneal at 500°C)

It is apparent from "Figure 2" and "Figure 3" that pre deposition annealing decreases the leakage current of gate stack significantly. Pre annealing in nitrogen ambient activates the wafer surface that seemingly reduces the nucleation at initial stages of ALD deposition [13, 14, 16, 17]. Probably this is one of the reasons behind improved leakage behaviour of pre annealed wafers. Leakage current behaviour also improves with the increase in pre annealing temperatures from 150°C to 350°C and then to 500°C [18]. XRR analysis shows that improvement in the leakage behaviour is not on the account of thickening of interface layer. It further supports our assumption of nucleation formation at initial deposition stage. Apparently with increase in the temperature of pre wafer treatment, time to nucleation and island formation decreases which contributes to the improvement of leakage current behaviour.

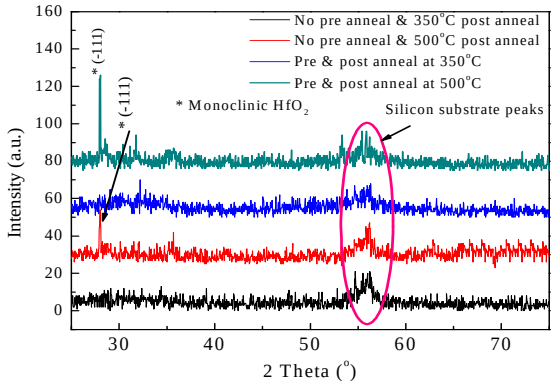
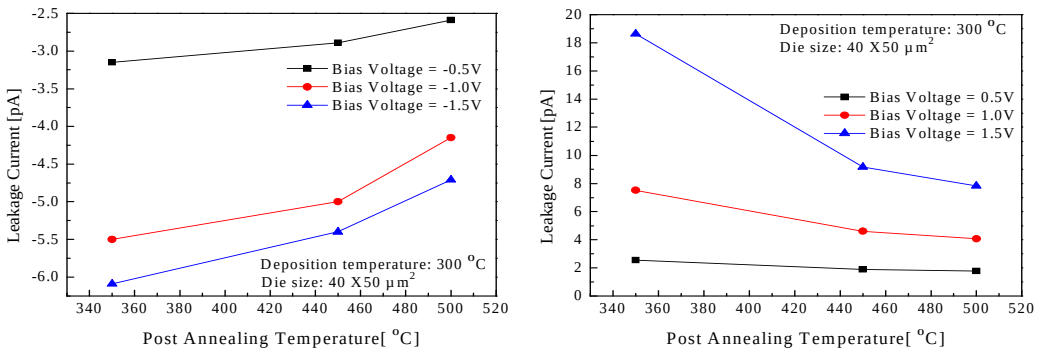


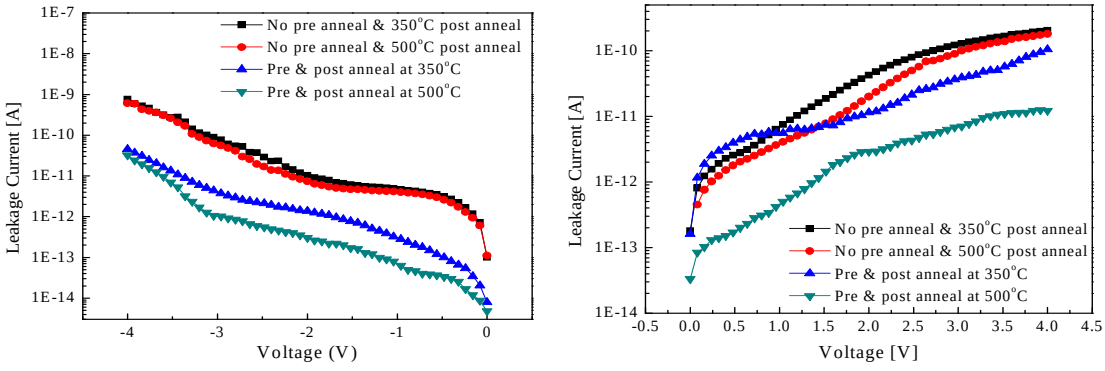
Figure 4: X-Ray Diffraction Patterns of HfO_2 Thin Film for Various Process Treatments

"Figure 4" shows GI XRD patterns for different process treatments. It is apparent from the graph that pre and post annealing at 350˚C does not affect the crystalline state of the deposited HfO_2 thin film and the films are amorphous. Whereas for the thin film oxides which were subject to post deposition anneal at relatively higher temperature of 500°C started to be crystalline. State of the film was found to be monoclinic after post deposition anneal at 500°C. It can also be concluded from the XRD pattern that pre deposition anneal of wafer does not have any significant effect on the crystalline state of the deposited oxide. Some of the samples were post annealed in nitrogen ambient for 1 hour. The effect of post deposition annealing temperatures (350°C, 450 and 500°C) on the leakage behaviour is shown in "Figure 5". No pre deposition annealing was carried out in this case. It can be seen from the "Figure 5" that leakage current decreases with the increase in the post deposition annealing temperature. The leakage current of the HfO_2 oxide film, post annealed at 500°C, is lower in comparison to the oxide films post annealed at 350°C and 450°C.



(a) **(b)**

Figure 5: Comparison of Different Post Deposition Annealing at 350, 450 and 500°C (a) Negative Voltage Bias (b) Positive Voltage Bias



(a) **(b)**

Figure 6: Comparison of Measured Leakage Currents for 7nm HfO_2 Layer, for a MOS Capacitor of 40x50µm^2 (a) Negative Voltage Bias (b) Positive Voltage Bias

"Figure 6" show the plot of leakage current as a function of voltage measured for different processing conditions. For positive bias voltages, leakage current measurement was carried out in the range of 0 to 4V and for negative bias, 0 to- 4V were applied. The sample for which pre and post deposition annealing at 500˚C were carried out seems to be the most consistent as far as leakage behavior is concerned.

This can be explained on the basis of experimental findings on activation of surface for ALD reactants by pre deposition annealing, rearrangement and repair of dangling bonds, change in crystalline state and formation of interfacial layer induced by the post deposition annealing [19, 20, 21, 22]. In our case, probably, pre deposition annealing at 500 °C is responsible for the activation of the wafer surface for ALD precursors. This probably resulted in reduced nucleation time and there is very little formation, or even no formation of island structures at initial stages. During the post deposition annealing at 500 °C, rearrangement and repairing of the dangling bonds take place also film start crystallizing that contributes to the improved film quality and the leakage current behaviour for oxide film subject to pre and post annealed at 500˚C.

CONCLUSIONS

HfO_2 thin oxides were grown on a pre-conditioned p-Si (100) substrate using TEMAHf as Hafnium precursor and H_2O as oxidant. A number of experiments were carried out to optimize the process parameters for the deposition of HfO2 having good electrical behaviour. All the films were deposited at 300˚C. To pre-condition the Si substrate, different pre-annealing (150 °C to 500 °C) temperatures were tried after RCA cleaning of Si substrate and just before the oxide deposition. Different post annealing temperatures in the range of 300°C to 500°C were also tried. It is found that the oxide for which pre and post annealing at 500°C were tried exhibit excellent leakage current behaviour.

ACKNOWLEDGEMENTS

The partial work reported in this paper, namely the fabrication of the device including optimization of the process flow, annealing and deposition conditions and the characterization of the device were carried out by Savita at EPFL with the support of ISJRP, under a joint research project of EPFL, Switzerland and IIIT, Allahabad, India. Special mention is needed for Mr Philippe Renaud, Director CMI who has very generously made available all the facilities of their laboratories and to Mr. Didier Bouvet, Ms Sara Rigante, Dr M Kayal and A M Ionescu for his insightful discussions on the selection of process parameters and modified conditions of ALD.

REFERENCES

1. M. L. Green, E. P. Gusev, R. Degraeve, and E. Garfunkel, Ultrathin (4 nm) SiO_2 and Si–O–N Gate Dielectrics Layers for Silicon Microelectronics: "Understanding the Processing, Structure and Physical and Electrical Limits," *Journal of Applied Physics (Rev). 90*, 2057 (2001).
2. M. Lukosius, Ch. Walczyk, M. Fraschke, D. Wolansky, H. Richter, Ch. Wenger, High performance metal–insulator–metal capacitors with atomic vapor deposited HfO_2 dielectrics, *Thin Solid Films, Volume 518, Issue 15*, 31 May 2010, Pages 4380-4384.
3. B. H. Lee, L Kang, R Nieh, W J Qi, J C Lee, Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing, *Applied Physics Letters, vol.76, no.14*, pp.1926-1928, Apr 2000.
4. H. Y. Yang, H. Niimi, and G. Lucovsky, Tunneling currents through ultrathin oxide/nitride dual layer gate dielectrics for advanced micro-electronic devices, *Journal of Applied Physics, vol. 83*, no. 4, pp. 2327–2337, Feb. 1998.
5. R. K. Pandey, K. V. R. M. Murali, S. S. Furkay, P. J. Oldiges, and E. J. Nowak, Crystallographic-orientation-dependent gate-induced drain leakage in nanoscale MOSFETs, *IEEE Trans. Electron Devices, vol. 57, no. 9*, pp. 2098–2105, Sep. 2010.
6. C.K. Maiti, S. Maikap, S. Chatterjee, S.K. Nandi, S.K. Samanta, Hafnium oxide gate dielectric for strained-Si1−xGex, *Solid-State Electronics, Volume 47, Issue 11*, November 2003, Pages 1995-2000.
7. Ando, Takashi; Copel, Matt; Bruley, John; Frank, Martin M.; Watanabe, Heiji; Narayanan, Vijay, Physical origins of mobility degradation in extremely scaled SiO_2/HfO_2 gate stacks with La and Al induced dipoles, *Applied Physics Letters, vol.96*, no.13, pp.132904-132904-3, Mar 2010.
8. H. Kim, P. C. McIntyre, C. O. Chui, K. C. Saraswat, and S. Stemmer, "Engineering chemically abrupt high-k metal oxide/silicon interfaces using an oxygen-guttering metal over layer, *Journal of Applied Physics, vol. 96*, no. 6, pp. 3467–3472, Sep. 2004.
9. X.F. Wang, Quan Li, P.F. Lee, J.Y. Dai, X.G. Gong, Characterization of the interface between the Hf-based high-k thin film and the Si using spatially resolved electron energy-loss spectroscopy, *Micron, Volume 41, Issue 1*, January 2010, Pages 15-19.
10. Y. Kamata, High-k/Ge MOSFETs for future nanoelectronics, *Materials Today, Volume 11, Issues 1–2*, January–February 2008, Pages 30-38.
11. L Nyns, L Ragnarsson, L Hall, A Delabie, M. Heyns, S V Elshocht, C Vinckier, P Zimmerman, S De Gendt, Atomic Layer Deposition of HfO_2 on (100) and (110) Oriented Silicon Surfaces, *ECS Transactions vol: 11 issue:4* pages:73-77, 2007.
12. W. Zhu, J. P. Han, T. P. Ma, Mobility Measurement and Degradation Mechanisms of MOSFETs made with ultrathin high-k dielectrics, *IEEE Transactions on Electron Devices, vol. 51, no. 1*, January 2004, pp 98-105.

13. J Kim, T W Kim, Initial surface reactions of atomic layer deposition, *Journal of the Minerals, Metals and Materials Society, Volume 61*, Number 6, 2009.

14. D. H. Triyoso, R. I. Hegde, B. E. White, P. J. Tobin, Physical and electrical characteristics of atomic-layer-deposited hafnium dioxide formed using hafnium tetrachloride and tetrakis (ethyl-methyl-amino hafnium), *Journal of Applied Physics, vol.97, no.12,* pp.124107-124107-9, Jun 2005.

15. Moonju Cho, Doo Seok Jeong, Jaehoo Park, Hong Bae Park, Suk Woo Lee, Tae Joo Park, Cheol Seong Hwang, Gi Hoon Jang, and Jaehack Jeong, Comparison between atomic-layer-deposited HfO_2 films using O_3 or H_2O oxidant and $Hf[N(CH_3)_2]_4$ precursor, *Applied Physics Letters 85,* 5953 (2004),

16. R. L. Puurunen1, W. Vandervorst1, W. F. A. Besling, O. Richard, H. Bender, T. Conard, C. Zhao, A Delabie, M Caymax, S De Gendt, M Heyns, M. M. Viitanen, M. de Ridder, H. H. Brongersma, Y Tamminga, T Dao, T de Win, M Verheijen, M Kaiser and M Tuominen, Island growth in the atomic layer deposition of zirconium oxide and aluminum oxide on hydrogen-terminated silicon: Growth mode modeling and transmission electron microscopy, *Journal of Applied Physics, vol.96, no.9,* pp.4878-4889, Nov 2004.

17. S. Maurya, B. R. Singh, M. Radhakrishna, Effect of pre-deposition annealing on the performance of MIS capacitor formed using atomic layer deposition of ultrathin HfO_2, *AIP Conference Proceedings, 1536,* 1159-1160 (2013).

18. W. Hei, H. Iwai, K. Kakushima, Material and interface instabilities of high-κ MOS gate dielectric films, *Nano CMOS, 2006 International Workshop on, vol., no.,* pp.169-174, Jan. 30 2006-Feb. 1 2006.

19. W. E. Fu, Y. Q. Chang, Layer structure variations of ultra-thin HfO_2 films induced by post-deposition annealing, *Applied Surface Science, Volume 257, Issue 17,* 15 June 2011, Pages 7436-7442.

20. H Wong, The Current Conduction issues in High-k Gate Dielectrics, *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on, vol., no.,* pp.31-36, 20-22 Dec. 2007.

21. J.Y. Son, W.J. Maeng, Woo-Hee Kim, Y.H. Shin, Hyungjun Kim, Interface roughness effect between gate oxide and metal gate on dielectric property, *Thin Solid Films, Volume 517, Issue 14,* 29 May 2009, Pages 3892-3895.

22. Y. K Chiou, C. H. Chang and T. B. Wu, Characteristics of hafnium oxide grown on silicon by atomic-layer deposition using tetrakis (ethylmethylamino)hafnium and water vapor as precursors, *Journal of Materials Research, Vol 22, No 7,* July 2007, pp 1899-1906.