Recovery of Microwave-Digital Signal Integrity with NGD Circuits

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Abstract

This paper presents an equalization technique of analogue-digital or mixed signals disturbed by electromagnetic interference (EMI) and electromagnetic compatibility (EMC) effects by using negative group delay (NGD) circuit. The basic principle illustrating the mechanism of the equalization technique thanks to the NGD function is explained. To illustrate the efficiency of the technique understudy, an equalization of RC-effect is performed. According to the frequency- and time-domain analyses, a possibility of the distorted signal reconstruction is demonstrated experimentally and by simulations. To confirm the proposed technique efficiency and reliability, the reduction of rise-/fall-time and propagation delay in relative value more than 90 % is performed by using trapezoidal signal with 1 Gbit/s-rate. It is stated that this technique allows reducing the signal delays. The technique proposed is useful for the microelectronic systems application.

Keywords

Negative Group Delay (NGD); Signal Integrity (SI); Equalization Technique; Electrical Interconnect; RC-Model

Introduction

The need of numerical electronic industries requires the development of digital systems operating higher in digital rate. Such an effect is fundamentally accompanied by signal with very wide spectrum from DC up to microwave frequency ranges and necessitates then further investigation on the electromagnetic interference (EMI). This later can generate undesired coupling effect. In order to take into account such an effect during the design process different computation methods and simulation techniques were developed. This allows for example to investigate the EMI and electromagnetic compatibility (EMC) phenomena associated with the signal integrity (SI) analysis in the microelectronic and integrated circuits. In this scope, it is worth noting that the interconnect effect become one of the major bottlenecks of current microelectronic structures. Because of the continuous increase of operating frequency with the circuit size global shrinking, the interconnect reflections, crosstalk, attenuation and delays are no longer negligible.

In the current VLSI circuits, the interconnect delay dominates widely the logic propagation delay. To enhance the system performance, we propose to introduce an equalization technique based on the use of negative group delay (NGD) circuit. We voluntarily chose the RC-circuit as disturbing system to be compensated because of its universal use as line, interconnect and channel modelling. Moreover, thanks to the simplicity of this disturbing circuit and the NGD circuit proposed, analytical demonstrations of the NGD behaviour and of the compensation technique is given. The NGD effects have been validated several times theoretically and experimentally in electronic areas. It was confirmed that this counterintuitive physical phenomenon does not forbid the causality principle [16-18]. Thanks to the NGD topology using a field effect transistor (FET), higher potentially applicable NGD circuits were developed more recently. By exploiting the topology introduced in [19], an equalization technique of the RC-effect perturbations is proposed in this paper.

For the better understanding, this paper is organized as follows. The basic principle of the equalization proposed based on the basis of transfer function and group delay parameters are outlined in Section 2. A mathematical description which highlights the interaction between the RC-model and an NGD-circuit is explained in Section 3. Then, the RCNGD-circuit parameters will be analysed and extracted. Furthermore, it will be shown also how the

cancellation of RC-circuit delay can be realized. Section 4 presents the verification results illustrating the feasibility of the equalization investigated showing the SI improvement. Finally, Section 5 draws the conclusion.

Principle of the Equalization Technique Proposed

The main objective of the equalization presented in this paper is to minimize the undesired effects of the given disturbing structure by using an NGD circuit. The block diagram shown in Fig. 1 illustrates the implementation of the equalization technique proposed. In other words, the compensation principle is simply an equalization of the disturbing circuit transfer function, noted $G_p(s)$ by that of NGD circuit, $G_{NGD}(s)$.

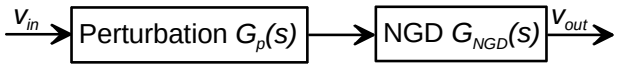

FIG. 1 BLOCK DIAGRAM ILLUSTRATING THE EQUALIZATION PRINCIPLE WITH NGD CIRCUIT

It means that in ideal condition, the transfer function of the whole system introduced in Fig. 1 is written as follows:

$$G(s) = \frac{V_{out}(s)}{V_{in}(s)} = G_p(s) \cdot G_{NGD}(s) \quad (1)$$

must be close to unity. The passive devices show a frequency magnitude response $|G_p(j\omega)|$ and a positive group delay $\tau_p(\omega)$ whose behaviour are depicted in Fig. 2. Thus, $G_{NGD}(s)$ should behave as a complement of $G_p(s)$, and provides gain and a negative group delay shown in Fig. 2:

$$|G_{NGD}(j\omega)| > 1, \quad (2)$$

and

$$\tau_{NGD}(\omega) = -\frac{\partial \angle G_{NGD}(j\omega)}{\partial \omega} < 1, \quad (3)$$

where $j = \sqrt{-1}$ and ω is the angular frequency. On condition that the proposed topology is able to fulfill a sufficient gain and NGD for the specified frequency band, for the whole circuit, the gain and the group delay depicted in Fig. 2 are expected. To highlight the functioning of this equalization technique, a compensation example with elementary circuits will be examined in the remainder of this paper.

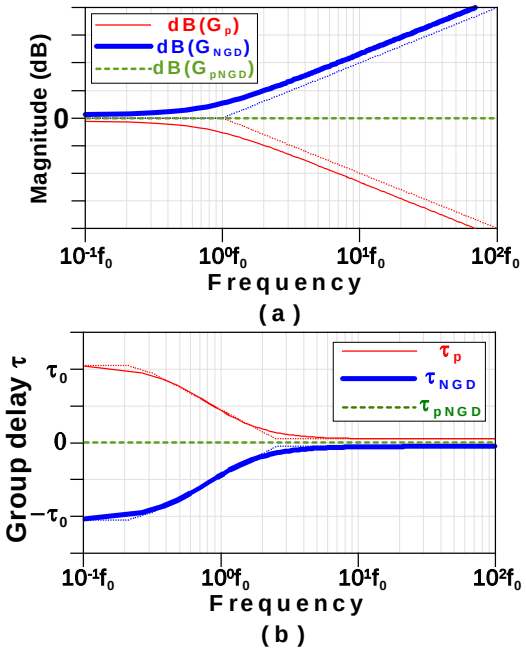

FIG. 2 BEHAVIOURS OF GAIN AND GROUP DELAY OF THE CORRECTED IDEAL SYSTEM ILLUSTRATING THE EQUALIZATION PRINCIPLE WITH NGD CIRCUIT

Analytical Investigation on the Rc Effect Equalization With Ngd Circuit

More concretely, the equalization principle consists in ending the disturbing effect to be compensated, here represented by the RC circuit, by an NDG circuit as depicted in Fig. 3.

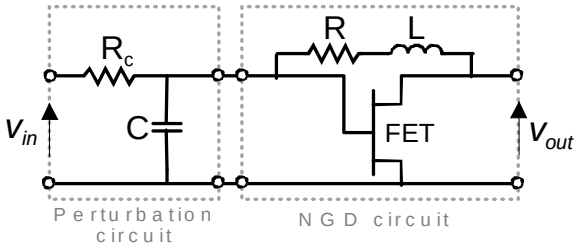

FIG. 3 RC-CIRCUIT (PERTURBATION) CASCADED WITH AN NGD ACTIVE CIRCUIT

Transfer Function Analysis

The transfer function and the static gain at low frequency of the whole circuit introduced in Fig. 5 are respectively denoted as:

$$G(s) = \frac{R_{ds}(1 - g_m R) - g_m R_{ds} L s}{R + R_{ds} + R_c(1 + g_m R_{ds}) + [R_c C(R + R_{ds}) + L]s + R_c C L s^2}, \quad (4)$$

$$G(0) = \frac{R_{ds}(1 - g_m R)}{R + R_{ds} + R_c(1 + g_m R_{ds})}. \quad (5)$$

Due to the unmatched effect between these RC- and NGD-circuit, this transfer function, G is not equal to the product, G_{rc} x G_{NGD}. This remark also applies to group delay:

$$\left|G(j\omega)\right| \neq \left|G_{rc}(j\omega)\right| \times \left|G_{NGD}(j\omega)\right|, \quad (6)$$

and

$$\tau(\omega) \neq \tau_{RC}(\omega) + \tau_{NGD}(\omega). \quad (7)$$

For the sake of mathematical simplification, let us consider the normalized canonical form $g = G/G(0)$ defined by:

$$g(s) = \frac{\alpha_0 + \alpha_1 s}{s + 2\zeta\omega_n s + \omega_n^2}, \quad (8)$$

where the coefficients are written as:

$$\alpha_0 = \frac{R_{ds}(1 - g_m R)}{R_c CL}, \quad (9)$$

$$\alpha_1 = \frac{-g_m R_{ds} L}{R_c CL}, \quad (10)$$

$$\omega_n = \sqrt{\frac{R + R_{ds} + R_c(1 + g_m R_{ds})}{R_c CL}}, \quad (11)$$

and

$$\zeta = \frac{R_c C(R + R_{ds}) + L}{2\sqrt{R_c CL\left[R + R_{ds} + R_c(1 + g_m R_{ds})\right]}}. \quad (12)$$

By considering this simplified transfer function, it is worth verifying the intrinsic stability of this active circuit, which can be done by studying the characteristic equation. According to the Routh-Hurwitz array, the first column indicates clearly that the real parts of the polynomial roots are always negative. Under these conditions, i.e. a simplified FET model with no additionnal RF/microwave/chip elements, the system is always stable.

Synthesis of the NGD Circuit in Function of the RC-Parameters

As the equalization principle consists in restitution of an output signal equal or close to the input one, the transfer function magnitude and group delay should be respectively almost equal to unity and null. In a simplifying purpose, one can apply these conditions at very low frequency:

$$\left|G(0)\right| \approx 1 \text{ and } \tau(0) \approx 0, \quad (13)$$

to get the following synthesis relations:

$$R = \frac{2R_{ds} + (g_m R_{ds} + 1)R_c}{g_m R_{ds} - 1}, \quad (14)$$

and

$$L = \frac{(g_m R - 1)(R + R_{ds})R_c C}{g_m^2 R_{ds} R_c + g_m(R_{ds} + R_c) + 1}. \quad (15)$$

To avoid the change of the output voltage sign at the end of the NGD circuit due to the Drain-Source current direction, one can use two stage NGD cells as displayed in Fig. 4.

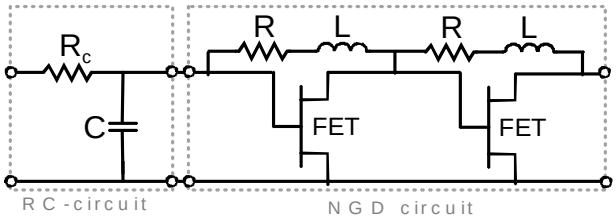

FIG. 4 RCNGD CIRCUIT: RC-CIRCUIT CASCADED WITH TWO-STAGE IDENTICAL NGD CELL

In this case, analytical investigation conducts to synthesis expressions of R and L parameters of the NGD circuit proposed in (16) and (17).

$$R = \frac{R_c + 3R_{ds} + \sqrt{R_c^2 + 2(4g_m R_{ds} - 1)R_{ds} R_c + 9R_{ds}^2}}{2(g_m R_{ds} - 1)}, \quad (16)$$

$$L = \frac{R_c C(g_m R_{ds} - 1)[R^2 + R_{ds} R(3 + g_m R_{ds}) + R_{ds}^2]}{(g_m R_{ds} + 1)\left[(g_m R_{ds} + 2) + g_m R_c\right]R + (4g_m^2 R_{ds}^2 + 5g_m R_{ds} + 1)R_c + 3R_{ds}(1 + g_m R_{ds})}. \quad (17)$$

Somehow, long interconnections are used for the complicated IC. In this case, certain number of NGD cells is necessary to correct such an effect. The following paragraph introduces the determination of the NGD cells number in function of the RC-parameters.

Synthesis of the NGD Circuit Order in Function of the RC-Parameters

At the end of the input pulse, when $t = T$, the RC circuit introduces a significant attenuation:

$$\left|v_{rc}(T)/V\right| = 1 - \exp(\frac{-T}{\tau_0}) << 1, \quad (18)$$

one stage of FET may be insufficient to compensate for the losses. In this case, the maximal gain value for an NGD cell is equal to:

$$G_{\max} = g_m R_{ds}. \quad (19)$$

We can get the number of cells, n, necessary to generate a whole gain approximately close to unity:

$$\left|\frac{V_{rc}(T)}{V}\right| \cdot G_{\max}^{n} \approx 1 \qquad (20)$$

This equation leads to the following expression of the number of the NGD cells in function of the delay, operating signal rate and also the employed transistor characteristics:

$$n \approx 1 + \mathrm{int}\left\{-\frac{\ln\left[1-\exp\left(-T/\tau_0\right)\right]}{\ln\left(g_m R_{ds}\right)}\right\} \qquad (21)$$

where for a real x, the function int(x) indicates the greatest integer equal or lower than x. I point out that NGD circuits comprised of two or an even number of transistors may be preferably implemented to avoid signal inversion if required in considered applications.

Simulation and Experimental Validations of the Equalization Technique under Study

The Following the previous section remarks and synthesis relations, this section describes the design process of an NGD prototype. Simulations using the most accurate available models are run under Advanced Design System (ADS) circuit simulator software from Agilent™, combined with a sensitivity analysis. The experimental results in frequency- and time-domains validate the entire compensation procedure.

Experimental Investigation

The aim of this demonstrator is to illustrate and visualize the reconstitution of the degraded signal. So, for a given data rate, 25 Msym/s, we choose RC values that highly degrade the input signal while keeping them in the range value of line or interconnect models. To carry out this experimental study, an RC-, an NGD-circuit and both associated (RCNGD-circuit) were designed and implemented (Fig. 5). The RCNGD circuit was manufactured instead of simply cascading RC by NGD to avoid mismatch due to 50 Ω connectors and transitions when joining the two circuits. To achieve broadband biasing and particularly to avoid the eventual disruptions caused by the bias network at low frequency, we bias the FET using a technique of improved active load technique. We choose a FET PHEMT - ATF-34143 provided by Avago Technology™, whose non linear model is available. Then, combining circuit simulation of the lumped components (non linear FET model) with electromagnetic simulations of the distributed parts using Momentum Environment of ADS (from Agilent™) delivers accurate frequency responses.

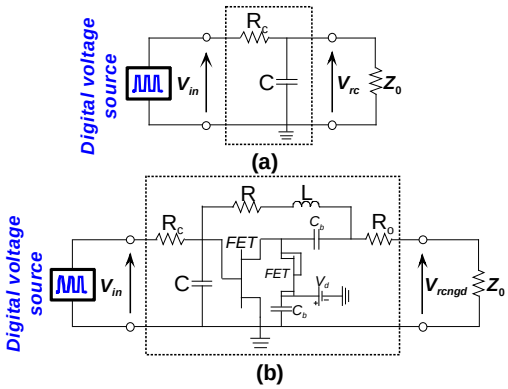

FIG. 5 SCHEMATICS OF THE (A) RC- AND (B) RCNGD-CIRCUITS INCLUDING BIASING NETWORK USING A FET = PHEMT ATF-34143 FOR R_C = 33Ω, C = 680 PF, AND R = 56 Ω, R_O = 10 Ω, L = 220 NH, C_B = 100 NF

These responses may be used in a final slight optimisation, in time domain, to choose the localized component values between those available. The layout of the hybrid planar circuit is printed on a FR4 substrate with a permittivity ε_r = 4.3 and a thickness, h = 800 µm, (layout and photograph in Figs. 6(b) and 6(a)). Finally, the surface-mount chip passive components R, L, and C are implemented on the substrate.

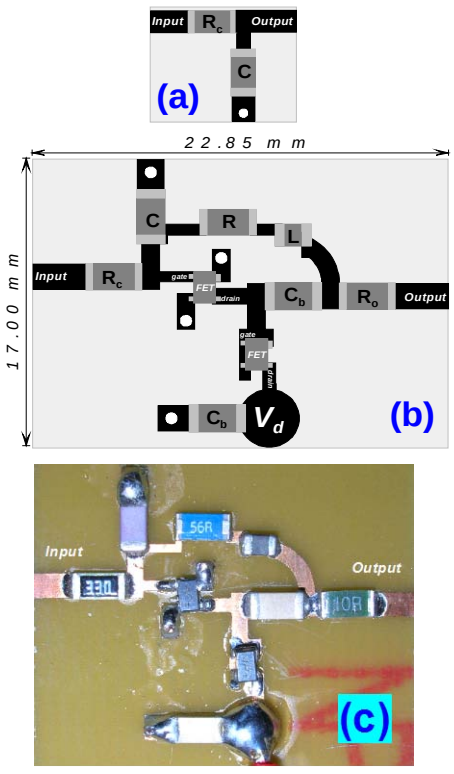

FIG. 6 LAYOUTS OF (A) THE RC- AND (B) THE RCNGD-CIRCUITS. (C) PHOTOGRAPH OF THE IMPLEMENTED RCNGD-CIRCUIT

1) *Sensitivity Analysis*

The simulations for the specifications and the conditions mentioned above (accurate models with combined circuit and electromagnetic simulations) are displayed respectively in Fig. 7 and Fig. 8 for frequency- and time-domains. Moreover, a sensitivity study of these responses versus the NGD element tolerance values (±5% around their nominal values R=56Ω and L=220nH) was carried out using a Monte-Carlos analysis over 10 trials. As shown in Figs. 7(a) and 7(b), the magnitude of the whole RCNGD-circuit is kept around 0 dB up to 40 MHz, and the corresponding group delay is strongly decreased from DC to 15 MHz compared to that of the RC-circuit. Moreover, the Monte-Carlos analysis highlights a weak dependence of the lumped tolerance values on the frequency responses.

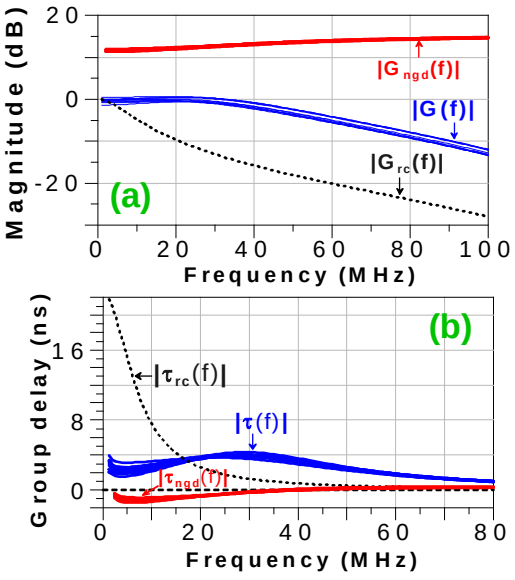

FIG. 7 (A) MAGNITUDE AND (B) GROUP DELAY SIMULATED FREQUENCY RESPONSES WITH A MONTE-CARLO ANALYSIS OF THE NGD CIRCUIT ELEMENTS R AND L (±5%)

First, we measured the signal at the output of the R& S Signal Generator SMJ 100A at the highest available rate, i.e. 25Msym/s and use it as the simulation input signal. Exciting the simulated RC- and RCNGD-circuit with this input square wave pulse with a magnitude, V_0 = 1 V, we get the time-domain simulations of Fig. 8.

The dashed curve indicates the degradation introduced by the RC-circuit. This temporal responses highlight that the signal recovery operates but the compensation is not complete. The 50% propagation delay is shortened from 16.5 ns (for the RC-circuit) to about 3 ns (RCNGD circuit), i.e. a relative reduction of more than 81%. The ±5%-variation of R and L do not change the front of the RCNGD-circuit output signal but it affects slightly its final value.

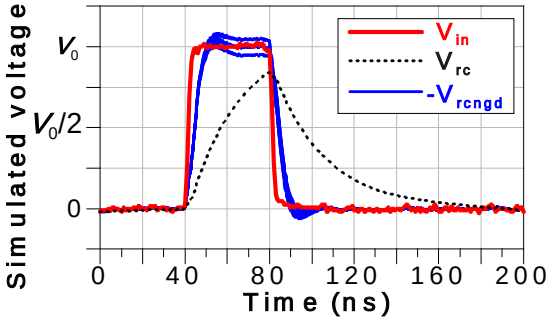

FIG. 8 TIME DOMAIN SIMULATED RESULTS (WITH A MONTE CARLO ANALYSIS OF THE NGD CIRCUIT ELEMENTS R AND L FOR THE ±5% RELATIVE VARIATION) FOR AN INPUT SQUARE WAVE PULSE (V_0 = 1 V WITH A 40 NS DURATION)

2) *Frequency and Time-Domain Measurements*

To fulfil a complete validation and to verify the theoretical predictions and simulation results, we have first tested the fabricated devices in frequency-domain and then in time-domain.

Frequency results: These measurements were made with a vector network analyzer that provides the scattering matrix of a two-port circuit (S-parameters). Consequently, we get the magnitude and the group delay (calculated from the phase of the transfer function) of the three implemented circuits (Fig. 9).

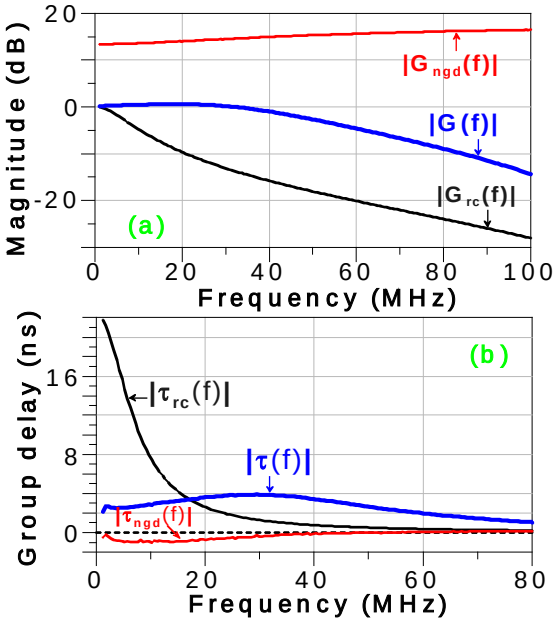

FIG. 9 (A) MEASURED MAGNITUDES AND (B) THE GROUP DELAYS OF THE RC-, NGD-CIRCUIT AND BOTH COMBINED

The measured magnitude of the overall circuit is kept within -10 dB and 0 dB up to 80 MHz and close to 0 up to 40MHz like in simulations. For the three circuits, magnitude and group delay responses both show a good agreement with the simulations of Fig. 7. As mentioned theoretically in previous section, it is worth noting that the total magnitude and delay values are different from the sum of the individual magnitudes because of mismatch between its two parts. The whole circuit group delay is not fully cancelled (Fig. 7(c)), but it is kept below 4 ns due to the NGD circuit. A higher NGD value could be achieved but a compromise between NGD value, NGD bandwidth and gain flatness has to be found to minimize overshoot or ripple in time-domain.

Time-domain results: Along this temporal study (in simulations and measurements), the tested circuit load, is settled to a high impedance value. The square wave pulse is delivered by the base band output of a vector signal generator (R&S SMJ 100A) using the highest rate available and recorded on a 2 Gs/s LeCroy™ digital oscilloscope. This digital pulse has a 25-Msym/s rate corresponding to a 40-ns width and an amplitude V_0 = 1V. To avoid cable and connector influences, we proceed systematically in two steps and recorded first the input and then the output signals using the same synchronization reference signal. Following that technique, we monitored the input pulse, vin, the RC- and RCNGD-circuit ones v_{rc}, v_{rcngd} which are resynchronized using the reference signal and plotted in Fig. 10. So, we observe that compared to v_{rc}, the output v_{rcngd} waveform is less distorted according to the input, v_{in}. We see in Fig. 10 that the RC-circuit provides a degraded output leading edge with a rise time and a 50 % propagation delay respectively of $t_r \approx 35\ ns$ and $T_{rc} \approx 18.50\ ns$. Hence, due to the NGD circuit compensation, these parameters were respectively reduced to $t_{rngd} \approx 10\ ns$ and $T_{rcngd} \approx 2.50\ ns$. It corresponds to a relative reduction $(1 - T_{rcngd} / T_{rc})$ and $(1 - t_{rngd} / t_r)$ of 71.4 % and 86.4 %. In addition, as illustrated in top of Fig. 10, an excellent improvement of the trailing edge is also achieved.

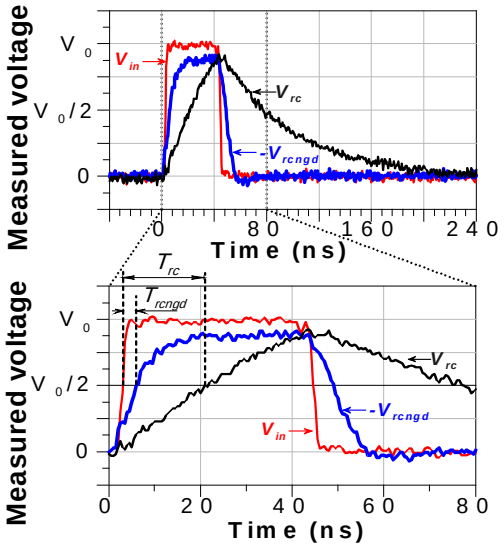

FIG. 10 TIME-DOMAIN RESPONSES WITH AN INPUT SQUARE WAVE WITH A 25-MSYM/S RATE, 2 NS RISE- AND FALL-TIMES AND ZOOM ON TWO TIMES OF THE SYMBOL DURATION

Application of the Equalization Technique with 1 Gbit/s Rate Data

Fig. 11 displays the two-stage simulated circuit allowing compensating the analogue-digital or mixed signal.

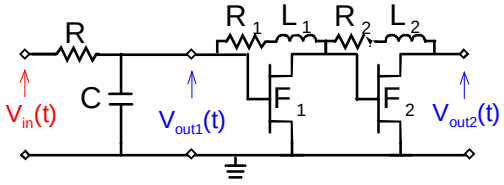

FIG. 11 TWO-STAGE OF NGD CIRCUIT COMPENSATING THE RC-CIRCUIT (R=200 Ω,C=4.3PF, R_1=100 Ω,R_2=130 Ω, L_1=12NH, L_2=9.1NH)

This former is represented by the trapezoidal signal with period with rise- and fall-time of T = 2 ns and 92 ps, respectively, degraded by the RC circuit. During the simulations, the employed FETs F_1 and F_2 are replaced by the pHEMT EC2612. We recall that this FET is characterized by the transcondutance g_m = 98.14 mS and the drain-source resistance R_{ds} = 116.8 Ω.

1) Frequency Results

Figs. 12 depict the frequency simulation results of the RC-perturbation, NGD circuit and both gathered for showing the equalization effect from DC to 3 GHz. As highlighted in Fig. 12(a), the magnitude of the RC-circuit presents attenuation almost 10 dB from 0.5 GHz. However, the magnitude of the NGD-circuit alone remains more than 13dB.

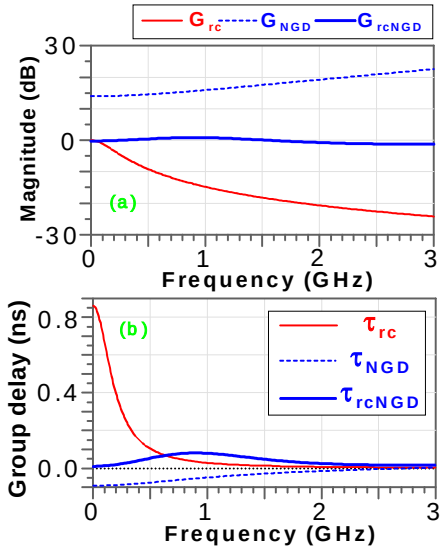

FIG. 12 MAGNITUDE AND GROUP DELAY OF THE RC-, NGD- AND RCNGD-CIRCUITS INTRODUCED IN FIG. 11

Consequently, both cascaded presents this last magnitude plotted in thick blue curve sandwiched in -1.2dB to 0.9dB. It is worth noting here that this last one is not equal to the sum of the two described previous one because of the mismatched between the two circuits as seen above ($G \neq G_{RC}.G_{NGD}$). For the group delay in Fig. 12(b), it is several hundred of ps below 0.3GHz. Because of that of the NGD circuit plotted in dashed blue curve, it is reduced under 80ps for the whole circuit. This effect traduces the equalization of the perturbation effects thanks to the NGD function and also the active gain. In the next point, we will see the consequence of this equalization on the periodical trapezoidal signal representing the mixed data through RC-circuit.

2) *Time-domain Results*

In this paragraph, we check an example of the feasibility of the equalization technique understudy regarding the analogue-digital data materialized by a periodical signal with rate 1 Gbit/s. Figs. 13 display the time domain response of the RC- and RCNGD-devices considered by using a periodical typically square wave inputs presenting a rate of 1 Gbit/s. As plotted in Fig. 13(a), due to the RC-disturbance, there is a marked signal distortion for the signal vout1 compared to v_{in} plotted in dashed blue- and plotted in red- curves, respectively.

After insertion of the NGD circuit, one obtains the improved output v_{out2} plotted in thick blue line. As explained by Fig. 13(b), this former presents a 50% propagation delay of about only 24 ps, meanwhile reduction more than 96 %. This states that the NGD effect is practically useful for the correction of the disturbances for the enhancement of the SI and even for the signal recovery.

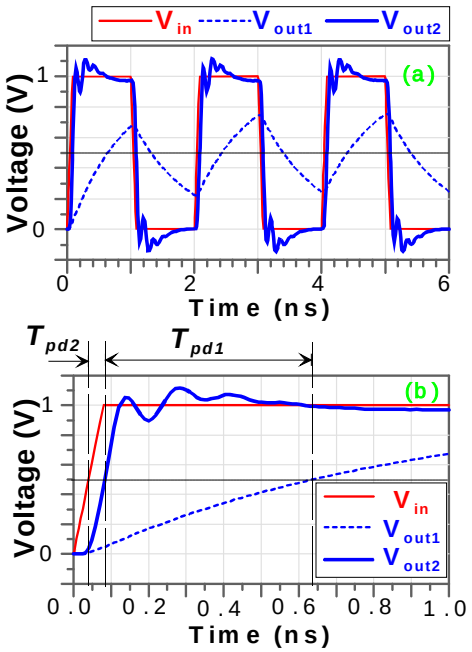

FIG. 13 TIME-DOMAIN RESPONSES OF THE CIRCUIT INTRODUCED IN FIG. 11 WITH TRAPEZOIDAL INPUT WITH PERIOD 2 NS, RISE- AND FALL-TIME 92 PS AND 50 % DUTY RATIO. REPRESENTATION IN (A) THREE PERIODS AND (B) IN ½-PERIODS

Conclusions

An equalization technique of the unintentional effects as EMI/EMC generated by interconnection network perturbations is introduced in this paper. The basic functioning of the technique was described. It is based on the cascade of the disturbing structure, in this case represented by the RC circuit, and an NGD circuit. The synthesis process of the NGD circuit in function of the RC-perturbations and also the operating signal rate is established. It was demonstrated that the possibility of the signal reconstitution is illustrated by theory and simulations. Experimental validations with sensitivity analyses both in frequency- and time-domain were presented. As expected, recovery of signal degraded is realized. Verifications made with frequency- and time-domain analyses confirm the relevance of the equalization technique proposed. Furthermore, analysis with 1 Gbit/s square wave analogue-digital input reveals that a signal recovery with the loss compensation and the delay cancellation was proved.

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