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0.5 V DC Suppression, Low Noise, High Impedance CCII-Based Electrocardiogram Amplifier

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Abstract: This paper presents the design of an electrocardiogram (ECG) front-end amplifier using two second generation current conveyors (CCII) based on the current-balancing instrumentation amplifier (CBIA) and five passive elements with the single supply at the transistor-level topology. Due to many disturbances for ECG measurement, the properties of proposed front-end CCII-based ECG amplifier are the DC suppression from electrode while measuring and to attenuate the power line interference at 50Hz asides from the ECG spectrum. The aim of this work is to design the single supply CCII-based ECG front-end amplifier circuit for the portable device. The proposed circuit was simulated at 0.35μ m CMOS technology model parameters. The experimental simulations with equivalent circuit model of electrode-tissue interface show that the proposed ECG amplifier verifies at ±0.5V DC suppression at 1%THD, a mid-band gain of 47 dB, Common Mode Rejection Ratio (CMRR) of 53 dB, input referred noise of 0.24μ Vrms@100Hz, input impedance of 280M\Omega and the power consumption of 66 μ W.

Keywords: Single supply circuit, Current conveyor (CC), ECG amplifier, Biopotential monitoring, Currentbalancing instrumentation amplifier (CBIA).

1. Introduction

The heart is an important engine of the human body. As the heart contracts and relaxes, an electric potential is generated. When considering the total electrical potential, an electrocardiogram (ECG) signal will be happened. Electricity generated at the heart is spread through the body in the form of an ionic current for measuring and recording ECGs for diagnosis. Hence, the electrodes should be placed for the standard contact with skin to obtain the largest and most clear signal. However, the measured vital potential is very small. Therefore, an amplifier circuit is an important to amplify the signal to be large enough for the signal transformation process.

Fig. 1 demonstrates the ECG measurement system with the vital signs voltage ranging between



Figure. 1 Block diagram of ECG measurement system

0.5 - 4 mV [1] which is measured by the electrode pads and sent into the front-end amplifier circuit. It has been commonly used as a low-noise instrumentation amplifier (IA) circuit. The amplified signal then passes through a low-pass filter (LPF) to select the specific ECG frequency before entering a variable gain amplifier (VGA) to obtain a value suitable for the dynamic range of analog-to-digital converter (ADC) before sending to various processing systems. The electrical potential of the vital signs measured by the electrode is very small and to be disturbed by the environment.

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Figure. 2 Motion artifact from electrode interface [1]

The front-end amplifier connected directly to the electrode is therefore an important part. So, the design of the front-end amplifier circuit must be taken into account these disturbances as follows.

1) Power line interference (PLI) is induced from the power line AC in the form of common-mode interference.

2) Input-referred noise is the noise generated at the amplifier input, which should be much smaller than the input signal.

3) DC Polarization voltage is the voltage generated on the skin from the electrode attached when breathing may move causing the DC polarization voltage to be higher. From the use of multiple electrodes, it will cause the pressure generated by each electrode to be unequal [1].

4) High input impedance amplifier is happened, if the input impedance of the front-end amplifier is insufficient when connecting to a high impedance electrode. It will result in reducing the gain of the amplifier circuit.

Motion artifacts are produced by attaching electrodes on skin for ECG signal measurement to the front-end amplifier circuit. Problems may occur because the electrode's conductive contact on surface is not close enough to the skin shown in Fig. 2. Due to shifting from breathing or other factors, the signal generated by the electrode is asymmetrical signal on both sides of the electrode, resulting in unequal contact impedance (Z_E) and half-cell potential (V_H) on each side. In which a small change in V_H and Z_E directly affects the input voltage signal, resulting in the baseline signal fluctuation. This situation is worse, if the electrode is dry that will increase the V_H value [1]. Motion artifacts can also be managed in the digital domain. When the ECG signal is digitized, it goes through the digital signal processing (DSP) [2], but it adds a lot of components that are not suitable for portable devices.

As a result of the DC polarization voltage as well as the contact impedance (Z_E) and half-cell potential (V_H), the offset voltage is applied at the

Table 1. Requirements for ECG front-end amplifier

CMRR	>60dB
Input Impendance	$> 10 M\Omega$
Differential gain	40 dB or greater
Input referred noise	< 5µVrms
Bandwidth	0.05-250Hz

input of the front-end amplifier and can cause the amplifier to saturate at the output. If voltage is not the same for each electrode, it will cause the common mode rejection ratio (CMRR) is also low.

Therefore, the design of high gain is required for the front-end amplifier. It should be the higher input impedance than the electrode impedance and high CMRR to eliminate the PLI or common-mode interference with the low input noise [1]. Requirements for the ECG front-end amplifier are summarized in Table 1.

In general, the ECG front-end amplifier is used the low-noise instrument amplifier with three-Op-Amp circuit where the CMRR depends on the matching of the resistance in the circuit, resulting in the CMRR value is not high [1]. Therefore, an instrument amplifier circuit with a high CMRR value independent of resistance matching has been developed. This leads to a CCII-based current-mode instrumentation amplifier (CMIA) [3] circuit. However, the above circuit does not have to suppress the input DC offset. Thus, there is also another type of instrumentation amplifier that uses ac-coupled capacitive IA [1], which has the advantages of direct signal suppression at the input and low power consumption, while the input impedance is also low. Subsequently, the currentbalancing instrumentation amplifier (CBIA) has been presented [4, 5] with the advantage of a high input impedance, a dynamic range at input and CMRR better than a three-Op-Amp, which trades off between the power consumption and noise. It can improve the less noise and higher CMRR by using chopping technique [6-8] as well as having the DC suppression. On the other hand, the circuit must have the switch chopping for making the circuit larger and more complex.

In this paper, the improvement of the proposed ECG amplifier is presented from the currentbalancing instrument amplifier. There is a low pass filter to reduce the effect of input DC offset voltage or direct voltage suppression on the input and a high pass filter to filter out the frequencies other than the ECG signal. This leads to an instrument amplifier with the band-pass filtering shown in Fig. 3 that it is unnecessary to add the low pass filter, while retaining other necessary properties as the high input

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Figure. 3 Block diagram of the proposed ECG measurement system



Figure. 4 Ideal CCII (a) symbol, (b) the equivalent circuit



Figure. 5 CCII-based balancing instrumentation amplifier



Figure. 6 Equivalent circuit of front-end ECG amplifier

impedance, CMRR and DC suppression with the compact circuit. This improvement will be achieved by using only two second-generation current conveyor (CCII) circuits.

2. Principle of second generation current conveyor

The second generation conveyor (CCII) circuit has the symbol shown in Fig. 4 (a). The electrical properties between the ports follow the equivalent circuit shown in Fig. 4 (b) [9], which can be generated from bipolar transistor or MOSFET transistor.

From the CCII equivalent circuit in Fig. 4(b), the

ideal electrical properties between the ports of the circuit are found as follows: at port Y, the $I_Y = 0$, no current flows to port Y and $r_x = 0$, $V_X = V_Y$ that is the voltage at port X equals the voltage at port Y and $I_X = I_Y$, the current flowing through port X is also passed to port Z which is a current controlled current source with the infinite output impedance (r_z) .

3. Proposed front-end ECG amplifier based on CCII

The objective of proposed circuit is how to use CBIA-based on CCII design. From Fig. 5, the frontend CCII-based balancing instrumentation amplifier is presented with two CC-IIs and two resistors. Fig. 6 shows the equivalent circuit of proposed front-end ECG amplifier using CCII shown in Fig. 4 that can be viewed in the topology of CBIA as the transconductance in the input stage and impedance in the output stage.

At the transconductance stage, it can convert the differential input voltage v_{in} to i_1 through the resistor R_1 as

$$i_1 = \frac{v_{in}}{R_1} \tag{1}$$

The current i_1 can transfer to the output with the current gain α

$$i_2 = \alpha i_1 \tag{2}$$

and current i_2 can transfer to the output voltage through the resistor R_2 as

$$v_{out} = i_2 R_2 = \alpha i_1 R_2 = \alpha \frac{v_{in}}{R_1} R_2$$
 (3)

Therefore, the voltage gain of CBIA is

$$\frac{v_{out}}{v_{in}} = \alpha \frac{R_2}{R_1} \tag{4}$$

If CCII is ideal, $r_x = 0, r_z = \infty$ and $\alpha = 1$, then $i_x = i_z$. Therefore, the voltage gain is defined by

$$\frac{v_{out}}{v_{in}} = \frac{R_2}{R_1} \tag{5}$$

It can be seen that the circuit built from 2-CCIIs can be used to create an IA circuit that determines the gain from only 2 resistors.

For the band-pass filtering of instrumentation amplifier, two selective frequency devices are added to the circuit in Fig 5. The result shows the proposed front-end CCII-based ECG amplifier in Fig. 7, which is consisting of only two CCIIs connected to *Vol.16, No.4, 2023* DOI: 10.22266/ijies2023.0831.29

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Figure. 7 Proposed front-end CCII-based amplifier

passive devices at the port X is R_x and C_x , at port Z is R_L and C_L . The proposed circuit receives the input signals from the electrode and enters the port. And from the properties of the CCII circuit in Fig. 7, the currents i_x and i_z can be expressed as

$$i_{z} = i_{x} = \frac{v_{1} - v_{2}}{2R_{x} + \frac{1}{sC_{x}}}$$
(6)

We assign that $v_{id} = v_1 - v_2$, it arrives at

$$i_z = v_{id} \frac{sC_x}{1 + s2R_x C_x} \tag{7}$$

Then, we analyze the circuit in Fig. 4 at the port Z to find the output signal v_o , we get

$$v_o = i_z Z_L = i_z \frac{R_L}{1 + s R_L C_L} \tag{8}$$

Transfer function of circuit can be calculated by substituting Eq. (7) into Eq. (8), we arrive at

$$\frac{v_o}{v_{id}} = \frac{sC_x}{1+2sR_xC_x} \cdot \frac{R_L}{1+sR_LC_L} \tag{9}$$

$$\frac{v_o}{v_{id}} = \frac{sC_x R_L}{(1 + 2sR_x C_x)(1 + sR_L C_L)}$$
(10)

From Eq. (10), the differential gain A_{dm} , the low frequency cut-off f_{CL} and high frequency cut-off f_{CH} are given by

$$A_{dm} = \frac{R_L}{2R_x} \tag{11}$$

$$f_{CL} = \frac{1}{2\pi (2R_x)C_x} \tag{12}$$

$$f_{CH} = \frac{1}{2\pi R_L C_L} \tag{13}$$

We found that the proposed circuit has the properties of band-pass amplifier required by ECG amplifiers by Eqs. (11) and (12). It is seen that the *International Journal of Intelligent Engineering and System*

differential gain A_{dm} depends on R_x and R_L , while f_{CL} depends on C_x and f_{CH} depends on C_L . It can conclude that the f_{CL} and f_{CH} are independent.

3.1 DC suppression

The CCII-CBIA circuit at the input stage can eliminate the common mode signal using CMRR that CMRR depends on the mismatch at the input buffer part of both CCIIs. Although the CMRR value is high, it will not suppress the dc-offset caused by motion artifacts from either side of the lead electrode. This dc-signal will be suppressed from the current through a capacitor between port x of both CCII detailed in Fig. 7. The input voltage at port Y with dc-offset occurs that it is switched to the current at port x, then capacitor C_x can suppress the DC current (i_x) from either side of the lead electrode at v_1 and v_2 . Then, the current (i_x) is copied to port z (i_z) and further converted to the output voltage.

3.2 Input-referred noise

According to the circuit design for measuring the small signal, the input-referred noise is an important parameter considering for designing the ECG amplifier. Half-circuit equivalent of noise in the conventional ECG amplifier is presented in Fig. 8 compared to the half-circuit equivalent of inputreferred noise shown in Fig. 9.

From Fig. 9, the input-referred noise for halfcircuit can be expressed by

$$\overline{v_{nAmp,half}^2} = \overline{v_{n1}^2} + \overline{v_{RX}^2} + \frac{\overline{v_{RL}^2}}{(R_L/2R_X)^2}$$
(14)

And the full circuit of input-referred noise is given by

$$\overline{v_{nAmp,full}^2} = 2\overline{v_{n1}^2} + 2\overline{v_{RX}^2} + 4\frac{\overline{v_{RL}^2}}{(R_L/2R_X)^2}$$
(15)

From Eq. (15), the input-referred voltage noise reduction appeared from the feedback load resistor R_L transferred to the input is from self-attenuation. Meanwhile the noise from resistor R_X is less than noise for CCII circuit. Therefore, the noise from CCII circuit can be approximated by

$$\overline{v_{nAmp}^2} \cong 2\overline{v_{n1}^2} \tag{16}$$

4. Simulation results

For the simulation, the proposed CCII in the transistor-level topology shown in Fig. 10 has been introduced to provide a circuit design with single

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Figure. 8 Half-circuit equivalent of noise in ECG amplifier



Figure. 9 Half-circuit equivalent of input-referred noise



Figure. 10 Transistor-level topology of the single supply CCII

supply and low-power consumption that can be used in the portable devices. Proposed front-end ECG amplifier is used two CCIIs connected with resistors and capacitors shown in Fig. 11 in the transistorlevel topology using the bias circuit by current mirror M_{19} to both CCIIs considered the body effect with the NMOS body connected to GND and PMOS body connected to V_{DD}.

The simulated experiment is used the 0.35μ m CMOS technology model parameters and the transistor aspect ratios design parameters shown in Table 2. For the calculation, the gain from Eq. (15) and frequency response covered the vital signs in the range of 2-500Hz from Eqs. (11)-(13) is considered. Design parameters in Table 2 are used for simulation at $A_{dm} = 250$. The result shows the frequency

response at 47dB in Fig. 12. It found that the range of bandwidth is of 0.9-512Hz. Fig. 13 shows that CMRR of the proposed circuit is measured at 53dB and the differential mode gain (A_{dm}) is at 47 dB and common-mode gain (A_{cm}) is at -6dB. It can conclude that these measured parameters proper to the ECG front-end amplifier.

4.1 Equivalent circuit model of electrode-tissue interfaces

It can be seen that there are many factors to consider while measuring the vital signs from tissue to electrode interface. As studied by [1], the authors have been presented how the tissue-electrode interface model for the biological signals measurement form the body-mounted electrodes are affected the measuring circuit and vital sign amplifier.

Fig. 14(a) shows the epidermis at the top and the dermis under the epidermis. An electrolyte gel is bonded between the electrode contact and the epidermis for signal measurement. Fig. 14(b) is the equivalent circuit of the interface between the electrode contact and the epidermis, where C_{elec} and R_{elec} are the electrode-tissue capacitor and resistor at 47nF and 51 k Ω , respectively [1].

Half-cell potential V_H in form of offset voltage is of 0.22V and C_{epi} , R_{epi} and R_D are the electrodeepidermis capacitor and resistor at 10nF and 100 k Ω [2]. Then, the electrode-tissue interface equivalent circuit model is shown in Fig. 15(b) that is applied to the front-end amplifier circuit in order to test the non-ideal factor of ECG measurement by operation of the ECG amplifier at the half-cell potential or offset voltage. The changes due to the motion artifact at V_{H1} in Fig. 15(b) is studied the effect on the various properties of the ECG amplifier circuit.

Fig. 16 depicts the CMRR versus the offset voltage in the range between $\pm 1V$. It is noticed that the offset voltage has no effect to CMRR. In

Table 2. Transistors aspect ratio design parameters for proposed front-end ECG amplifier

proposed nont-end Lee amplifier							
MOSFET	W (µm)	<i>L</i> (µm)					
M_1, M_4	20	4					
M_2, M_3	30	4					
M_5, M_6, M_7, M_8	20	4					
M_9, M_{10}	40	4					
M_{11},M_{12} , M_{16} , M_{17}	220	4					
M_{14},M_{10} , M_{13} , M_{18}	80	4					
M_{19}	80	4					
Capacitor	Value						
C_x , , C_L , R_x , , R_L	$80\mu\mathrm{F}$, $0.64\mathrm{nF}$, $1\mathrm{k}\Omega$, $0.5\mathrm{M}\Omega$						
Biasing	Value						
$I_{\rm B}, V_{\rm DD}$	1µA , 5 V						

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A_{dm} and A_{cm}

addition, the total harmonic distortion (THD) versus the input signal is at 1mV and 2mV from input offset voltage is demonstrated and the output signal at 1% THD and $\pm 0.5V$ shown in Fig. 17. It seems that the proposed ECG amplifier is robust to the input signal including with the $\pm 0.5V$ offset voltage.

And Fig. 18 presents the properties of inputreferred noise (IRN) at 1-1kHz, less than $2\mu V_{rms}$ at offset voltage = ±0.5V. It can be seen that the proposed ECG circuit has the low IRN for the ECG amplifier.

Fig. 19 shows the input impedance (Z_{in}) in the range of 227-331 M Ω at ±0.5V. It is found that Z_{in} is higher than the electrode-tissue resistor that does not attenuate the input signal. According to the time domain analysis, the equivalent model of electrode-tissue interface is presented in Fig. 15(b).

4.2 ECG real dataset with PLI and DC offset

For the empirical simulation, the 1mV amplitude of clean ECG real dataset [10, 11] is used for input signal (V_s) as shown in Fig. 20(a). The input signal is disturbed by PLI (V_{CM}) at amplitude of 300mV, frequency of 50Hz and the offset voltage of $V_H = 0$ V shown in Fig. 20(b).

Fig. 21 depicts the output signal. It may also be noted that the proposed front-end ECG amplifier can eliminate the PLI induced in the ECG signal.

Then, the range of input offset is studied with the ECG output signal for DC suppression shown in Fig. 22, where the input offset is added at 0.25V.



V_s: ECG signal: Amplitude = 0.5-4mV/0.05-250HzV_H: Half-cell potential (offset voltage) = 0.22 VV_{CM}: Common-mode or PLI = 300mVV_{Bias}: Biased voltage; V_{DD}/2

Figure. 15 Model of electrode-tissue interface (a) Equivalent circuit and (b) Circuit for simulation



Figure 16 CMRR versus DC offset in the range of $\pm 1V$

Meanwhile, the ECG output signals are presented in Figs. 23 and 24 where the input offset signals are added at 0.5V and 1 V, respectively. In accordance with the results from time-domain in Figs. 22-24, it found that the proposed ECG front-end circuit can amplify the ECG disturbed input from PLI including with the 1V offset voltage.

Table 3 shows the properties of proposed frontend CCII-based ECG amplifier compared with the previous works. It is noticed that the proposed circuit has IRN lower than 10 times compared to



Figure 17 THD versus input offset in the range of -0.5 to 0.5V for amplitude from $1mV_p$ to $2mV_p$



Figure. 18 Input-referred noise VS input offset in the range of -0.5V to 0.5V



0.5V

[14, 15] in the transistor level, where input impedance of proposed is $280M\Omega$ at 100Hz with $\pm 0.5V$ DC suppression at 1%THD.



Figure. 20 ECG input signal (a) ECG input signal at 1mV [10] and (b) ECG input at 1mV including with the PLI at amplitude of 300mV

According to the requirements for ECG frontend amplifier shown in Table 1, the summary and comparison of performance circuits in Table 3 are as follows. The CMRR of proposed circuit is of 53dB that is robust to DC offset at ± 0.5 V as shown in Fig. 16. It is noted that V_{DD} is set to 5V supported for USB and suitable for single supply of portable electronic devices.

The advantages of proposed circuit are as the total current (I_{total}) is of 12.45µA less than CCII, input impedance (Z_{in}) is high and DC suppression is more robust for ±0.5V at 1%THD even the 1mV and 2 mV amplitude of input signal as shown in Fig. 17.

5. Conclusion

This paper has been proposed the front-end CCII-based ECG amplifier circuit for DC suppression at the input. The small signal analysis has been derived. Motion artifacts are concerned and generated in terms of the input offset at ± 0.5 V and equivalent circuit model of electrode-tissue interface

in the simulation. Simulation results show that the proposed CCII-based ECG front-end amplifier circuit has a high input impedance at 280M Ω , IRN of 0.24 μ V_{rms} at 100Hz for ECG amplifier and at ±0.5V DC suppression, a mid-band gain of 47 dB, CMRR of 53 dB, IRN of 0.24 μ Vrms@100Hz, input impedance of 280M Ω and the power consumption of 66 μ W. It is confirmed that proposed circuit can apply for ECG measurements in practical.



Figure. 21 Output ECG from input offset voltage = 0V



Figure. 22 Output ECG from input offset voltage = 0.25V



Figure. 23 Output ECG from input offset voltage = 0.5V

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Parameters	[7]	[8]	[12]	[13]	[14]	[15]	Proposed circuit
	2020	2022	2018	2018	2021	2019	_
$A_{dm}[dB]$	60	26	44	51	40	40	47
CMRR [dB]	103	109	105	51	83	86	53
IRN [µV _{rms}]	0.59	0.91	NA	NA	2	2	0.24@100Hz
Power [W]	15.2µ	1.19µ	177µ	846µ	0.67µ	0.67 µ	62µ
V _{DD} [V]	1.2	3	± 0.75	± 0.9	2	+2	+5
Itotal [A]	12.7µ	0.39µ	NA	NA	0.36µ	0.336	12.45µ
Zin@fin	4-	469@50	NA	NA	57@150	295@50Hz	280@100Hz
[MΩ,Hz]	380@50						
DC	+0.5	± 0.4	NO	NO	NO	± 0.1	\pm 0.5
Suppression							
[V]							
Active/Passive	NA	NA	2/1	2/1	NA	NA	2/5
element count							
Active	Chopper	Chopper-	CCII	COA	Transistor	Transistor	CCII
element used	-CBIA	CBIA			-level IA	-level IA	

Table 3. Summary and comparison of performance



Figure 24 Output ECG from input offset voltage = 1V

Conflicts of interest

The authors declare no conflict of interest.

Author contributions

Conceptualization, Panlop Pantuprecharat, Suchada Sitjongsataporn and Prajuab Pawarangkoon; methodology, Panlop Pantuprecharat; software, Panlop Pantuprecharat

and Prajuab Pawarangkoon; formal analysis, Panlop Pantuprecharat, Suchada Sitjongsataporn and Prajuab Pawarangkoon; writing—original draft preparation, Panlop Pantuprecharat, and Suchada Sitjongsataporn; writing—review and editing, Panlop Pantuprecharat and Suchada Sitjongsataporn; supervision, Suchada Sitjongsataporn.

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