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Power Quality Performance Enhancement Using Single-phase UPQC with Fuzzy Logic Controller Integrated with PV-BES System

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Abstract: The research objective is to enhance the power quality performance of a single-phase unified power quality conditioner (UPQC) system supplied by a combination of photovoltaic (PV) array and battery energy storage (BES) using fuzzy logic control (FLC) connected to a 220 V-50 Hz distribution system. The PV array consists of several PV panels with a maximum power of 12 kW. Solar PV is highly dependent on external environmental factors i.e. sunlight, temperature, radiation, weather and seasons where levels can change at any time. BES functions to store PV power and both provide a more stable load power supply to the load when an interruption/disconnection occurs on the source (off-grid mode). The proposed system is also more efficient because it does not require a DC-link capacitor. The FLC method with the Mamdani fuzzy inference system (FIS) is proposed to overcome the weaknesses of proportional and integral (PI) control in determining proportional constants and integral constants. The faults were selected in a total of six case studies (CS) based on the fault categories and single-phase UPQC configuration i.e. CS 1 (sinusoidal/S-Sag-non-linear load/NL-PV), CS 2 (S-Swell-NL-PV), CS 3 (S-interruption/Inter-NL-PV), CS 4 (S-Sag-NL-PV-BES), CS 5 (S-Swell-NL-PV-BES), and CS 6 (S-Inter-NL-PV-BES). In single-phase UPQC systems from CS 1 to CS 6, FLC is able to produce lower total harmonic distortion (THD) of load voltage and source current, as well as higher source power factor (PFS) compared to proportional-integral (PI) control. The system using single-phase UPQC on CS 1 to CS 6 with PI/FLC control is capable of producing load voltage THD and source current THD below IEEE 519 limits. The system with a single-phase UPQC configuration with PI/FLC control shows that CS 4 to CS 6 is capable produces a change in load voltage disturbance that is slightly greater than CS 1 to CS 3. The system uses single-phase UPQC with PI/FLC control on CS 3 and CS 6 is able to deliver load active power with values close to CS 1 and CS 4.

Keywords: Power quality, Single-phase UPQC-PV-BES, FLC, PI, THD.

1. Introduction

Rapid growth is being experienced in the demand for electrical energy based on renewable resources that are connected to the distribution network. The primary drawback of renewable energy is its sporadic power generation, which varies with the seasons. In addition to producing electricity, PV generators, as a component of renewable energy, also cause several other issues, such as voltage sag or swelling, harmonic distortion from PV's integration into the network, power converter devices present, unbalanced load current disturbances from unbalanced loads, and non-linear load current harmonics from the massive increase in loads in this category in terms of both quantity and capacity, all of which ultimately result in a decrease in the quality of the electricity. A UPQC device was suggested as a solution to several issues about the integration of PV with low-voltage distribution systems and the resultant power quality disruptions. UPQC is used to make up for issues in source voltage and load current power quality. For better simultaneous control of power quality issues, UPQC combines series active filters (Se-AF) and shunt active filters (Sh-AF) connected in parallel [1, 2].

UPQC connected to a three-phase, four-wire (3P4W) system using synchronous reference frame (SRF) control theory has been investigated in [3]. Simulation results shown that the proposed UPQC control method is capable of load balancing, neutral source current mitigation, power-factor correction, load voltage harmonic mitigation, and source current. The implementation of UPQC in a distribution system containing several single-phase distributed energy resources (DER) has been simulated using power systems computer aided design (PSCAD) [4]. The shunt converter can provide all of the reactive power required by the load, the series converter may adjust the voltage magnitude to account for variations in the point common coupling (PCC) bus voltage, and the proposed UPQC can isolate the PCC voltage from the load bus voltage. The non-linearly connected single-phase UPQC system uses the zero-voltage switching (ZVS) method and the modified repetitive controller (MRC), respectively, which have been proposed in [5, 6]. Many power quality issues, such as distorted voltage, sag/swell voltage, load voltage harmonics, source current harmonics, and reactive power compensation, can be compensated for by the suggested UPQC control system.

Improving power quality using single-phase UPQC integrated PV using PQ theory, discrete adaptive notch filter (DANF), and phase locked loop (PLL)-less d-q control in conditions of varying solar radiation, sag/swell voltage disturbances, and load side disturbances has been investigated in [7-9]. The function of the PV array was to maintain the DC link voltage by injecting active power so that critical loads still receive a sinusoidal voltage source. The proposed UPQC-PV system was able to improve network power quality by providing compensation for load current harmonics and reactive power. The implementation of single-phase UPQC and three-phase UPQC using the SRF method with two operating modes has been observed in [10] and [11]. The proposed UPQC control system was able to suppress harmonic currents, compensate for reactive power, improve power-factor, and compensate for sag/swell voltage at the source.

A modular multilevel matrix converter (M3C) is suggested in [12] as a single-phase UPQC method to enhance power quality in medium- and high-voltage distribution systems. The performance of the M3C-UPQC operating system has been confirmed through a scaled-down experimental prototype. A faster approach using the membership function (MF) concept, which uses a weight factor (WF) in three-phase UPQC control for sag and distorted voltage disturbances, has been observed in [13]. The results of the proposed approach shown that this method is capable and effective in identifying actual UPQC parameters in three-phase systems. In [14], PV system network integration via single-phase PV-UPQC based on a new notch filter control algorithm has been designed and implemented. Superior features such as improved phase identification, voltage sag/swell, voltage imbalance, and the removal of voltage and current harmonics can all be achieved with the suggested control system. It has been noted in [15] that notch filters and feedback were used in a single-phase UPQC control technique to decrease DC-link voltage ripples caused by low-frequency effects. A module for AC microgrid (ACMG) in the form of modulated UPQC (M-UPQC) to independently improve the quality of AC/DC hybrid microgrid operating parameters has been carried out [16]. Through the use of an experimental setup, the effectiveness of M-UPQC functioning under static and dynamic disturbance circumstances was evaluated. An integrated PV-wind hybrid system on UPQC has been presented as a distributed generation (DG) system [17]. The UPQC-Hybrid PV-Wind Turbine (WT) system, apart from being able to supply active power to the grid, the system, is also able to compensate for reactive power and suppress load harmonic currents, the load was supplied with a voltage that is free of harmonics, balanced and regular.

Three-phase UPQC simulations using a modular multilevel converter (MMC) with Matlab and the results verified with field programmable gate arrays (FPGA) have been carried out in [18]. The proposed system was able to compensate sag voltage, suppress source current harmonics, control source voltage due to unbalanced and varying loads, and reduce load voltage harmonics. For electronic device efficiency, integrated single-phase UPQC of large-capacity PV arrays without using a DC-link capacitor using FLC has been proposed in [19]. In response to sag/swell and interruption on the source, the system can lower source current/load voltage harmonics, maintain load voltage, and enhance load active power.

The weakness of PV integration in UPQC which has been worked on by previous researchers in [7-9],[14],[17],[19] is its intermittent nature, namely its inability as a renewable energy generator to produce energy continuously. Solar PV is highly dependent on external environmental factors i.e. sunlight, temperature, radiation, weather and seasons where levels can change at any time. To overcome this weakness, the research proposes a single-phase UPQC system supplied by a combination of PV array and BES using FLC connected to a 220 V and

Tabel 1. Comparison with other previous literature

Authors	Method	THD V_L	THD I_S	PF_S	Disturbance Mitigation						UPQC Injected by	DC Link Capacitor	BES
					Sag	Swell	Interruption	Unbalance Source/Load	LL	NL			
[1]	3PH-UPQC-PI-DG	X	X	X	✓	✓	✓	X	X	✓	DG	✓	X
[3]	3PH-UPQC-SRF	✓	✓	X	✓	X	X	✓	✓	✓	X	✓	X
[4]	1PH-UPQC-DER	X	X	✓	X	X	X	✓	✓	X	DER	✓	X
[5]	1PH-UPQC-ZVS	✓	✓	X	✓	✓	X	X	X	✓	X	✓	X
[6]	1PH-UPQC-MRC	✓	✓	X	X	X	X	X	X	✓	X	✓	X
[7]	1PH-UPQC-PV-PI	✓	✓	X	✓	✓	X	X	✓	✓	PV	✓	X
[8]	1PH-UPQC-PV-DAFN	X	✓	X	✓	✓	X	X	✓	✓	PV	✓	X
[9]	3PH-UPQC-PV-PLL Less d-q	✓	✓	X	✓	✓	X	✓	✓	✓	PV	✓	X
[10]	1PH-UPQC-PV-SRF-PI	X	X	X	✓	✓	X	X	X	✓	X	✓	X
[11]	3PH-UPQC-PV-SRF-PI	X	✓	X	✓	✓	X	X	X	✓	X	✓	X
[12]	1PH-UPQC-M3C	✓	✓	✓	✓	✓	X	X	X	✓	X	✓	X
[13]	1PH-UPQC-MF-WF	✓	✓	✓	✓	✓	X	X	X	✓	X	✓	X
[14]	1PH-UPQC-PV-PLL Notch Filter	X	✓	X	✓	✓	X	X	X	✓	PV	✓	X
[15]	1PH-UPQC-Low Frequency dc-link Voltage Ripple	✓	✓	X	✓	✓	X	X	X	✓	X	✓	X
[16]	Modulated-3PH-UPQC-Hybrid AC/DC Microgrid	✓	✓	X	X	X	X	✓	X	✓	X	✓	X
[17]	3PH-UPQC-PV-WT	✓	✓	✓	X	X	X	X	X	✓	PV and WT	✓	X
[18]	3PH-UPQC-MMC	✓	✓	X	✓	X	X	X	X	✓	X	✓	X
[19]	1PH-UPQC-PV-FLC	✓	✓	X	✓	✓	✓	X	✓	✓	PV	X	X
This paper	1PH-UPQC-PV-BES-FLC	✓	✓	✓	✓	✓	✓	X	X	✓	PV	X	✓
	Note: ✓ = available; X = not available												

50 Hz distribution system. BES functions to store PV power at night and provide a more stable load power supply to the load when a disconnection occurs on the source side (off-grid mode). A summary of the contribution and position of this paper compared to other previous literature is shown in Table 1.

In light of the aforementioned issues, the primary contributions of this study are as follows: (1) designing UPQC supplied by PV and BES without DC link capacitors to mitigate issues with power quality on the load and source sides; (2) validating performance single-phase UPQC-PV and single-phase UPQC-PV-BES, both without the use of DC-link capacitors, to ascertain the optimal configuration for mitigating power quality, (3) Application of FLC with FIS-Mamdani on Sh-AF single-phase UPQC-PV series connected to BES without DC-link capacitor, and (4) Validation of the FLC method with PI control on a single-phase UPQC-PV circuit connected to BES to identify the optimal control for enhancing system power quality.

This paper is arranged as follows: The suggested approach, which includes a model of a single-phase UPQC-PV-BES without a DC-link capacitor linked to NL, is shown in Section 2. It also includes simulation parameters, PV array, Se-AF, Sh-AF, PI, and FLC. The results and discussion are shown in

Section 3. The data includes the single-phase UPQC's magnitude output voltage and current, THD value, source and load power-factors, percentage of load voltage disturbance, PV output, BES output, and load active power utilizing PI and FLC. This section presents two single-phase UPQC controls in 12 CS by PV and PV-BES, respectively. Matlab-Simulink is used to verify the results. Finally, the paper is concluded in Section 4.

2. Methodology

2.1 Research method

The goal of the project is to use FLC coupled to a single-phase low-voltage distribution system to enhance the power quality performance of a single-phase UPQC system provided by a combination of a PV array and BES. Multiple PV panels, each having a maximum PV output of 12 kW, make up the PV array. Two circuit designs are suggested: one that uses solely a PV array for single-phase UPQC coupled to NL, and the other that uses a PV array in conjunction with BES. The suggested UPQC circuit does not make use of a DC link capacitor circuit, according to earlier studies. When in on-grid mode, the large-capacity PV array channels active power to the source via Se-AF, compensates for load reactive power, suppresses load harmonic currents, and lowers load voltage. In this way, it acts as a DC voltage source, taking the place of DC capacitors. The PV array channels active power to the load via Sh-AF to maintain a constant voltage and load power while it is in off-grid mode or when the source side voltage is switched off. The addition of the BES circuit allowed it to store solar energy and release it in the event of a voltage interruption (mode-off grid), thus overcoming the intermittent nature of PV, which is dependent on temperature, weather, and solar irradiance and can only generate power during the day. Fig. 1 shows the proposed model of a single-phase UPQC-PV-BES system without a DC link capacitor. Fig. 2 shows the active power flow of a single-phase UPQC without a DC link capacitor supplied by PV array and PV-BES combination.

Combining single-phase Sh-AF and single-phase Se-AF results in single-phase UPQC. Four metal oxide semiconductor field effect transistor (MOSFET) switches (MO_1, MO_2, $MO_3, and\ MO_4$) make up the single-phase Se-AF circuit used in this study. Their purpose is to inject a compensatory voltage into the load bus in the event that there is a voltage sag or swell on the source bus. In the meantime, the four insulated gates bipolar transistor (IGBT) switches (IG_1, IG_2, $IG_3, and\ IG_4$) that make up the single-phase Sh-AF circuit serve to provide harmonic compensatory current into the source bus as the result of a non-linear load (NL) existence. In order to provide the load bus with a more stable active power supply in the event of voltage sags, swellings, and disconnections on the source bus, single-phase UPQC-PV-BES is proposed. This reduces the THD of the load voltage while also lowering the THD of the source current on each disturbance.

A 220V-50 Hz voltage distribution line connects the single-phase UPQC-PV-BES circuit to the source bus or point common coupling (PCC) between the load bus. The flaw in PI control in figuring out integral constants (K_I), and proportional constants (K_P), is addressed by the FLC approach with Mamdani's fuzzy inference system (FIS). The following six case studies (CS) describe faults in single-phase UPQC setups linked to PV arrays and PV-BES combinations:

a. CS 1 (S-Sag-NL-PV): There is a 50% voltage drop in the sinusoidal source when the system is linked to the NL. To generate the sag voltage, a 220 V-50 Hz source is connected in series with the source inductance ($L_{S=} = 0.1\,mH$), parallel with the component inductance ($L_{P=} = 0.1\,mH$), and in normally open (NO) mode with power breaker circuit 1 (CB1).The DC link terminal is connected to a PV array with a nominal power of 12 kW. The single-phase UPQC is connected to NL in the form of a four-bridge diode rectifier circuit connected to the load in the form of NL resistance ($R_L = 60\,\Omega$), and NL inductance ($L_L = 1\,mH$).
b. CS 2 (S-Swell-NL-PV): A 50% voltage swell is experienced by the sinusoidal source when the system is linked to NL. A 220 V-50 Hz source voltage linked in series with the source inductance component ($L_{S=} = 0.1\,mH$), is coupled in parallel with a 330 V-50 Hz voltage source via CB 2 in the NO condition to generate the swell voltage. The same as in CS 1, the DC link circuit is supplied by a PV array with the same capacity, and a single-phase UPQC system is also connected to the NL.
c. CS 3 (S-Inter-NL-PV): The system is connected to NL and the sinusoidal source experiences 100% interrupt voltage. The interrupt voltage is generated by short-circuiting a 220 V-50 Hz voltage source circuit connected in series with the source inductance component ($L_{S=} = 0.1\,mH$), in parallel via CB 3 with NO condition. The same as CS 1, the DC link circuit is supplied

by a PV array with the same capacity and a single-phase UPQC system is also connected to the NL

d. CS 4 (S-Sag-NL-PV-BES). The system is the same as CS 1, the difference is that the system's DC-link circuit is not only supplied by the PV array but is also connected to the BES circuit via CB 4 with NO conditions.
e. CS 5 (S-Swell-NL-PV-BES). The system is the same as CS 2, the difference is that the system's DC-link circuit is not only supplied by the PV array but is also connected to the BES circuit via CB 4 with NO conditions.
f. CS 6 (S-Swell-NL-PV-BES). The system is the same as CS 3, the difference is that the system's DC-link circuit is not only supplied by the PV array but is also connected to the BES circuit via CB 4 with NO conditions.

The total simulation time is 0.5 s, with an interruption duration of 0.2 s between 0.15 s- 0.35 s.

To enhance power quality on six CSs, the FLC approach is applied as DC voltage control on Sh-AF, and the outcomes are contrasted with PI control. A single-phase UPQC circuit employs FLC and PI control at each CS, for a total of 12 CS. The findings of the analysis performed on the parameters, which include PV power (P_{PV}), BES power (P_{BES}), and load real power (P_L), as well as the magnitude of the source voltage (V_S), load voltage (V_L), source current (I_S), and load current (I_L), as well as the THD of source voltage (V_S), THD of load voltage (V_L), THD of source current (I_S), and THD of load current (I_L).

After all the parameters are obtained, the next step is to determine the percentage of load voltage disturbance (V_D), and the value of the load power-factor (PF_L), and source power-factor (PF_S), on the single-phase UPQC-PV connected to NL referring to each CS. The aim is to determine a single-phase UPQC combination model that is able to provide the

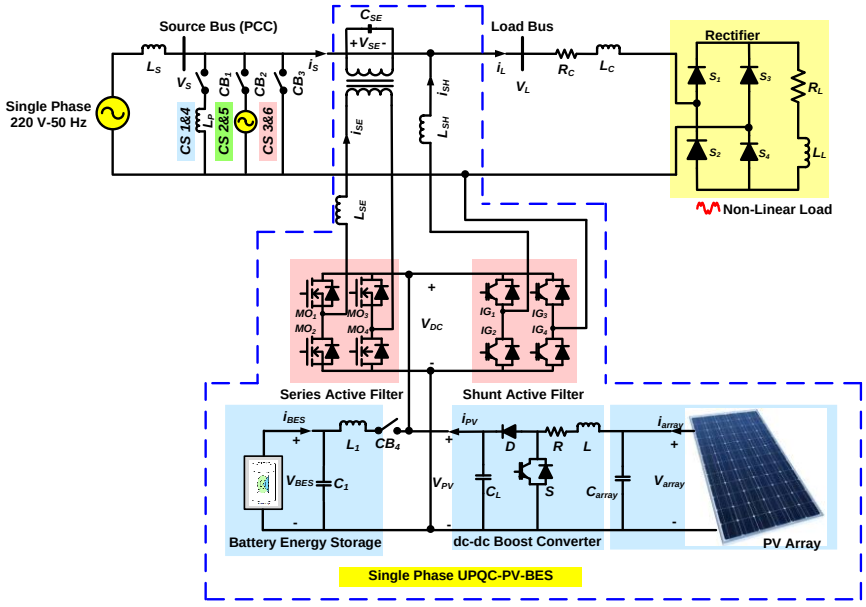
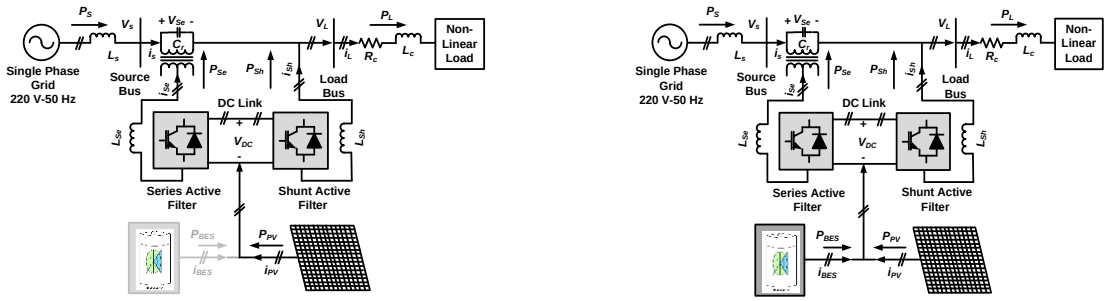


Figure. 1 Proposed single-phase UPQC-PV-BES system model without DC link capacitor



(a) (b)

Figure. 2 Active power flow of a single-phase UPQC without a DC link supplied by: (a) PV array and (b) PV-BES

best performance with indicators i.e. able to reduce THD I_S and THD V_L, improve PF_S, maintain V_L , and distribute P_L on six CS. Table 2, Table 3, and the Appendix section show the abbreviations, notation list, and research simulation parameters, respectively.

2.2 Control of single-Phase shunt-Active filter

UPQC series-active filters that are coupled to a single-phase system are controlled by the unit vector template generation (UVTG) technique [20]. With a frequency of 50 Hz, the peak fundamental input voltage (V_m)is found to be 220 V in magnitude. Fig. 3 displays the single-phase Se-AF control diagram.

2.3 Control of single-Phase shunt active filter

A detailed description of Sh-AF control in single-phase systems as part of UPQC control can be found in [21]. In three phase three wire (3P3W) and three phase four wire (3P4W) systems, P-Q theory—or power theory in general—is frequently utilized. By repeating the two voltage and current signals with a 120º angle shift, this technique can also be applied to single-phase active filters. It employs three voltage and current signals. The separation of power components into mean and oscillatory components forms the foundation of this theory. Phase "a" should be assigned to the single-phase load current, and phases "b" and "c" should be assigned to the doubling technique's additional phases. Equation (1) can be used to mathematically represent the load current as phase current "a." The load current for phases "b" and "c" can be described using Eqs. (2) and (3) if it is considered that Eq. (1) represents the load current for phase "a."

$$i_a = \sum_{i=0}^{n} \sqrt{2}\, I_i \sin(w_i + \theta_i) \tag{1}$$

$$i_b = \sum_{i=0}^{n} \sqrt{2}\, I_i \, sin\,(w_i + \theta_i - 120°) \tag{2}$$

$$i_c = \sum_{i=0}^{n} \sqrt{2}\, I_i \sin\,(w_i + \theta_i - 120°) \tag{3}$$

If it is assumed that Eq. (1) reflect the load current for phase "a," then Eqs. (2) and (3) can be used to explain the load current for phases "b" and "c."

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 1 \\ 1\angle 120° \\ 1\angle 240° \end{bmatrix} [i_a] \tag{4}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 \\ 1\angle 120° \\ 1\angle 240° \end{bmatrix} [v_a] \tag{5}$$

Table 2. Abbreviation

Acronym	Description
UPQC	unified power quality conditioner
PV	photovoltaic
BES	battery energy storage
FLC	fuzzy logic control
FIS	fuzzy inference system
PI	proportional and integral
CS	case study
THD	total harmonics distortion
S	sinusoidal
Inter	interruption
NL	non-linear load
Se-AF	series-active filter
Sh-AF	shunt-active filter
SRF	synchronous reference frame
DER	distributed energy resource
PSCAD	power systems computer aided design
PCC	point common coupling
ZVS	zero voltage switching
MRC	modified repetitive controller
DANF	discrete adaptive notch filter
PLL	phase locked loop
M3C	modular multilevel matrix converter
MF	membership function
WF	weight factor
ACMG	AC microgrid
M-UPQC	modulated UPQC
DG	distributed generation
WT	wind turbine
FPGA	field programmable gate arrays
MMC	modular multilevel converter
1PH	single phase
3PH	three phase
MOSFET	metal oxide semiconductor field effect transistor
IGBT	insulated gate bipolar transistor
3P3W	three phase three wire
3P4W	three phase four wire
UVTG	unit vector template generation
PWM	pulse width modulation
NB	negative big
NM	negative medium
NS	negative small
Z	zero
PS	positive small
PM	positive medium
PB	positive big
PFC	power factor correction
MPPT	maximum power point tracking

Table 3. Notation List

Notation	Description
K_I	integral constant
K_P	proportional constant
L_S	source inductance
L_P	parallel inductance
L_{SE}	series inductance
L_{SH}	shunt inductance
R_C	load resistance
L_C	load inductance
R_L	non-linear load resistance
L_L	non-linear load inductance
V_S	source voltage
V_L	load voltage
I_S	source current
I_L	load current
THD V_S	THD of source voltage
THD V_L	THD of load voltage
THD I_S	THD of source current
THD I_L	THD of load current
PF_L	load power-factor
PF_S	source power-factor
V_{SE}	series voltage
I_{SE}	series current
C_{SE}	series ripple filter
I_{SH}	shunt current
V_m	peak fundamental input voltage
i_a, i_b, i_c	load current for phases “a”, “b”, and “c”
i_α, i_β, i_0	α, β, and 0 reference currents
v_α, v_β, i_0	α, β, and 0 reference voltages
p	active power
q	reactive power
$\bar{p}$	average active power
$\bar{q}$	average reactive power
$\tilde{p}$	oscillating active power
$\tilde{q}$	oscillating reactive power
$\bar{p}_{loss}$	instantaneous active power related to resistive losses and UPQC switching losses.
$i^*_{\alpha\beta}$	$\alpha - \beta$ reference current
i^*_{abc}	three phase reference current
V_{DC}	DC voltage
V_{Ph-N}	phase-to-neutral source voltage
m	modulation value
$V_{DC-error}$	error DC voltage
$\Delta V_{DC-error}$	delta error DC voltage
V_{PV}	PV voltage
I_{PV}	PV current
V_{BES}	PV voltage
I_{BES}	PV current
P_{DC}	DC power
P_{PV}	PV power
P_{BES}	BES power
P_L	load active power
SoC	state of charge
PF_{true}	true power factor
V_D	percentage change in sag/swell and interruption voltage

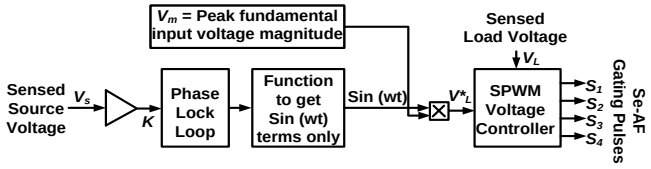


Figure. 3 Single-phase series active filter control using the UVTG method

Using the Clarke transformation approach, the following formulas can be used to determine $\alpha - \beta$ reference voltage and $\alpha - \beta$ reference current: Eq. (7) for load voltage and Eq. (6) for load current.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (7)$$

Reference [21] states that the formulas for active and reactive power are, respectively, in Eqs. (8, 9), and (10):

$$p = v_a i_a + v_\beta i + v_o i_o \quad (8)$$

$$q = v_a i_a - v_\beta i_\beta \quad (9)$$

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (10)$$

Active power and reactive power are composed of two components: average power and oscillating power, or the DC and AC parts, respectively. The following equations represent active and reactive power, respectively, i.e., Eqs. (11) and (12):

$$p = \bar{p} + \tilde{p} \quad (11)$$

$$q = \bar{q} + \tilde{q} \quad (12)$$

A low-pass filter, which can remove high frequencies and produce a fundamental component, or DC part, can be used to determine the DC portion. Eq. (13) [22] explains the $\alpha - \beta$ reference current of the DC active power and reactive power sections.

$$i^*_{\alpha\beta} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} + \bar{p}_{loss} \\ -q \end{bmatrix} \quad (13)$$

The average active power is calculated using the $\bar{p}_{loss}$ parameter of the voltage control. This parameter is represented as instantaneous active power and is related to resistive losses and UPQC switching losses. Before the signal is reduced to the

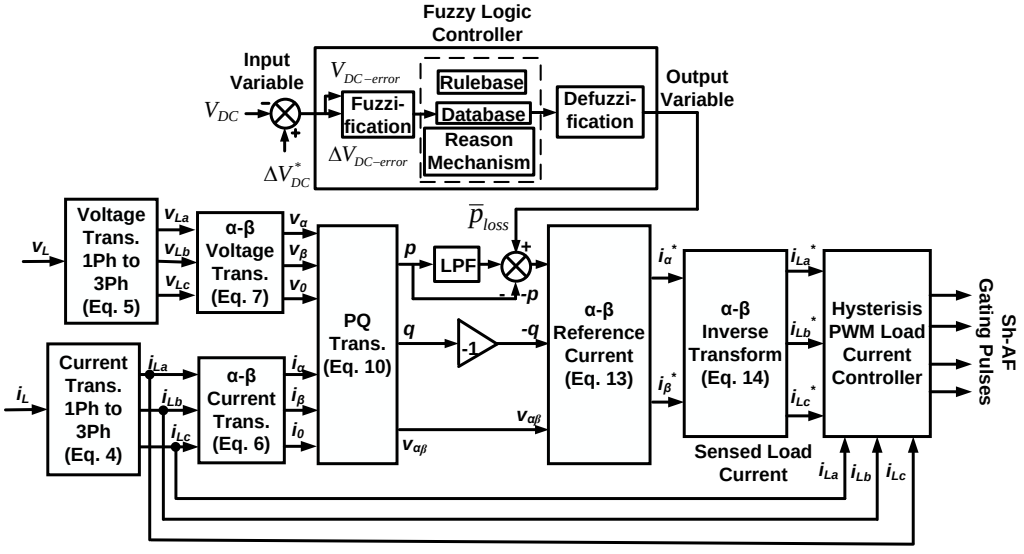


Figure. 4 Control diagram of Sh-AF system using the FLC method

load current, Eq. (14) gives the reference current for the three-phase active power filter. The generation of pulse width modulation (PWM) signals involves reducing the three-phase current and hysteresis bands. In one Sh-AF, the hysteresis band inputs are limited to two out of the six PWM signals produced by the hysteresis band.

$$i_{abc}^{*} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} i_{\alpha\beta}^{*} \quad (14)$$

To operate properly, single-phase UPQC requires a minimum DC voltage (V_{DC}), which is represented in Eq. (15) [23].

$$V_{DC} = \frac{2\sqrt{2}V_{Ph-N}}{\sqrt{3}m} \quad (15)$$

Using a phase-to-nutral source voltage (V_{Ph-N}) of 220 V and a modulation value (m) of 1, DC voltage (V_{DC}) is set at 400 V and is found to be equivalent to 359.26 V.

Next, using Eqs. 1–14 As a basis, the author developed an FLC control model for the Sh-AF circuit coupled to a single-phase system. Fig. 4 shows the results of this model.

2.4 Fuzzy logic controller design

Using the UPQC switching loss ($\bar{p}_{loss}$) as an input variable, the FLC approach for Shunt-AF in the UPQC circuit first creates a source reference current for hysteresis current control and a trigger signal for Shunt-AF. A set of four IGBTs from UPQC with control points PI 1 and PI 2, where K_P and K_I are, respectively, 0.2 and 1.5. The $\bar{p}_{loss}$ is also calculated using the FLC method, following the same process. As seen in Figure 5, each FLC block comprises fuzzification, defuzzification, and decision-making (rulebase, database, and reasoning mechanism). The Mamdani method with max-min is employed by FIS to determine the input and output variables. The rulebase, database, and reasoning process are the three components that make up FIS [24]. In the defuzzification step, the input variables— V_{DC} error ($V_{DC-error}$) and delta V_{DC} error ($\Delta V_{DC-error}$),—as well as the output variable

Tabel 4. Linguistic function and boundaries of the Mamdani FIS set of input variable of $V_{DC-error}$

No.	Input Variables	Linguistic Functions	MFs	Boundaries Parameter
1	Negative Big	NB	trapmf	-400, -240, -120
2	Negative Medium	NM	trimf	-240, -120, -40
3	Negative Small	NS	trimf	-120, -40, 0
4	Zero	Z	trimf	-40, 0, 40
5	Positive Small	PS	trimf	0, 40, 120
6	Positive Medium	PM	trimf	40, 120, 240
7	Positive Big	PB	trapmf	120, 240, 400

Tabel 5. Linguistic function and boundaries of the Mamdani FIS set of input variable of $\Delta V_{DC-error}$.

No.	Input Variables	Linguistic Functions	MFs	Boundaries Parameter
1	Negative Big	NB	trapmf	-400, -300, -200
2	Negative Medium	NM	trimf	-300, -200, -100
3	Negative Small	NS	trimf	-200, -100, 0
4	Zero	Z	trimf	-100, 0, 100
5	Positive Small	PS	trimf	0, 100, 200
6	Positive Medium	PM	trimf	100, 200, 300
7	Positive Big	PB	trapmf	200, 300, 400

Tabel 6. Linguistic function and boundaries of the Mamdani FIS set of input variable of $\bar{p}_{loss}$

No.	Output Variables	Linguistic Functions	MFs	Boundaries Parameter
1	Negative Big	NB	trapmf	-100, -75, -37.5
2	Negative Medium	NM	trimf	-75, -37.5, -12.5
3	Negative Small	NS	trimf	-37.5, -12.5, 0
4	Zero	Z	trimf	-12.5, 0, 12.5
5	Positive Small	PS	trimf	0, 12.5, 37.5
6	Positive Medium	PM	trimf	12.5, 37.5, 75
7	Positive Big	PB	trapmf	37.5, 75, 100

Table 7. Fuzzy rule base

a / ***b***	**NB**	**NM**	**NS**	**Z**	**PS**	**PM**	**PB**
PB	Z	PS	PS	PM	PM	PB	PB
PM	NS	Z	PS	PS	PM	PM	PB
PS	NS	NS	Z	PS	PS	PM	PM
Z	NM	NS	NS	Z	PS	PS	PM
NS	NM	NM	NS	NS	Z	PS	PS
NM	NB	NM	NM	NS	NS	Z	PS
NB	NB	NB	NM	NM	NS	NS	Z
$\boldsymbol{a = V_{DC-error}; b = \Delta V_{DC-error}}$							

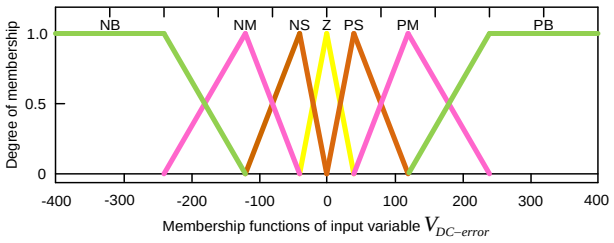


Figure. 5 Input MFs of $V_{\mathrm{DC-error}}$

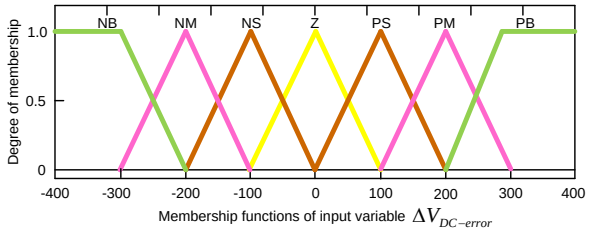


Figure. 6 Input MFs of $\Delta V_{\mathrm{DC-error}}$

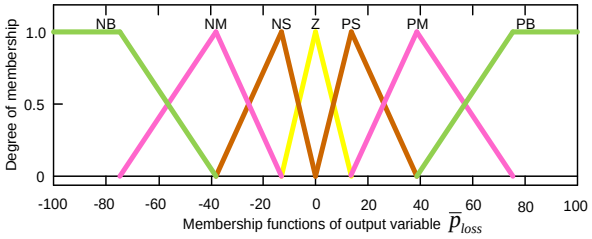


Figure. 7 Output MFs of $\bar{p}_{loss}$

$(\bar{p}_{loss})$ are determined using the FLC method.

Eq. (13), which determines the compensation current $(i^*_{\alpha\beta})$, uses the $\bar{p}_{loss}$ value as an input variable. Numerous input variables are computed, transformed into linguistic variables, and referred to as membership functions (MFs) throughout the fuzzification process. Seven linguistic variables are derived from the values of one output variable and two input variables in MF, respectively. NB (Negative Big), NM (Negative Medium), NS (Negative Small), Z (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big) are the crips input variables used in the $V_{DC-error}$ and $(\Delta V_{DC-error})$. With limits ranging from -400 to 400, the combined triangular and trapezoidal MF models make up the crips variable model of the two input variables. The crips output variable $\bar{p}_{loss}$, is similar to the crips input variable in that it combines trapezoidal and triangular MF, but its MF limit is different—it falls between -100 and 100. In this paper, a combination of triangular and trapezoidal for input and output MFs is proposed. The triangular shape represents fuzzy numbers, while the trapezoidal shape represents fuzzy intervals. The reason for using a combination of two models is that it has the simplest form, is easy to implement in the system, and produces faster computing times than other MFs [25].

The same linguistic variables are contained in both the crips input and output variables. Figs. 5-7 displays the FLC's MF input $V_{DC-error}$, MF input $(\Delta V_{DC-error})$, and MF output $\bar{p}_{loss}$ in that order. The linguistic functions and bounds of each Mamdani-FIS set, which has two input variables and one output variable, are displayed in Tables 4-6. Following the extraction of $V_{DC-error}$ and $\Delta V_{DC-error}$. The two MF inputs are transformed into linguistic variables and employed as FLC input functions. The MF output with an inference block and fuzzy rule base 49 is shown in Table 7. The MF $\bar{p}_{loss}$ output generated from linguistic variables is then changed to be transformed back into numeric variables via the defuzzification step. The $\bar{p}_{loss}$ value then functions as an input variable to reduce source current harmonics and control the hysteresis current to provide a trigger pulse to the IGBT in Sh-AF in UPQC. Then, from the six identified CSs, the UVTG control on the Se-AF is responsible for managing the load voltage in order to enhance the single-phase system's power quality.

2.5 True power-factor dan harmonics

The true power-factor (PF_{true}) in the non-sinusoidal case has a relationship with the value of the current harmonics. The actual power-factor value as a function of the current harmonic value due to the non-sinusoidal case i.e. distorted sources and non-linear loads are expressed in Eq. (16) as follows [20]:

$$PF_{true} = \frac{1}{\sqrt{1+(THD_I/100)^2}} \tag{16}$$

where, PF_{true} and THD_I, respectively are the actual power-factor and THD current values.

2.6 Percentage of Sag/Swell and interruption deviation

IEEE Std. 1159-1995 (Voltage sag/swell and interrupt monitoring) has been validated [26]. This regulation governs the definitions, tables, and specifications for sag/swell voltage decreases and interruption voltages according to typical duration, typical magnitude, and categories (instantaneous, momentary, and temporary). With the pre-disturbance voltage value established at 220 V, Eq. (17) below indicates the V_D value, which represents the percentage change in sag/swell voltage disturbance and interruption voltage.

$$V_D\ (\%) = \frac{|Vpre\_disturb - V\_disturb|}{Vpre\_disturb} \qquad (17)$$

Where $V_{pre-distrub}$ which is selected to be 220 V, is the load voltage prior to the sag/swell disturbance and interruption voltage occurring. Additionally, $V_{disturb}$, which varies depending on the kind of disturbance, is the load voltage following sag/swell disturbance and interruption voltage.

3. Results and discussion

3.1 Simulation result

The proposed model is a UPQC circuit connected to a single-phase system (on-grid) via a DC link circuit without capacitors. There are two single-phase UPQC configurations used i.e. (1) single-phase UPQC connected to the PV and (2) single-phase UPQC connected to the PV-BES combination. Each combination is described in six Case Studies (CSs) simulations of disturbances i.e. CS 1 (S-Sag-NL-PV), CS 2 (S-Swell-NL-PV), CS 3 (S-Inter-NL-PV), CS 4 (S-Sag-NL-PV-BES), CS 5 (S-Swell-NL-PV-BES), and CS 6 (S-Inter-NL-PV-BES). Each single-phase UPQC combination uses FLC with Mamdani-FIS and is validated by PI control for a total of 12 CSs.

Each model combination is performed using Matlab Simulink in accordance with the given CS to produce a curve, i.e. V_S, V_{SE}, V_L, I_S, I_{SH}, and I_L. The magnitudes of V_S, V_{SE}, V_L, I_S, I_{SH}, and I_L are determined using this graph. The values of $THD\ V_S$, $THD\ V_{SE}$, $THD\ V_L$, $THD\ I_S$, $THD\ I_{SH}$, and $THD\ I_L$ are then ascertained using the output of the Matlab Powergui simulation, which was conducted using the previously plotted curves for each parameter. For each CS, measurements of the nominal current, voltage parameters, and THD value were made for three cycles, ranging from 0.22 to 0.28 s.

The next step is to run simulations on six CSs to generate curves and ascertain the values of the following: PV power (P_{PV}), DC power (P_{DC}), BES State of Charge (SoC), PV voltage (V_{PV}), DC voltage (V_{DC}), PV current (I_{PV}), BES voltage (V_{BES}), BES current (I_{BES}), BES power (P_{BES}) and load active power (P_L). Since the UPQC circuit does not require capacitor, PV power, which is the PV output power following the DC-DC boost converter circuit, has the same value as DC power. After taking these factors into account, the measurements of the ten parameters are then expressed in eight measurement result graphs, which are completed in one cycle at t = 0.25 seconds and include, i.e., V_{PV}/V_{DC}, I_{PV}, V_{BES}, I_{BES}, P_{BES}, P_{PV}/P_{DC}, SoC, and P_L. For CS 1 through CS 6, the overall simulation time for disturbances is t=0.5 s, and the duration of the disturbances ranges from 0.15 to 0.35 s.

Fig. 8 shows the performance of V_S, V_{SE}, V_L, I_S, I_{SH}, and I_L. on a single-phase UPQC connected system using the FLC method on CS 4, CS 5, and CS 6.

Fig. 8.a illustrates how the source voltage (V_S) in CS 4 decreases by 50% from 220 V to 113.6 V over the 0.15–0.35 s portion of the whole simulation length, t = 0.5 s. The combined power of PV and BES is less able to generate voltage under these conditions. The maximum DC voltage (V_{DC}), as it can only inject a 101.3 V series voltage (V_{SE}) on a single-phase Se-AF using a series transformer. Thus, the single-phase system's load voltage (V_L) significantly dropped to 218.1 V during the CS 4 period. In the end, the load current (I_L) decreased marginally to 3,490 A due to the decrease in load voltage (V_L) Therefore, the THD of the source current (I_S) can be reduced to 0.48% compared to the existing THD load current (I_L) of 2.55% by injecting a shunt compensation current (I_{SH}) of 22.80 A and a THD of 0.38% in the opposite phase direction at the same CS as the single-phase UPQC-PV-BES configuration.

Fig. 8.b illustrates how the source voltage (V_S) in CS 5 increases by 50% from 220 V to 321.3 V throughout the 0.15–0.35 s of the entire simulation length, t = 0.5 s. Under these circumstances, the PV-BES combination can generate a DC voltage (V_{DC}) and inject a 99.3 V series compensation voltage (V_{SE}) at Se-AF via a series transformer. The single-phase system's load voltage (V_L) increased by 225.4 V during the CS 5 timeframe. The load current (I_L) increased marginally to 3,662 A as a result of the increase in load voltage (V_L). On the other hand, at the same CS, the single-phase UPQC-PV-BES configuration is capable of injecting a shunt

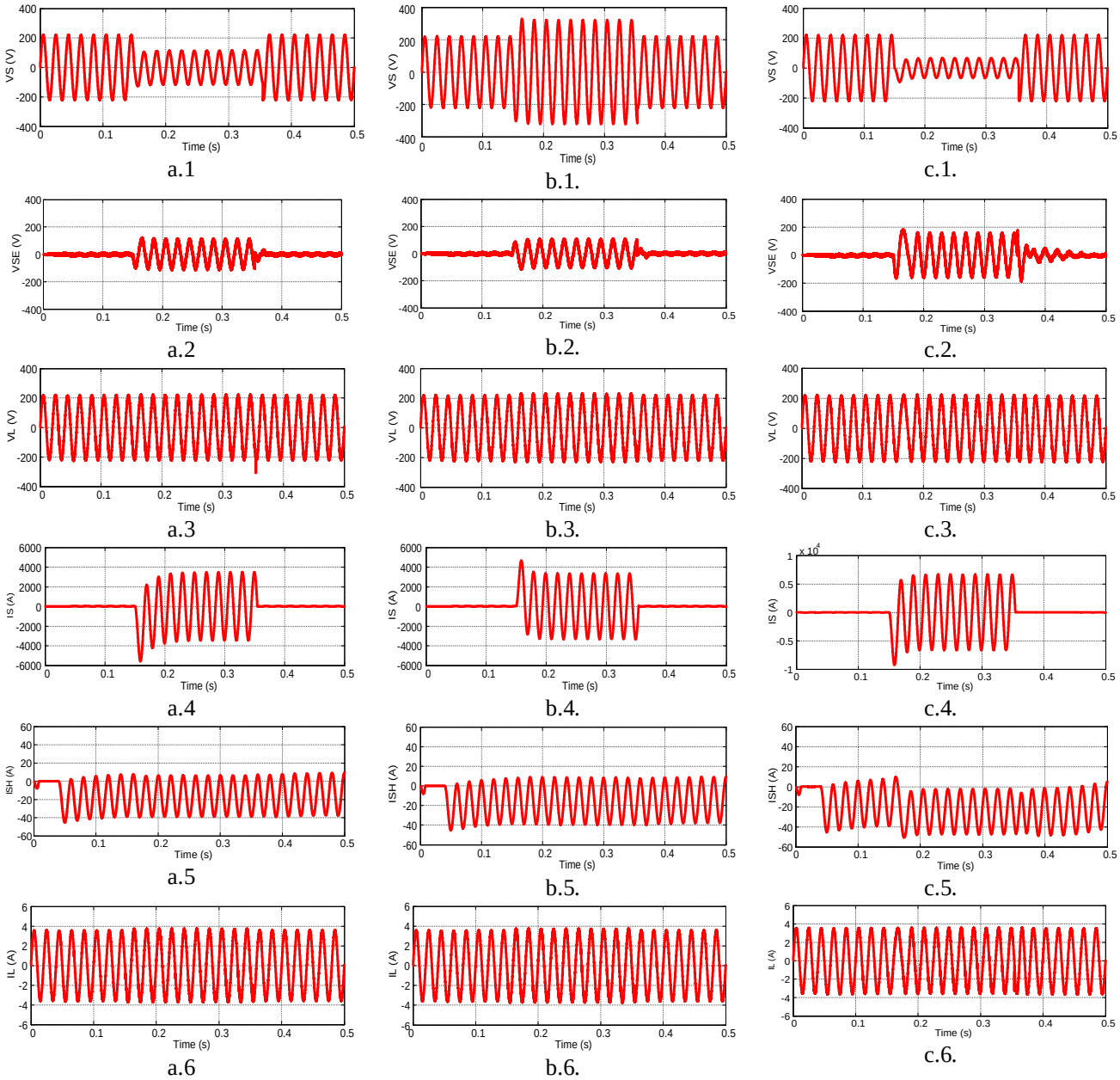


Figure. 8 Performance of V_S, V_{SE}, V_L, I_S, I_{SH} and I_L from singe phase UPQC using FLC method in: (a) CS 4, (b) CS 5, and (c) CS 6

compensation current (I_{SH}) of 23.10 A and a THD of 0.39% in the opposite phase direction to reduce the THD of the source current (I_S) by 0.08% compared to the load current THD (IL) of 1.97%.

Fig. 8.c illustrates how the source voltage (V_S) in CS 6 decreases from 220 V to 66.20 V during the 0.15–0.35 s portion of the whole duration t = 0.5 s. The PV-BES combination can sustain the voltage under these circumstances. The DC voltage (V_{DC}) is able to apply a 149.0 V series compensation voltage (V_{SE}) to the Se-AF using a series transformer. The single-phase system's load voltage (V_L) dropped by 215.3 V over the CS 6 period. In the end, the load current (I_L) decreased marginally to 3,497 A due to the decrease in load voltage (V_L). The single-phase UPQC-PV-BES configuration, on the other hand, can reduce the THD of the source current (I_S) to 0.01% in contrast to the load current (I_L) THD of 3.00% at the same CS by injecting a shunt compensation current (I_{SH}) of 22.56 A and a THD of 3.07% in the opposite phase direction.

Fig. 9 shows the performance of V_{PV}/V_{DC}, I_{PV}, V_{BES}, I_{BES}, P_{BES}, P_{PV}/P_{DC}, SoC, and P_L on a single-phase UPQC connected system using the FLC method on CS 4, CS 5, and CS 6.

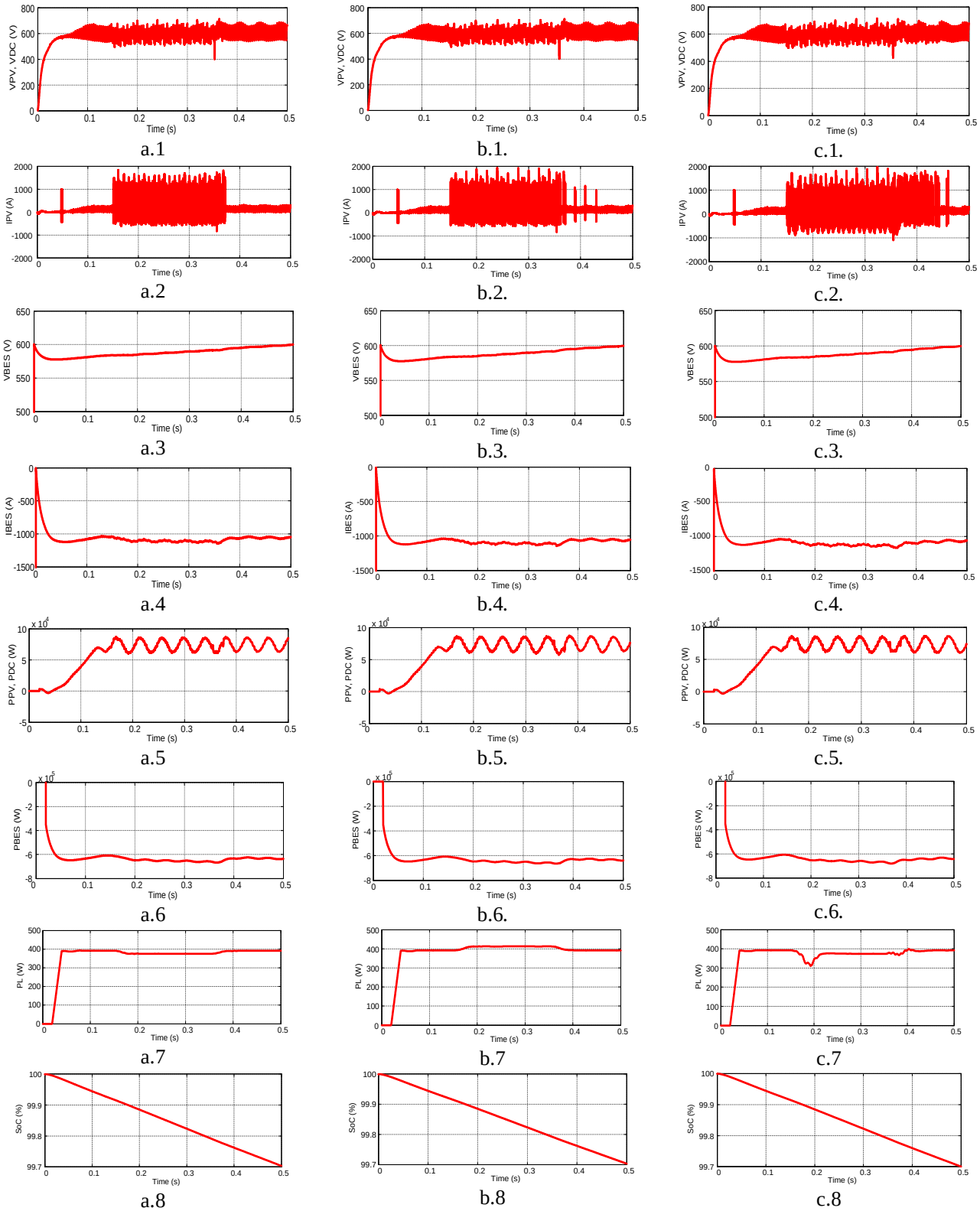


Figure. 9 Performance of V_{PV}/V_{DC}, I_{PV}, V_{BES}, I_{BES}, P_{BES}, P_{PV}/P_{DC}, SoC, and P_L base FLC method in: (a) CS 4,(b) CS 5, and (c) CS 6

Fig. 9.a illustrates how the DC voltage (V_{DC}) in CS 4 and the FLC technique is equal to the PV voltage (V_{PV}) of 564.7 V since the single-phase UPQC-PV-BES system does not employ a DC-link capacitor. The PV generates 82.59 A of output current (I_{PV}) and 78020 W of power output (P_{PV}), The BES each release 653,200 W of power and 1104 A of current at a 99.85% SoC under the same

circumstances. Additionally, Fig. 9.a demonstrates that the PV output power (P_{PV}) value is equal to the DC power (P_{DC}) value and, when combined with BES, can distribute 375.4 W of load power (P_L).

Fig. 9.b illustrates how the DC voltage (V_{DC}) in CS 5 and the FLC technique is equal to the PV voltage (V_{PV}) of 559.9 V since the single-phase UPQC-PV-BES system does not employ a DC-link capacitor. The PV generates 79690 W of power output (P_{PV}) and 36.58 A of current flow (I_{PV}) respectively. The BES each discharge 651,000 W of power (P_{BES}) and 1093 A of current (I_{BES}) at a 99.85% SoC under the same circumstances. Additionally, Fig. 9.b demonstrates that the PV output power (P_{PV}) value is equal to the DC power (P_{DC}) value and, when combined with BES, can distribute 412.2 W of load power (P_L) Fig. 9.c illustrates how the DC voltage (V_{DC}) in CS 6 and the FLC technique is equal to the PV voltage (V_{PV}) of 531.3 V since the single-phase UPQC-PV-BES system does not employ a DC-link capacitor. The PV plant generates 80910 W of power output (P_{PV}) and 750.7 A of current flow (I_{PV}) respectively. The BES each released 659,800 W of power (P_{BES}) and 1119 A of current(I_{BES}) at a 99.85% SoC under the same circumstances. Additionally, Fig. 9.C demonstrates that the PV output power (P_{PV}) value is equal to the DC power (PDC) value and, when combined with BES, can distribute 375.3 W of load power (P_L)

3.2 Analysis of voltage and current magnitude, harmonics, power-factor correction, PV power, BES power, and load power

Using the same procedure, all parameter values, i.e., V_S, V_{SE}, V_L, I_S, I_{SH}, and I_L, V_D, and THD, as well as PF_S and PF_S, are presented in Tables 8 and 9. The values of V_{PV}/V_{DC}, I_{PV}, V_{BES}, I_{BES}, P_{BES}, P_{PV}/P_{DC}, SoC, and P_L in each CS and single-phase UPQC configuration using PI and FLC methods, respectively, are also presented fully in Table 10.

Table 8 demonstrates that the system combining PI control with single-phase UPQC is still able to maintain a load voltage (V_L) between 214.8 and 225.4 V in CS 1 to CS 6. Using the same control as the FLC technique, CS 1 through CS 6 can sustain a slightly higher voltage load (V_L) of 214.9 V to 225.4 V. Additionally, Table 8 demonstrates that the system employing PI control and single-phase UPQC at CS 1 to CS 6 can support load current (I_L) ranging from 3,490 A to 3,662 A. The CS 1 through CS 6 faults can generate somewhat bigger load currents (I_L) between 3,497 A and 3,662 A. Additionally, Table 8 demonstrates that the system utilizing PI control and single-phase UPQC at CS 1 to CS 6 can cause load voltage change (V_D) fluctuations ranging from 0.82% to 2.45%. CS 1 to CS 6 disturbances can result in reduced load voltage (V_D) variations of 0.68% to 2.45% in the same system with FLC.

As illustrated in Fig. 10, in CS 4, the single-phase UPQC-PV-BES configuration employing the FLC method may generate a source current (I_S) THD of 0.48%, which is less than the load current (IL) THD of 2.55%. According to IEEE 519 Standard, the single-phase UPQC configuration provided by PV-BES employing the FLC method can inject shunt compensation current (I_{SH}) to greatly minimize the source current (I_S) THD. PV-BES provides the single-phase UPQC setup in CS 4, as illustrated in Fig. 11. The load voltage (V_L) THD of 2.46% that the single-phase UPQC-PV-BES can produce is greater than the source voltage (V_S) THD of 0.18%. The IEEE-519 Standard states that even though the THD value of the load voltage (V_L) is still marginally greater than the THD of the source voltage (V_S), the values of both components are within the THD voltage limit.

The system that uses PI control in conjunction with single-phase UPQC on CS 1 through CS 6 can produce load voltage THD (VL) ranging from 0.85% to 4.24%, as Table 9 demonstrates. With the FLC approach, CS 1 through CS 6 can lower the load voltage's THD from 0.81% to 3.07% in the same system. The single-phase UPQC system with PI control at CS 1 to CS 6 may produce THD (IS) source current in the range of 0.08% to 1.08%, as Table 9 demonstrates. Using the FLC approach in the same configuration, CS 1 through CS 6 can lower the source current (I_S) THD by 0.01% to 0.48%. The load power-factor (PF_L) produced by the single-phase UPQC system with PI control at CS 1 to CS 6 ranges from 0.99912 to 0.99999, as Table 9 demonstrates. Using the FLC approach in the same arrangement, CS 1 through CS 6 yield a higher load power-factor (PF_L) ranging from 0.99955 to 0.99997. Table 9 further demonstrates that the source power-factor (PF_S) may be improved between 0.99994 and 1.0000 by the single-phase UPQC system with PI control at CS 1 to CS 6. Using the FLC approach in the same configuration, CS 1 through CS 6 can increase the source power-factor (PF_S) by 0.99999 to 1.0000. As a result, the single-phase UPQC system at CS 1 to CS 6 can serve as a power-factor correction or enhance the source power-factor (PF_S), depending on whether it is powered by PV or PV-BES.

Table 8. Magnitude of voltage, current, load voltage disturb using single-phase UPQC

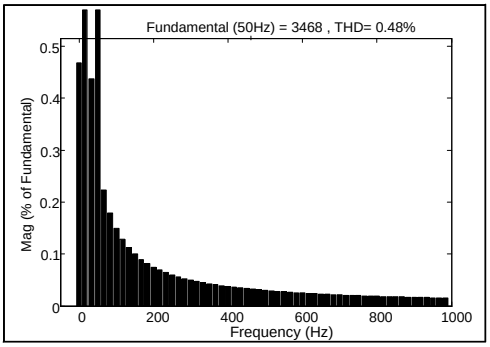
Case Studies	V_S (V)	V_L (V)	I_S (A)	I_L (A)	V_{SE} (V)	I_{SH} (A)	V_D (%)
Proportional Integral Controller							
1	113.6	218.1	3469	3.543	104.6	-23.14	0.86
2	321.3	221.8	3333	3.604	99.50	-23.54	0.82
3	66.20	218.2	6663	3.546	152.0	-22.91	0.82
4	113.6	214.8	3468	3.490	101.3	-22.79	2.36
5	321.3	225.4	3333	3.662	95.97	-23.91	2.45
6	66.62	215.0	6664	3.492	148.7	-22.56	2.27
Fuzzy Logic Controller							
1	113.6	218.1	3469	3.543	104.5	-23.14	0.86
2	321.3	221.8	3333	3.605	99.48	-23.54	0.82
3	66.61	218.5	6663	3.550	152.2	-22.90	0.68
4	113.6	214.9	3468	3.490	101.3	-22.80	2.32
5	321.3	225.4	3333	3.662	99.3	-23.10	2.45
6	66.20	215.3	6664	3.497	149.0	-22.56	2.14

Table 9. Voltage THD, current THD, source PF, and load PF using single-phase UPQC

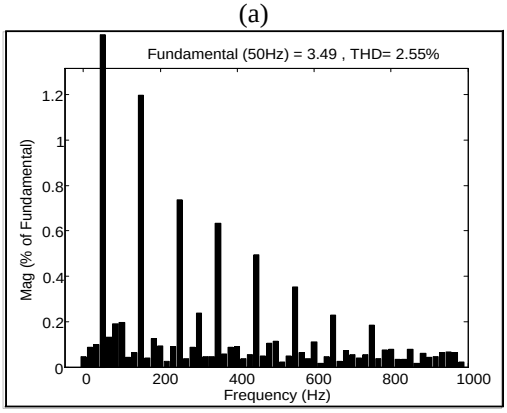
Case Studies	THD of V_S (%)	THD of V_L (%)	THD of I_S (%)	THD of I_L (%)	THD of V_{SE} (%)	THD of I_{SH} (%)	PF_S	PF_L
Proportional Integral Controller								
1	0.17	0.97	1.08	1.11	3.36	0.47	0.99994	0.99994
2	0.01	0.85	0.09	0.35	3.45	0.35	1.00000	0.99999
3	0.10	3.61	0.08	3.62	5.46	4.51	1.00000	0.99935
4	0.23	2.47	1.08	2.56	12.72	0.52	0.99994	0.99967
5	0.01	2.28	0.08	1.97	12.92	0.39	1.00000	0.99981
6	0.10	4.24	0.08	4.19	9.46	4.55	1.00000	0.99912
Fuzzy Logic Controller								
1	0.09	0.88	0.48	1.04	3.29	0.29	0.99999	0.99995
2	0.00	0.81	0.02	0.76	3.48	0.23	1.00000	0.99997
3	0.02	2.20	0.01	2.21	3.60	3.12	1.00000	0.99976
4	0.18	2.46	0.48	2.55	12.70	0.38	0.99999	0.99968
5	0.01	2.28	0.08	1.97	3.45	0.39	1.00000	0.99981
6	0.02	3.07	0.01	3.00	8.43	3.07	1.00000	0.99955

Table 10. PV output, BES output and load power using single-phase UPQC

Case Studies	V_{PV}, V_{DC} (V)	I_{PV} (V)	V_{BES} (V)	I_{BES} (W)	P_{BES} (W)	SoC (%)	P_V (W)	P_L (W)
Proportional Integral Controller								
1	189.0	450.0	600.4	0	0	100	72090	386.7
2	174.4	180.5	600.4	0	0	100	74140	399.6
3	251.5	102.5	600.4	0	0	100	75680	386.8
4	564.7	82.59	587.3	-1104	-653200	99.85	78020	375.4
5	559.8	36.58	587.5	-1093	-651000	99.85	79590	412.2
6	531.3	-750.7	587.0	-1995	-659800	99.85	80910	375.3
Fuzzy Logic Controller								
1	189.0	450.0	600.4	0	0	100	72090	386.7
2	174.4	180.5	600.5	0	0	100	74140	399.6
3	251.5	102.5	600.4	0	0	100	75680	386.8
4	564.7	82.59	587.3	-1104	-653200	99.85	78020	375.4
5	559.9	36.58	587.5	-1093	-651000	99.85	79590	412.2
6	531.3	-750.7	587.0	-1119	-659800	99.85	80910	375.3

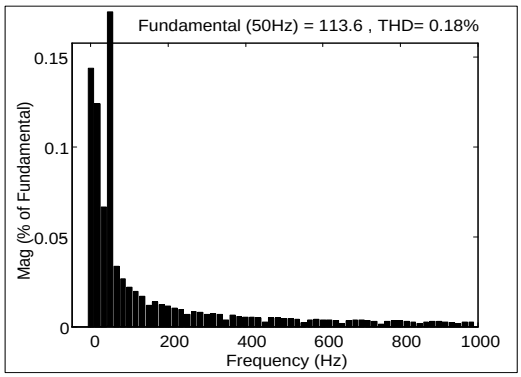


(a)

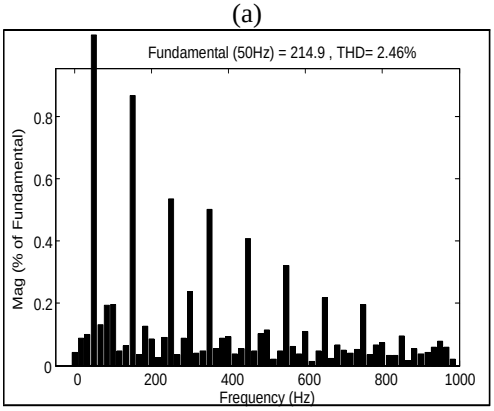


(b)

Figure. 10 Harmonic spectra: a) I_S and (b) I_L at CS 4 (S-Sag-NL-PV-BES) using single-phase UPQC with FLC



(a)



(b)

Figure. 11 Harmonic spectra: (a) V_S and (b) V_L at CS 4 (S-Sag-NL-PV-BES) using single-phase UPQC with FLC

Table 10 demonstrates that the same PV voltage (V_{PV}) and DC voltage (V_{DC}) may be produced by the single-phase UPQC system provided by PV and PV-BES employing PI and FLC at CS 1 to CS 6. PV and PV-BES are the sources of PV current (I_{PV}) that flow in the DC-link without a capacitor in UPQC are able to produce the same amount of DC power (P_{DC}) and PV power (P_{PV}). In the single-phase UPQC combination, PV and PV-BES supply CS 3 and CS 6 with PI control and FS, demonstrating their ability to inject the maximum power while maintaining active load power (P_L) distribution with values nearly equal to CS 1, CS 2, CS 4, and CS 5 conditions.

3.3 Analysis of load voltage harmonics, source current harmonics, source power-factor, load voltage disturbance, and load active power

Fig. 12 shows the THD performance of VL from CS 1 to CS 6.

In a single-phase UPQC arrangement with PI/FLC control, Fig. 12 demonstrates that CS 3 and CS 6 can generate the highest THD load voltage ($THD\ V_L$) (above 2.20%) when compared to other CS. With respect to other CS, the single-phase UPQC setup with PI/FLC control in CS 2 and CS 5 may generate the lowest THD load voltage ($THD\ V_L$) (above 0.81%). FLC can generate a lower THD load voltage than PI control in a single-phase UPQC system with CS 1 to CS 6. The system may provide THD load voltage ($THD\ V_L$) below the IEEE 519 limit by using single-phase UPQC on CS 1 to CS 6 with PI/FLC control.

Fig. 13 shows the THD of I_S performance from CS 1 to CS 6.

The single-phase UPQC system at CS 1 and CS 4 with PI/FLC control may produce the maximum source current THD (THD above 0.48%), as Figure 13 demonstrates. However, the PI/FLC-controlled

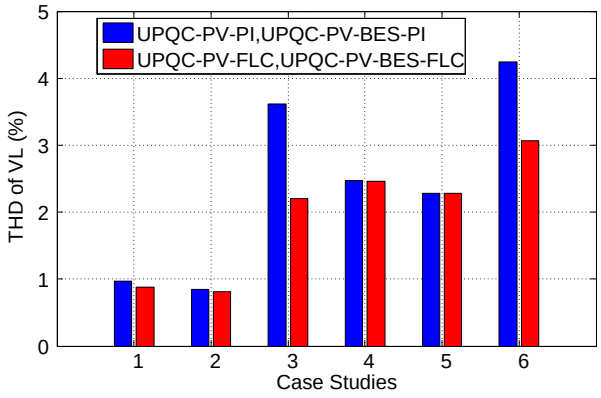


Figure. 12 THD of V_L performance for CS 1 to CS 6

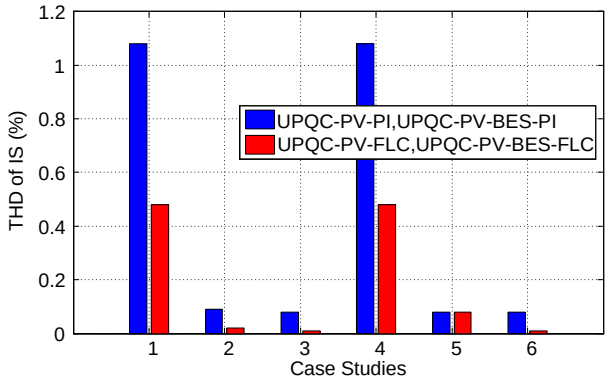


Figure. 13 THD of I_S performance for CS 1 to CS 6

single-phase UPQC system on CS 3 and CS 6 can produce the lowest source current THD (THD above 0.01%). A reduced source current THD can be achieved by the system that uses single-phase UPQC on CS 1-6 with FLC control as opposed to PI control. Shunt compensation current (I_{SH}) can be injected into the load bus by the single-phase UPQC system for setup, fault, and control to greatly minimize the THD of the source current (I_S) compared to the load.

Fig. 14 shows the performance of source power-factor (PF_S) for CS 1 to CS 6.

The system with PI/FLC and single-phase UPQC on CS 2, 3, 5, and 6 is able to achieve the maximum source power-factor (PF_S of 1.0), as Figure 14 demonstrates. On the other hand, the system may produce the lowest source power-factor (PF_S over 0.99994) by using single-phase UPQC with PI/FLC on CS 1 and CS 4. The system, which can produce somewhat greater PF_S than PI control, uses single-phase UPQC on CS 1-6 with FLC.

Fig. 15 shows the performance of load voltage change (V_D) for CS 1 to CS 6.

In a system with a single-phase UPQC configuration with PI/FLC control, Fig. 15 demonstrates that CS 4-6 can generate load voltage fluctuations (V_D) greater than 2.14%. It can generate a 0.68% change in load voltage(V_D) at CS 1-3 with PI/FLC. The calculation shows that the maximum voltage change limit ($V_D \leq 5\%$) is still reached by the load voltage change in single-phase UPQC using two distinct controls and six CS.

Fig.16 shows the P_L performance for CS 1- 6.

The system that uses PI/FLC control and single-phase UPQC on CS 1 through CS 6 can produce the same load of active power (P_L) as shown in Fig. 16. The system on CS 2 and CS 5 that uses single-phase UPQC is able to absorb more active load power than the systems on CS 1, CS 3, CS 4, and CS 6 (P_L over

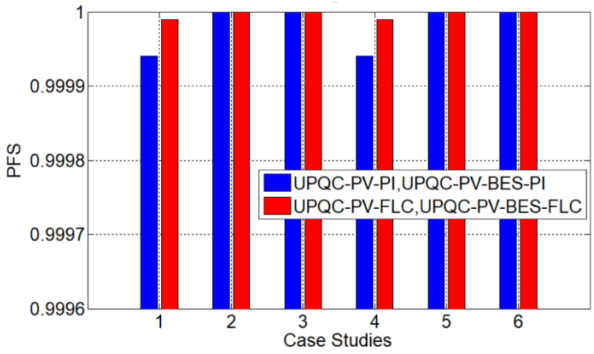


Figure. 14 PF_S performance for CS 1 to CS 6

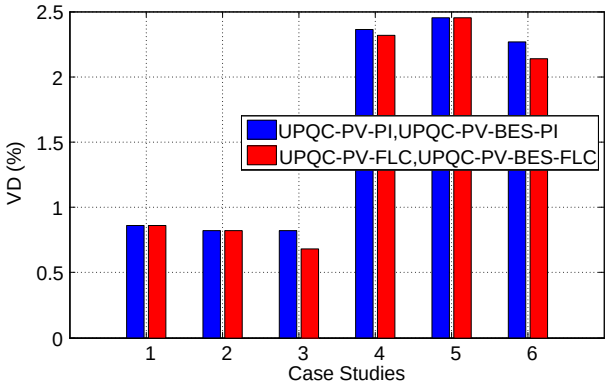


Figure. 15 V_D performance for CS 1 to CS 6

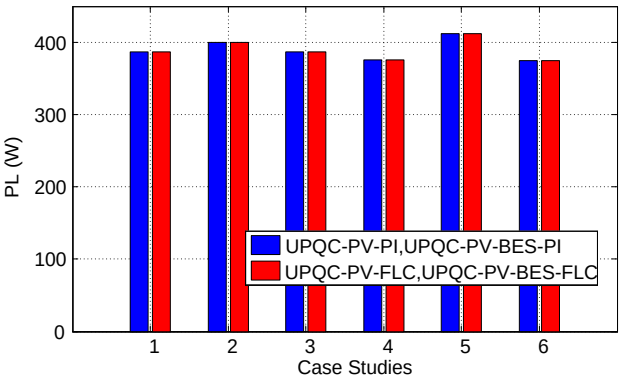


Figure. 16 P_L performance for CS 1 to CS 6

399.6 W). This is the difference PV and PV-BES, which experience swell voltages can absorb more load active power (P_L) than systems that suffer sag voltages and interruption voltages, provide systems with single-phase UPQC. The system uses single-phase UPQC with PI/FLC on CS 3 and CS 6, which is capable of distributing active load power with values close to CS 1 and CS 4.

3.4 Validation of proposed system

The system validation results of this research are displayed in Table 11, and compared to six selected

Table 11. Comparison with selected method

Authors	Method	THD V_L (%)		THD I_S (%)		PF_S	Disturbance Mitigation						UPQC Injected by	DC Link Capacitor	BES
		Nominal Value	Met IEEE 519	Nominal Value	Met IEEE 519		Sag	Swell	Interruption	Unbalance Source/Load	LL	NL			
[9]	1PH-UPQC-PV PLL Less d-q	4.72%	✓	1.45%	✓	X	✓	✓	X	X	✓	✓	PV	✓	X
[14]	1PH-UPQC-PV PLL Notch Filter	X	X	2.8%	✓	X	✓	✓	X	X	✓	✓	PV	✓	X
[16]	Modulated-3PH-UPQC-Hybrid AC/DC Microgrid	4.4% (ph. A)	✓	5.3% (ph. A)	X	X	X	X	X	✓	X	✓	X	✓	X
[17]	3PH-UPQC-PV-WT	1.4% (ph. A)	✓	29% (ph. A)	X	0.99	X	X	X	X	X	✓	PV and WT	✓	X
[18]	3PH-UPQC-MMC	3.89% (ph. A)	✓	2.87% (ph. A)	✓	X	✓	X	X	X	X	✓	X	✓	X
[19]	1PH-UPQC-PV-FLC	0.79%	✓	0.01%	✓	X	✓	✓	✓	X	✓	✓	PV	X	X
Proposed Study	**1PH-UPQC-PV-BES-FLC**	**2.28%**	✓	**0.01%**	✓	**1.0**	✓	✓	✓	**X**	**X**	✓	**PV**	**X**	✓
	Note: ✓ = available; X = not available														

methods. The parameters that are being monitored include the kind of disturbance mitigation, i.e., sag, swell, interruption, unbalanced source/load, LL, and NL, power quality parameters, i.e., THD V_L, THD I_S, and PF_S, as well as the presence of BES, DC-link capacitor, and RE source injected to UPQC. The 1PH-UPQC-PV-PLL Less d-q architecture was proposed by [9] for a single-phase distribution system. The minimum THD V_L and THD I_S values are 4.72% and 1.45%, respectively as well and both have met IEEE 519, as a result of the mitigation of the forms of disturbance i.e. sag, swell, LL, and NL. The model without BES, PV injection and a DC-link capacitor is used in the single-phase UPQC system. The 1PH-UPQC-PV PLL with the Notch Filter technique was proposed in [14]. Sag, swell, LL and NL interference, resulting in a THD I_S of 2.8% and meeting IEEE 519. The UPQC system uses PV injection and a DC-link capacitor, without BES. A hybrid AC/DC microgrid was used in the study of modulated-3PH-UPQC [16]. Unbalance load and NL are the two forms of interference that are mitigated. The system results in V_L and I_S of 4.4% and 5.3% (phase A), respectively. The second parameter has crossed the limit of IEEE 519. The UPQC system has a DC-link capacitor but no PV injection and BES.

An improvement in power quality using 3PH-UPQC-PV-WT has been observed in [17]. The type of interference that is mitigated is NL, so it produces THD V_L, THD I_S, and PF_S of 1.4% (phase A), 29% (phase A), and 0.99 respectively. Both THD parameters have met IEEE 519. The UPQC system uses a DC-link capacitor, PV-WT injection, and no BES. The power quality problems in distribution networks due to sag and NL using 3PH-UPQC-MMC have been investigated in [18]. The proposed UPQC topology is capable of producing THD V_L and THD I_S of 3.89% (phase A) and 2.87% (phase A), respectively as well as both have meet IEEE 519.

The UPQC system has a DC-link capacitor but no PV injection dan BES. Injection of PV-WT and without BES has been used in a 1PH-UPQC-PV-FLC system in [19] to serve LL and NL. Sag, swell, interruption, LL, and NL are the types of interference, resulting in a minimal THD V_L and THD I_S of 0.79% and 0.01%, respectively as well as both meet IEEE 519. PV injection, a DC-link capacitor, and no BES are used in the UPQC system.

The 1PH-UPQC-PV-BES-FLC system has been proposed by the authors to mitigate power quality on both the source and load sides. Sag, swell, interruption, and NL interference have resulted in THD V_L, THD I_S and PF_S are 2.28%, 0.01%, and 1.0 respectively. The proposed study of THD V_L value is marginally greater than those of [17, 19], while its THD I_S value is already lower than other topologies/methods, and both adhere to IEEE 519. The system is also able to produce the highest PF_S values in PFC compared to [17]. The system provides the best performance because it is also able to mitigate interruption voltage compared to [9, 14] and [16-18]. The UPQC system also has better circuit efficiency because without uses a DC-link capacitor compared to [9,14] and [16-18]. The PV array is also able to provide a more stable load power supply to the load when an interruption voltage/disconnecting occurs (CS 3 and CS 6) on the source side (off-grid mode) because PV power can be stored previously in the BES in the form of energy at night and is not dependent on weather factors compared to [19]

4. Conclusion

The combination of a 12 kW PV array and BES with an FLC coupled to a low voltage distribution system to power a single-phase UPQC system has been proposed. When disconnection occurs on the source side, BES serves to store PV power and offer a more reliable load power supply (off-grid mode). To circumvent the limitations of PI control in the determination of proportional and integral constants, the FLC approach with the Mamdani FIS is developed.

In single-phase UPQC systems from CS 1 to CS 6, FLC is able to produce a lower THD of load voltage and source current, as well as a higher PF_S compared to PI control. At CS 6, PI control on single phase UPQC-PV-BES produces THD V_L, THD I_S, and PF_S respectively 4.24%, 0.08%, and 1.0. Meanwhile, the same system using FLC produces values of 3.07%, 0.01%, and 1.0, respectively. The system using single-phase UPQC on CS 1 to CS 6 with PI/FLC control is capable of producing load voltage THD and source current THD below IEEE 519 limits. The system with a single-phase UPQC configuration with PI/FLC control shows that CS 4 to CS 6 is capable produces a change in load voltage disturbance (V_D) that is slightly greater than CS 1 to CS 3. From CS 1 to CS 6, FLC on single-phase UPQC produces V_D, i.e., 0.86%, 0.82%, 0.68%, 2.32%, 2.45%, and 2.14%, respectively. The system uses single-phase UPQC with PI/FLC control on CS 3 and CS 6 is capable of distributing load active power with values close to CS 1 and CS 4. At CS 1, CS 3, CS, 4 and CS 6, FLC on single-phase UPQC produces load active power (P_L), i.e., 386.7 W, 386.8 W, 375.4 W, and 375.3 W, respectively.

Elimination of the DC-link capacitor circuit in the PV-integrated single-phase UPQC system is expected to reduce system implementation costs. However, adding BES to the same system will certainly increase the overall system component costs. Determination of the optimal capacity of BES according to single-phase UPQC capacity using artificial intelligence control can be proposed as future work to solve this problem.

Appendix

Parameters of the single-phase UPQC-PV-BES. Single-phase Grid: RMS Voltage (L-N) $220\,Volt$, Frequency $50\,Hz$, Line Inductance $L_S = 0.1\,mH$; Sag Voltage Generation (CS 1 and CS 4): Sag Parallel Inductance $L_P = 0.1\,mH$, CB_1 = Sag Circuit Breaker with NO condition; Swell Voltage Generation (CS 2 and CS 5): Swell Voltage (L-N) $330\,Volt$, CB_2 = Swell Circuit Breaker with NO condition; Interruption Voltage Generation (CS 3 and CS 6): Circuit Breaker CB_3 = Interuption Circuit Breaker with NO condition; Se-AF: Series Inductance L_{SE} = 0.0015 mH, MOSFETs (MO_1, $MO_2, MO_3, and\ MO_4$); Sh-AF: Shunt Inductance L_{Sh} = 30 mH, IGBTs (IG_1, $IG_2, IG_3, and\ IG_4$); Series Transformer: Rating kVA $1000\,kVA$, Frequency $50\,Hz$, Transformation Rating (N_1/N_2) 1 : 1, Series Ripple Filter $C_{SE} = 4700\,\mu F$; Load Impedance $R_C = 1\,\Omega$ and Load Inductance $L_C = 0.01\,mH$; Non-Linier Load (NL) : Four Bridge Rectifiers (Diodes) (S_1, $S_2, S_3, and\ S_4$) connected to $R_L = 60\,ohm$; and $L_L = 1\,mH$; DC Link: DC Voltage $V_{DC} = 400\,Volt$; BES: Type = Nickel Metal hydride, DC voltage = 400 volt, Rated Capacity = 40 Ah, Initial State of Charge = 100%, Inductance $L_1 = 6\,mH$, capacitance $C_1 = 200\,\mu F$; Solar Photovoltaic Array: Active Power $12\,kW$, Irradiance $1000\,W/m2$, Temperature $25^0\,C$, Maximum Power Point Tracking (MPPT) Perturb

and Observer; DC-DC Boost Converter: IGBT Internal Diode Resistance, $C_L = 2\,mF, R = 0.01\,\Omega$, and $L = 0.01\,H$; Proportional Integral: Proportional Gain (K_P)= 0.2, Integral Gain (K_I) =1.5; FLC: FIS Mamdani, Composition Max-Min, Defuzzification Max-Min; Input MFs: Error V_{DC} ($V_{DC-error}$) trapmf and trimf, Delta Error V_{DC} , ($\Delta V_{DC-error}$) trapmf and trimf; Output MFs: Instantaneous of Power Losses ($\bar{p}_{loss}$) trapmf and trimf.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Amirullah Amirullah and Adiananda Adiananda; methodology, Amirullah Amirullah and Adiananda Adiananda; software, Amirullah Amirullah and Adiananda Adiananda; validation, Amirullah Amirullah; formal analysis, Amirullah Amirullah and; investigation, Amirullah Amirullah; resources, Amirullah Amirullah; data curation, Amirullah Amirullah; writing—original draft preparation, Amirullah Amirullah; writing—review and editing, Amirullah Amirullah and Adiananda Adiananda; visualization, Adiananda Adiananda; supervision, Amirullah Amirullah; project administration, Amirullah Amirullah; funding acquisition, Amirullah Amirullah. All authors have read and approved the final manuscript.

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