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Designing A Multi-Frequency Low Power Low-Density Parity Check (LDPC) Encoder with A Dynamic Voltage and Frequency Scaling (DVFS) Approach

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Abstract: Low density parity check (LDPC) codes are highly regarded for their exceptional error correction capabilities, making them a preferred choice for error correction coding (ECC) in modern communication standards. These codes are implemented in specialized integrated circuits (ICs) that facilitate data transmission. However, the power requirements of complementary metal-oxide-semiconductor (CMOS) circuits, which operate across a wide frequency range, present a significant challenge for future communication systems. To address this challenge, this paper proposes a novel multi-frequency power reduction strategy for LDPC encoders. The strategy utilizes dynamic voltage and frequency scaling (DVFS), a well-established power reduction method in CMOS circuits. By combining DVFS with fuzzy logic control, the system optimizes the voltage supplied to the LDPC encoder, achieving substantial power reduction while maintaining coding efficiency, flexibility, and performance. The proposed approach dynamically adjusts the encoder's voltage levels based on real-time conditions, ensuring efficient power consumption across different frequencies. This innovative strategy aims to overcome the power challenges faced by future communication generations, which have been largely overlooked in previous research efforts. This paper aims to assess the effectiveness of a multi-frequency power reduction strategy for LDPC encoders. Through extensive analysis and evaluations, it demonstrates significant power reduction while maintaining LDPC coding efficiency. These findings contribute to the development of power-efficient LDPC encoder designs, meeting the evolving needs of communication systems. Results reveal the system's performance across different frequency ranges. In the low-frequency range (1 MHz to 100 MHz), a remarkable 90% power reduction is achieved. In the medium-frequency range (100 MHz to 1 GHz), the reduction is 50%, while in the high-frequency range (1 GHz to 5 GHz), it reaches 20% to 14.5%. Notably, the system operates most effectively in the low and medium frequency range, providing substantial power savings. These results highlight the potential of the multi-frequency power reduction strategy for LDPC encoders in addressing power challenges across different frequencies. The significant power reduction achieved demonstrates its effectiveness and adaptability to varying frequency demands. This contributes to the development of power-efficient LDPC encoder designs, optimizing performance and energy consumption in various communication systems.

Keywords: Low density parity check (LDPC), Forward error correction (FEC), Complementary metal-oxide-semiconductor circuits (CMOS), Dynamic voltage and frequency scaling (DVFS), Fuzzy logic controller (FLC).

1. Introduction

Low density parity check (LDPC) codes, initially developed by Gallager [1] in 1962 and later rediscovered by Mackay and Neal [2], have garnered significant attention as robust forward error correction (FEC) codes. These codes excel in high-speed data transmission, possess powerful error correction capabilities, and exhibit computational efficiency, allowing them to approach the Shannon limit with minimal performance loss. LDPC codes have found wide application in modern communication standards, including Wi-Fi, DVB-S2, IEEE 802.11n, 802.3an, 802.16a, Wi-MAX, and others. They are also strong contenders for next-generation mobile communication standards [3].

LDPC codes offer efficient encoding, fast decoding, low latency, robust error detection and correction, and require less interleaving compared to turbo codes. They are represented by using either a parity check matrix (PCM) or a Tanner graph, both of which offer graphical depictions of the code's structure [4]:

1. Parity check matrix (PCM): The parity check matrix is a binary matrix that defines the relationships between the parity checks and the bits in an LDPC code. The PCM is structured such that each row represents a parity check equation, and each column represents a bit variable. The elements of the matrix are either 0 or 1, indicating the presence or absence of a connection between a bit and a parity check equation. For example, consider an LDPC code with n bits and m parity checks. The PCM is an m x n matrix, where each row corresponds to a parity check equation and each column corresponds to a bit variable. The presence of a '1' in the matrix indicates that a bit participates in a particular parity check equation. The PCM allows for easy visualization and analysis of the code's structure, enabling efficient encoding and decoding algorithms. It helps in identifying the connections between bits and parity checks, facilitating the error correction process [5-6].

2. Tanner graph: A Tanner graph is a bipartite graph that represents the connections between bits and parity checks in an LDPC code. It provides a graphical representation of the code's structure, where nodes in the graph represent bits and parity checks, and edges represent the connections between them. In a Tanner graph, there are two sets of nodes: variable nodes and check nodes. Variable nodes represent the bits of the LDPC code, and check nodes represent the parity check equations. An edge between a variable node and a check node indicates that the corresponding bit participates in the respective parity check equation. By visualizing the LDPC code as a Tanner graph, the relationships between bits and parity checks become apparent, facilitating the understanding and analysis of the code's properties. The graph structure aids in the development of efficient decoding algorithms, such as belief propagation or message passing algorithms [7].

Both the parity check matrix and Tanner graph representations (see Fig. 1) provide valuable insights into the structure and connections of LDPC codes, enabling efficient encoding and decoding techniques. They play a crucial role in the design and analysis of LDPC codes for various communication applications.

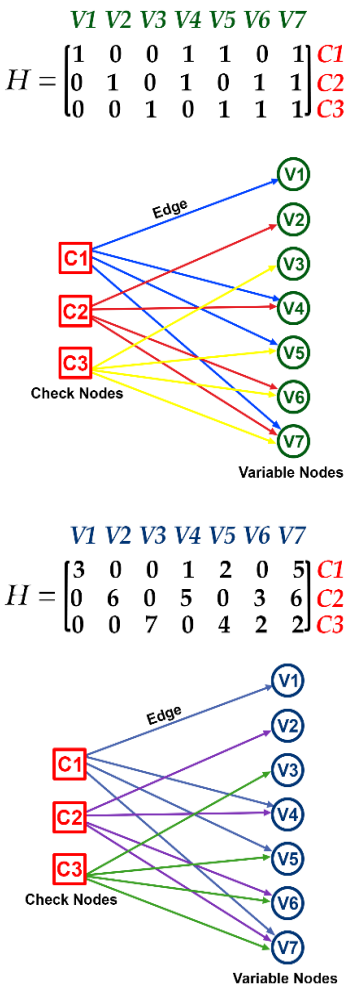

Figure. 1 LDPC representation as PCM and tanner graph [6]

In the realm of communication systems, LDPC codes and complementary metal-oxide-semiconductor (CMOS) circuits are interconnected components. LDPC codes are renowned for their exceptional error correction capabilities, while circuits, based on CMOS technology, serve as the fundamental building blocks of electronic devices. CMOS circuits enable the implementation of various functions in communication systems, including encoding, decoding, modulation, demodulation, and signal processing [8].

The link between LDPC codes and CMOS circuits lies in the integration of LDPC encoding and decoding algorithms into specialized integrated circuits (ICs) known as LDPC codecs. These codecs efficiently perform the necessary operations for LDPC codes. By harnessing CMOS technology, LDPC codecs can be designed to be compact, power-efficient, and seamlessly integrated into diverse communication systems, such as wireless networks, optical communication systems, and storage devices,

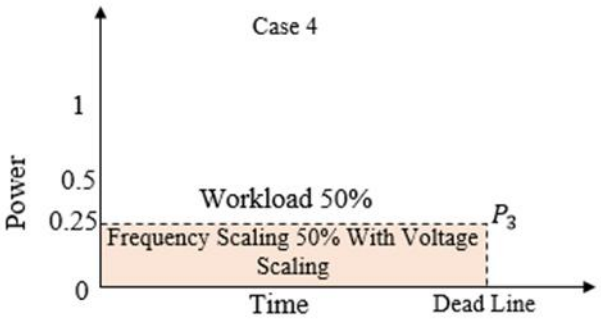

Figure. 2 Effect of DVFS approach on a random system [10]

thus enhancing data transmission reliability and performance. As communication systems demand higher data rates, achieving power efficiency becomes crucial. Researchers are actively exploring strategies to reduce the power consumption of CMOS circuits, including LDPC codecs [9].

Techniques like dynamic voltage and frequency scaling (DVFS) are used in power reduction for CMOS circuits, it reschedules the voltage along the task time so that, instead of completing the vital task as quickly as possible with high power consumption, the system will complete the required task in the exact required time with fewer overall power as shown in Fig. 2. This technique can be applied to channel encoders to optimize power consumption without compromising the error correction performance. In other words, LDPC codes and CMOS circuits are mutually dependent in communication systems. CMOS circuits provide the technological foundation for implementing LDPC codecs, enabling efficient encoding and decoding operations. Advances in CMOS technology, combined with power reduction strategies, contribute to the development of power-efficient LDPC codecs that archives performance requirements across various communication applications [10].

The rapid progress in CMOS technology and the implementation of power reduction strategies have played a pivotal role in the development of power-efficient LDPC codecs. These codecs as mentioned previously has significantly enhance data transmission reliability and performance across a wide range of communication applications. To achieve energy savings, a diverse set of energy-saving techniques tailored specifically for microprocessors and CMOS circuits have been introduced. These techniques include clock gating, which selectively disables clock signals to idle circuit components, and energy gating, which involves shutting down idle circuit blocks to conserve power [8].

Among these energy-saving techniques, DVFS stands out as particularly significant. DVFS, performed by a fuzzy controller, enables dynamic adjustment of the frequency and voltage of the LDPC encoder circuit in response to varying frequency. By controlling voltage levels, the fuzzy controller effectively reduces power consumption without sacrificing performance. This adaptability, achieved through the DVFS method implemented by the fuzzy controller, makes it an optimal approach for optimizing LDPC codec operations. It enables efficient power utilization while maintaining desired performance levels [11].

This research is extender from our previous study [12], focuses on investigating the influence of various frequency ranges (low, medium, and high) on the overall power consumption of LDPC encoder, regardless of the specific communication standard being used. The objective is to improve power efficiency by monitoring and controlling the effects of these frequency ranges. Through experimental analysis and performance evaluations, the study aims to determine the optimal frequency and voltage settings for different communication scenarios, carefully considering the trade-off between power consumption and performance. By identifying the most effective configurations, the research seeks to enhance the power efficiency of LDPC codecs and optimize their performance in real-world communication applications.

This paper is structured as follows: section 2 provides a brief overview of the relevant literature. Section 3 presents the implementation of the LDPC encoder and outlines its specifications. Section 4 focuses on power measurement for the LDPC encoder logic circuit. Section 5 introduces the proposed multi-frequency power controller system. section 6 presents the results of the aforementioned designs and includes comparisons with other power reduction approaches. Finally, section 7 offers the conclusion of the paper, summarizing the key findings and implications of the study.

2. Related work

The related work section of this paper delves into the extensive research conducted on LDPC codes, uncovering a wealth of knowledge and advancements in the field. Over the years, numerous encoding methods for LDPC codes have been developed, showcasing the ongoing efforts to enhance their performance and efficiency. This section specifically aims to provide a comprehensive overview of studies that have concentrated on reducing power consumption in LDPC encoders through various

methods. A comprehensive investigation of these studies is presented, shedding light on the diverse techniques employed to optimize power efficiency in LDPC encoders.

For example, the authors in [13] presented an efficient encoding method and low-complexity encoder architecture for quasi-cyclic low-density parity-check (QC-LDPC) codes in the 5th generation new radio (5G NR) standard. The proposed method achieved significant reduction in area and memory storage compared to existing approaches. The achieved throughput meets the requirements of the 5G NR standard. However, the study primarily focused on the encoding method and encoder architecture, without addressing other aspects such as error correction performance or system integration considerations.

In addition, authors in [14] introduced a novel partially parallel architecture for encoding QC-LDPC codes in 5G NR. This architecture improved hardware usage efficiency (HUE) while maintaining flexibility for all 5G NR codes. The processing schedule was optimized using a genetic algorithm to minimize encoding time. The optimized encoder demonstrated high throughput, low latency, and superior HUE compared to existing solutions. However, the proposed partially parallel architecture may introduce additional complexity to the LDPC encoder design, potentially impacting the overall design, verification, and implementation processes.

Likewise, in the study [15], the authors proposed a parallel QC-LDPC encoding algorithm for 5G NR. They developed a high area-efficient parallel encoder with configurable architecture, offering the advantages of parallel encoding and pipelined operations. The encoder demonstrated excellent performance and significant area efficiency. However, it should be noted that the focus of the paper was on the encoder's compatibility with different base graphs of 5G LDPC codes, limiting its applicability and adaptability to other coding schemes or applications outside the 5G context.

Similarly, to meet the requirements of low latency and high throughput in 5G NR data transmission, researchers in [16] aimed to minimize encoding hardware latency and reduce base station power consumption. Their design is flexible, accommodating various code lengths and rates needed for 5G NR. Experimental results demonstrated impressive data throughputs. However, the study may have focused primarily on low latency and high throughput, potentially overlooking other factors such as error correction performance, complexity, or system integration.

Based on different application, the paper [17] proposed a two-step encoding algorithm for IEEE 802.11n/ac/ax QC-LDPC codes, aiming to reduce complexity and enable full-parallel architectures. A VLSI encoding architecture based on XOR-gate trees was introduced, achieving high throughput rates with minimal hardware resources. However, it is important to conduct full verification and testing when integrating the proposed encoder into practical systems to ensure reliability and adherence to standard specifications. Any design or implementation flaws could potentially impact the overall performance and reliability of the LDPC encoding process.

Using different standard, the study [18] introduced an efficient reconfigurable encoder for the IEEE 1901 standard in power line communication (PLC). It aimed to meet the throughput requirement of the standard while being power- and area-efficient. The implementation results validated the effectiveness of the encoder. However, it's important to note that while the encoder was described as power- and area-efficient, there may be trade-offs in terms of encoding speed, latency, or error correction capabilities. These trade-offs could potentially impact the overall performance and reliability of the transmitted data.

Furthermore, in [19] the authors recommended an efficient and compact LDPC encoding process using pipelining design. Gauss Elimination was employed to reduce parity check matrices. Conventional and wave pipelining techniques were implemented to address area and latency issues. The proposed architectures were synthesized and implemented on an FPGA device, showcasing reduced power and area overheads. The Maximal Rate Pipelining (MRP) structure enabled LDPC Encoders to require less memory. However, the study didn’t discuss other performance metrics beyond power, area, and memory consumption.

Nevertheless, in the study [20], the authors presented an alternative approach for deploying LDPC coding in resource-limited systems, focusing specifically on microcontroller-based applications in an IoT environment. They developed a low-complexity network node device that encodes messages for transmission to a gateway. Experimental results showed significant improvements in memory usage and encoding time compared to direct parity check matrix representation. However, the study emphasis on resource-limited systems, such as IoT devices, this may result in potential trade-offs in encoding speed, complexity, or error-correction performance compared to more resource-rich systems.

Table 1. Related work overview

Ref. No.	LDPC Type	LDPC Encoder Algorithm Used	Power Reduction Method	Application	Technology or hardware used	Improvement Scope	Drawbacks
[13]	QC-LDPC	Richardson–Urbanke (RU) Method	Storing the quantized value of the permutation information for each submatrix.	5G-NR	TSMC 65-nm CMOS technology	A high-throughput, low-complexity, and flexible parallel encoder architecture help to reduce power usage.	The study neglected addressing other aspects such as error correction performance or system integration considerations.
[14]	Binary LDPC	Forward substitution-based encoding	Partially parallel architecture	5G-NR.	Circular shifter	High throughput, low latency, best HUE, and more energy-efficient encoder design.	The proposed architecture may introduce additional complexity to the LDPC encoder design.
[15]	QC-LDPC	High parallel LDPC encoding algorithm	parallel encoder with compatible architecture	5G-NR	65 nm CMOS technology	High performance, significant area-efficiency, flexible, fully compatible with different base graphs of 5G LDPC codes.	Limited applicability and adaptability to other coding schemes or applications outside the 5G context.
[16]	QC-LDPC	High parallelism encoding algorithms	To obtain multiple parity check bits, the QC-LDPC encoder adopted multi-channel parallel construction.	5G-NR	SIMC 28-nm CMOS technology	Higher throughput, low encoding latency, flexibility, coding efficiency, and hardware power usage.	The study overlooked other factors such as error correction performance, complexity, or system integration
[17]	QC-LDPC	Two-step encoding algorithm	VLSI encoding architecture based on XOR-gate trees.	IEEE 802.11n/ac/ax standards.	90- and 45-nm CMOS technology	High throughput.	Full verification and testing required when integrating the proposed encoder into practical systems.

[18]	LDPC-CC	LDPC-CC encoder	Fine-tuned parallelized encoder	IEEE 1901 standard.	28-nm CMOS technology	Proposed encoder can meet the throughput requirement of the standard and its power- and area-efficient.	There may be trade-offs in terms of encoding speed, latency, or error correction capabilities.
[19]	Binary LDPC	Straightforward Encoding With Generator Matrix Multiplication	The LDPC Encoder's pipelining architecture includes two-stage, three-stage, and MRP structures.	SYNOPSYS tool and XC3S-250E FPGA device.	XC3S-250E FPGA Device	Reduce overheads such as power and area by using less memory.	The study did not discuss other performance metrics beyond power, area, and memory consumption.
[20]	QC-LDPC	Richardson–Urbanke (RU)	LDPC implementation in a microcontroller with low computational resources.	IoT	STM32L476 microcontroller	Throughput increased while encoding time is reduced, lowering energy consumption and increasing error correction.	There may be potential trade-offs in encoding speed, complexity, or error-correction performance.
[21]	QC-LDPC	Preprocessing algorithm	Multiplication architecture for QC matrix and efficient encoder architecture.	Consultative Committee for Space Data Systems (CCSDS).	FPGA, Zynq UltraScale+ MPSoC hardware.	Throughput performance for the specified codes, with low resource utilization.	Preprocessing step may add complexity to the encoding process and require additional computational resources.
[22]	QC-LDPC	Hardware-shared architecture	Cost-effective early termination (ET) scheme	Multilevel cell (MLC) NAND flash memory.	TSMC 90 nm CMOS technology.	High encoding throughput, decoding energy efficiency, energy reduction and low area overhead.	Further testing and validation are required to apply the system in real world.

Additionally, the authors in [21] suggested a novel architecture for the multiplication of a dense QC matrix with a bit vector in QC-LDPC encoding. The architecture leverages parallelism in the QC structure and optimized scheduling for concurrent processing of multiple bits. The proposed architectures were implemented on various FPGA technologies. The results showed improved speedup compared to previous approaches with low resource utilization. However, for Near-Earth communications, a preprocessing algorithm was introduced, which adds complexity to the encoding process and may require additional computational resources.

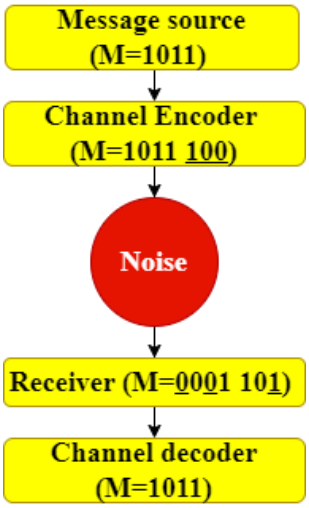

Figure. 3 Channel encoding and decoding demonstration [25]

Lastly, the authors in [22] offered an energy-efficient codec design using a rate-0.91 systematic QC-LDPC code, incorporating a cost-effective early termination scheme that achieved significant energy reduction (54.6%) with minimal area overhead compared to no early termination. The chip operated at 278 MHz and achieved the best decoding energy efficiency and high throughput. It also demonstrated a high encoding throughput of 4.4 Gbps. However, further validation in diverse scenarios, considering different channel conditions, system configurations, and variations in input data, is necessary to assess the codec's performance and robustness in real-world applications.

To facilitate a comprehensive understanding of previous works, Table 1 has been included. This table provides a detailed focus on previously mentioned encoder power reduction studies, encompassing essential details such as the LDPC type and algorithm used, the power reduction method employed, the application context, technology used, improvement scope, and any identified drawbacks for each mentioned study.

As evident from Table 1, previous studies on LDPC encoder power consumption have often suffered from issues such as complexity, flexibility overheads, high resource requirements, or treated the power consumption problem as secondary parameter. In contrast, this research takes a dedicated approach to address power consumption in LDPC encoders. This can be done using DVFS as a technique to lower power usage across different frequencies, by developing a suitable model that achieves power reductions without effecting encoder performance. This new concept has significant potential to meet the demands of next-generation digital communication and network applications in a more comprehensive manner. By solely targeting power reduction and incorporating DVFS techniques into fuzzy logic controller (FLC), this can offer large power savings without sacrificing performance, resulting in more efficient and sustainable digital communication systems.

3. Implementation of LDPC Encoder

The LDPC encoder plays a crucial role in the communication system as it functions as a channel encoder (see Fig. 3). Positioned on the transmitter side of the communication channel, its primary objective is to augment the transmitted message bits with additional parity bits. These parity bits are strategically interconnected in a random manner. This random interconnection serves a significant purpose by enabling the decoder at the receiver side to correct multiple erroneous bits in the received message, without the need for retransmission or handshaking [23]. By incorporating this random link between the parity and message bits, the LDPC encoder enhances the error correction capability of the communication system. It allows for the detection and subsequent correction of errors introduced during the transmission process. This proactive error correction mechanism improves the overall reliability and efficiency of the communication system, as it mitigates the need for resource-intensive retransmission or complex handshaking protocols [8, 24].

In this research, the Straightforward encoding method with generator matrix multiplication is employed as the encoding technique for constructing the LDPC encoder. This method is specifically chosen due to its advantages in hardware implementation. By pre-calculating the generator matrix using this method, the necessary matrix multiplication can be easily accomplished in hardware, ensuring efficient and streamlined encoding operations [14]. The process of building the LDPC encoder using the Straightforward encoding method is illustrated in Fig. 4. The flowchart provides a visual representation of the sequential steps involved in constructing the encoder to generate the encoded output based on the input data. To further illustrate the design specifications of the LDPC encoder, Table 2 is presented. This table provides detailed information on the specific requirements and characteristics of the encoder design. It encompasses parameters such as input data size, output data size, parity bit size, and H matrix size.

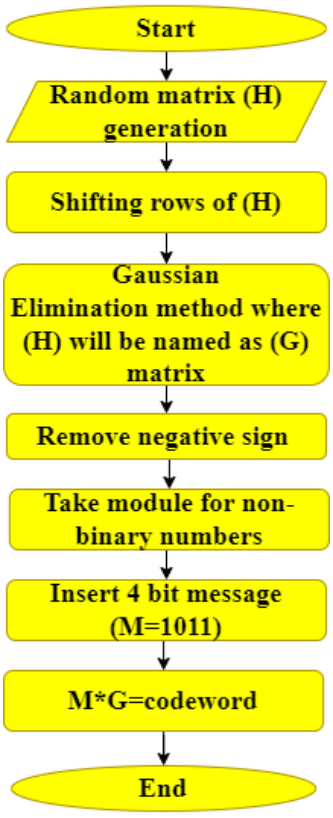

Figure. 4 LDPC encoder flowchart

Table 2. Specifications of LDPC encoder design using MATLAB M. file.

Parameter	Specification
Type of LDPC PCM matrix	Binary irregular
Algorithm/method used	Straightforward encoding with generator matrix multiplication.
Size of H matrix	4×7
Number of message bits	4 bits
Number of parity bits	3 bits
Number of code word bits	7 bits

In the construction of the logic circuit for the LDPC encoder, the multiplication operation plays a crucial role. This operation involves multiplying the message bits with the H matrix to generate the code word which consist of original message bits besides parity bits. For example:

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix} \times [1\ 0\ 1\ 1] = [messag\ bits \mid parity\ bits] \quad (1)$$

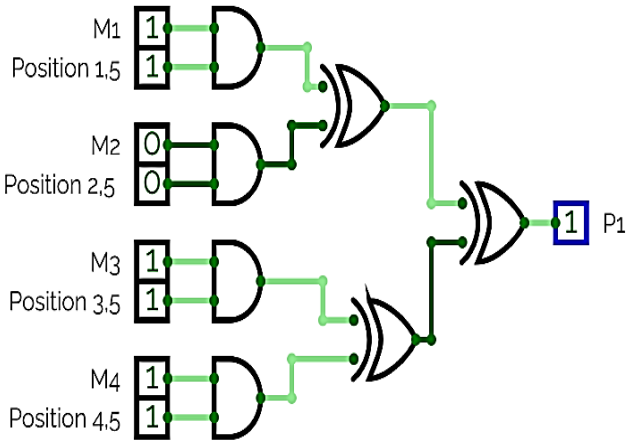

Figure. 5 Initial LDPC encoder logic circuit for the first parity bit p1. The first inputs (m1, m2, m3, m4) represent the message bits, and the second inputs (position 1,5, position 2,5, position 3,5, and position 4,5) represent the position in the G matrix

Previous research design phases have provided valuable insights into representing multiplication using logical AND gates and module-2 addition using logical XOR gates. Fig. 5 provides a visual representation of the basic encoder logic circuit, specifically highlighting the generation of the first parity bit (P1). The circuit utilizes logical AND gates to perform the necessary multiplications between the message bits and the corresponding positions in the G matrix. These AND gate outputs are then fed into logical XOR gates, which perform module-2 additions, resulting in the desired parity bit (P1). It is important to note that the same approach can be applied to design the remaining parity bits (P2, P3). However, the key difference lies in the matrix positions used for the multiplications. By adjusting the connections and calculations based on the specific matrix positions, each parity bit can be generated accurately. This contributes to the overall error correction capabilities of the encoding process, ensuring the reliable transmission of data [26].

In our previous study, the total logic circuit responsible for generating the three parity bits in the LDPC encoder was specifically designed to mimic the behaviour of digital circuits on a very large scale integration (VLSI) platform. As depicted in Fig. 5 from our previous study, the original circuit was modified to exclusively employ NAND, NOR, and NOT logic gates. This adjustment was necessary to ensure compatibility with VLSI technology [31]. Furthermore, the determination of fan-out and path values was an important aspect of evaluating the circuit's characteristics. The fan-out value was calculated by examining each gate's forks,

Table 3. Specifications of LDPC encoder logic circuit

Parameter	Specification
Total number of inputs	16
Total number of output	3 (p_1,p_2,p_3)
Total number of gates	51
Total number of paths	16 paths for each output. total=48
Maximum gate output	2
Maximum path gates	7 gates

representing the number of outputs connected to a particular gate. On the other hand, the path value was determined by assessing the number of gates leading to the main output gate. These measurements provided valuable insights into the circuit's performance and behaviour [12].

Within the circuit, there exist multiple alternative paths, each contributing to a significant amount of time delay. The path with the longest delay, known as the worst-case condition, can be identified for each parity bit. Specifically, for P1, the longest path is path16 = [gate17, gate16, gate15, gate13, gate12, gate11, gate9]. Similarly, for P2, the longest path is path16 = [gate34, gate33, gate32, gate30, gate29, gate28, gate26]. Lastly, for P3, the longest path is path16 = [gate51, gate50, gate49, gate47, gate46, gate45, gate43]. These paths have been determined based on their composition of sequential gates and are critical in understanding and analysing the time delays within the circuit. Specifications of the LDPC encoder logic circuit in [12] are shown in Table 3:

4. Implementation of the proposed power control system for the LDPC encoder based on different frequency ranges

In general, every logic gate in a circuit incurs a certain time delay. This delay becomes more significant as the frequency of the circuit increases, leading to higher voltage requirements and increased power dissipation. The total delay time of the circuit is determined by the cumulative sum of all the gate delays that the input signal passes through before reaching the output. The gate timing delay (t_d) can be defined as follows [27]:

$$t_d = \frac{C_L V_{dd}}{\mu C_{ox} \frac{w}{l} (V_{dd} - V_{th})^2} \quad (2)$$

Where C_L is the load capacitor for each gate, μ is the carrier mobility, C_{ox} is the oxide capacitance, $\frac{w}{l}$ is the transistor width to length ratio, and V_{th} is the threshold voltage. C_{ox} is given by [27]:

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad (3)$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the oxide permittivity. For silicon devices, $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})\, F/cm$.

The design parameter K_i, also known as the trans-conduction parameter, is used to characterize the behaviour of the i-channel device, where i represents either the p or n substrate. For the sake of simplicity, it is commonly referred to as the conduction parameter. In the case of an i-channel device, the conduction parameter can be expressed as follows [28]:

$$K_i = \frac{W \mu_i C_{ox}}{2L} \quad (4)$$

Eq. (4) reveals that the conduction parameter is determined by a combination of electrical and geometric factors. The oxide capacitance and carrier mobility are constants that are dependent on the fabrication technology employed. However, the geometry of the MOSFET, represented by the width-to-length ratio (w/l), can be adjusted to achieve desired current-voltage characteristics in MOSFET circuits. In addition to these parameters, the fan-out and path values play a crucial role. By measuring the time delay associated with each logic gate in the LDPC encoder circuit, it is possible to measure the overall performance. A flowchart illustrating the procedure for calculating the time delay is presented in our previous work Fig. 6 [12].

The proposed block diagram for a multi-frequency LDPC encoder with power reduction is depicted in the Fig. 6 below. This system utilizes three frequency ranges, namely low, medium, and high, which are inputted into the fuzzy logic controller during the initialization phase. The power value obtained from this process is then fed back to the fuzzy logic controller, which employs the DVFS approach. This allows the controller to select an appropriate voltage value that ensures the system operates efficiently, resulting in reduced power consumption for the overall LDPC encoder because the relationship between voltage and power is direct according to the following Eq. (5) [29]:

$$P_d = \alpha\, F\, V_{dd}^2 \sum_{i=1}^{n} C_{Li} \quad (5)$$

Where F is the circuit frequency, C_{Li} is the load capacitor of the i^{th} gate in the circuit and n is the number of gates in the circuit. This design demonstrates the flexibility of the system in accommodating different frequency ranges while achieving significant power reduction.

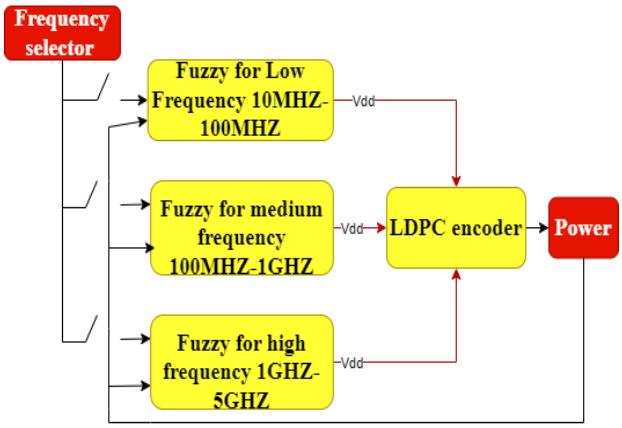

Figure. 6 Different frequency ranges for LDPC encoder power controller.

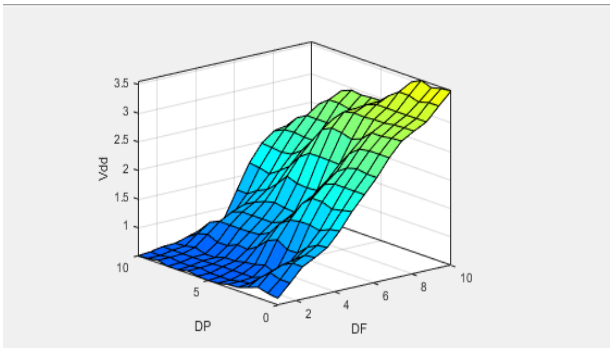

Figure. 7 Surface of fuzzy used

Table 4. Specifications of the proposed LDPC encoder power measurement system.

Parameter	Specification
Range of voltages	[0.8-3.5] Volt
Range of frequencies	[10M-5G]Hz
CMOS technology	16 nm
Technology parameters	C_L: 1.78×10^{-14} C_{OX}: 0.028 W_n: 1.76×10^{-8} L_n: 1.76×10^{-8} W_p: 1.76×10^{-8} L_p: 1.76×10^{-8} μ_p: 0.0075 μ_n: 0.028 V_{tp}: -0.6862 $V_{tn.}$: 68191
Energy initialization	0

The FLC was chosen as the controller for its simplicity and the absence of the need to create a mathematical model of the control system. In the proposed design, the FLC is responsible for controlling the voltage. It takes two inputs, namely frequency and power, and produces a single output, V_{dd}, as shown in Fig. 6. By using these parameters, multiple rules can be derived to construct the surface illustrated in Fig. 7.

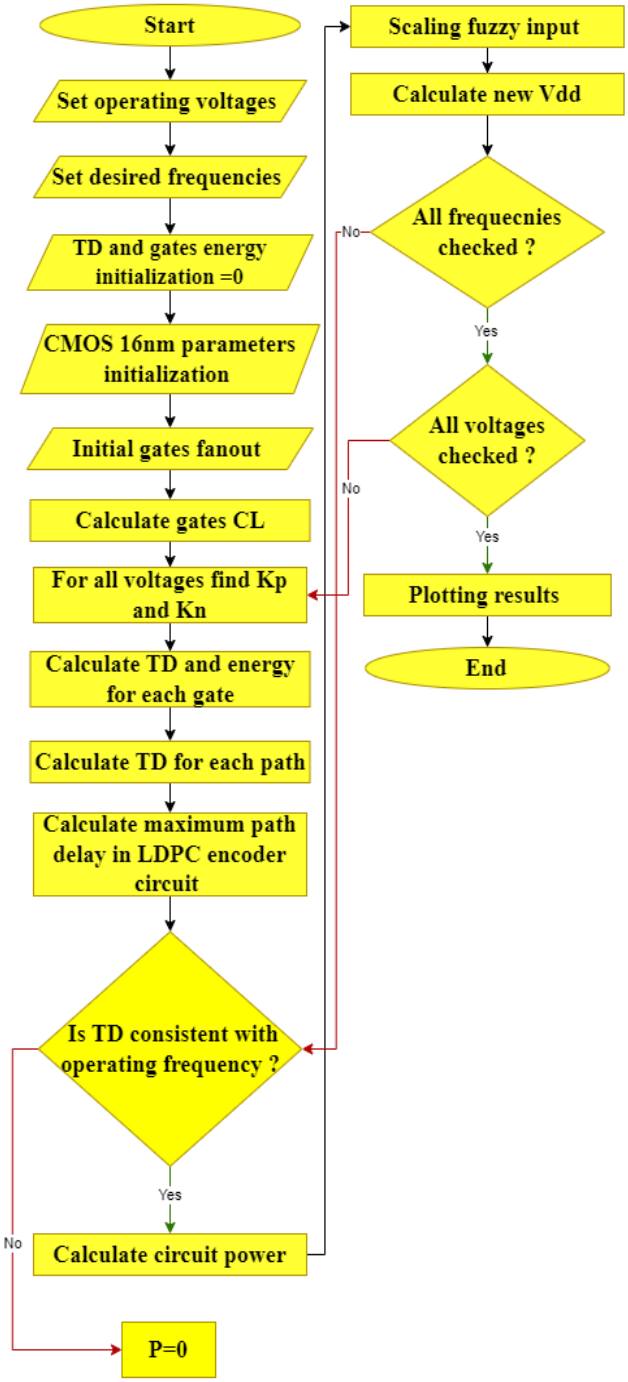

Figure. 8 Flowchart of power reduction for LDPC encoder program.

The system design steps are outlined in Fig. 8, providing a comprehensive overview of the design process.

The used power control and power measurement system parameters are listed in Table 4 below.

5. Result and discussion

The MATLAB M-file was employed to execute all the design steps mentioned earlier. The outcomes

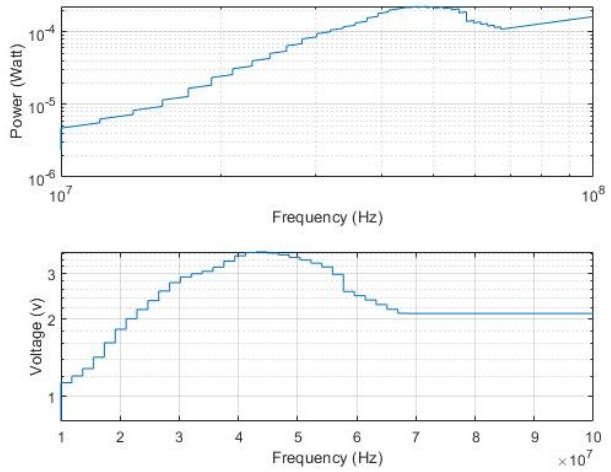

Figure. 9 Relationship between power vs frequency and voltage vs frequency with low range

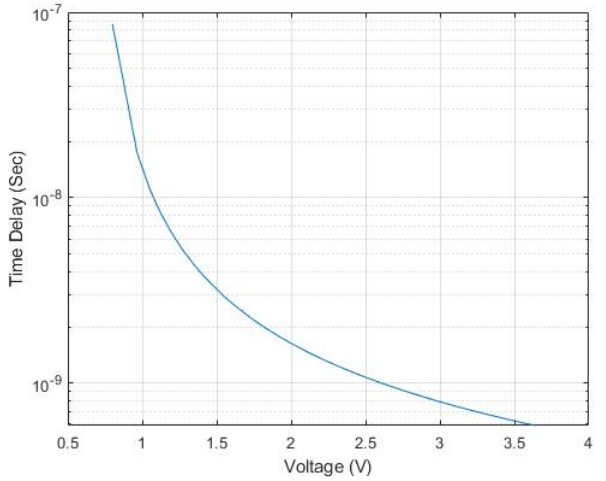

Figure. 10 Relationship between time delay vs voltage in low frequency range

of the system, depicted in Figs. 8, 9, utilizing the low frequency range and an initial voltage of 0.8V, are presented below:

Fig. 9 illustrates a direct relationship between voltage and frequency within the low range of 1MHz to 100MHz. As the frequency increases, the voltage also increases, leading to higher power consumption over time. This relationship is depicted by Eq. (5), which demonstrates the impact of frequency on voltage and power consumption. On the other hand, Fig. 10 demonstrates an indirect relationship between voltage and time delay. As the frequency increases, the delay decreases, resulting in a higher voltage requirement to sustain the desired performance. This relationship aligns with the previously mentioned Eq. (2), highlighting the influence of frequency on voltage and power consumption.

In the medium frequency range of 100MHz to 1GHz, the system exhibits excellent performance and

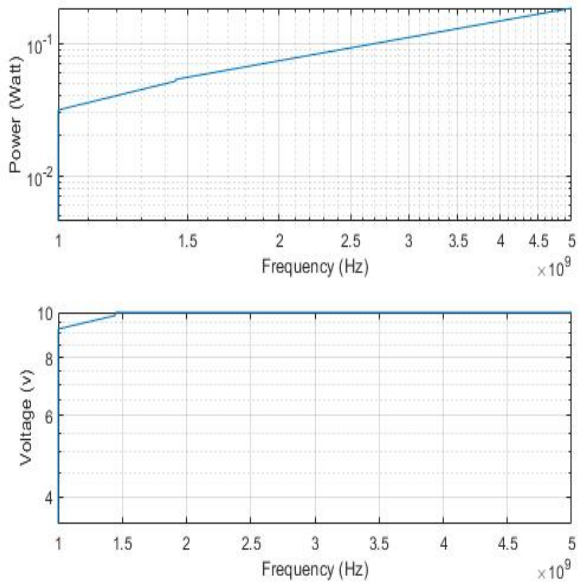

Figure. 11 The relationship between power vs frequency and voltage vs frequency with high range

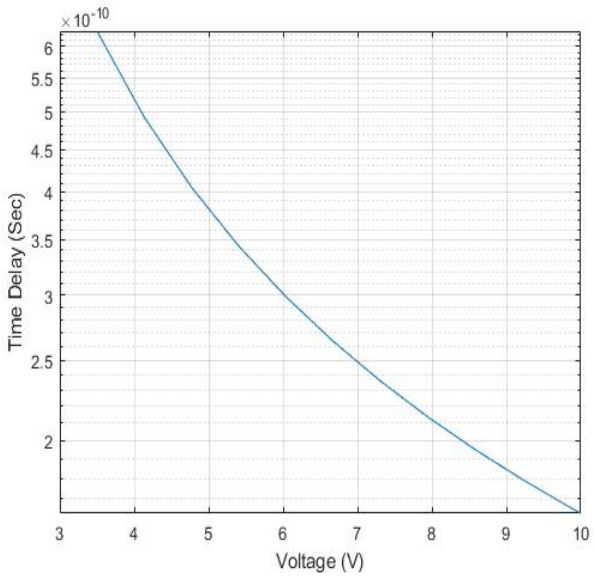

Figure. 12 Relationship between time delay vs voltage in high frequency range

effectively controls the overall power consumption by regulating the voltage input through the fuzzy logic controller and DVFS method. As demonstrated in the previous work, Fig. 12 and 13 specifically, the system operates with an initial voltage of 0.9V. With the aid of the fuzzy logic controller and DVFS method, the system achieves optimal power management by dynamically adjusting the voltage based on the frequency requirements. This capability ensures efficient operation and power reduction throughout the medium frequency range, contributing to enhanced performance and energy efficiency [12].

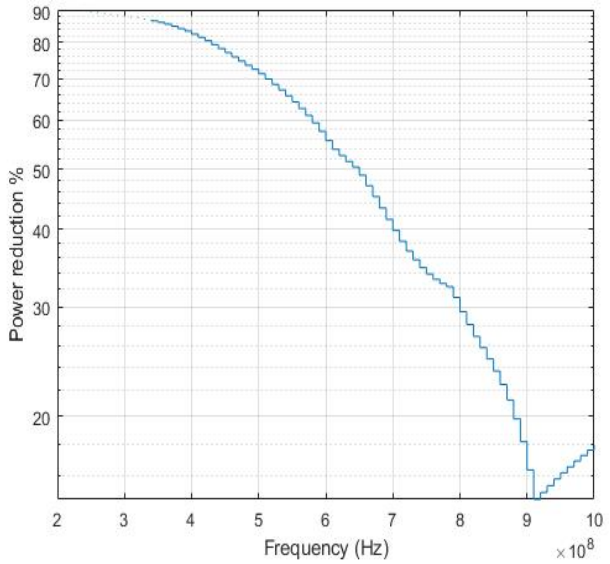

Figure. 13 Effect of the controller on the purposed system

The following results illustrate the system's response to the high frequency range when initialized with a voltage of 3.5V:

As shown in Fig. 11, the relationship between voltage and frequency remains consistent and direct across all three frequency ranges. As the frequency increases, the voltage also increases accordingly as described by Eq. (5). However, in the high frequency range from 1G to 5G, the voltage reaches a critical point of 10V. This voltage level is impractical for real-world systems due to limitations and constraints. Fig. 12 illustrates the significant reduction in time delay as the frequency increases. This reduction in time delay necessitates higher voltage levels to maintain system performance, as indicated by Eq. (2) and (5). However, the corresponding increase in voltage leads to higher power dissipation.

Fig. 13 demonstrates the significance and impact of the controller on the proposed system across the three frequency ranges, as well as the percentage of power reduction achieved. The controller, which incorporates the fuzzy logic controller and DVFS method, plays a crucial role in regulating the voltage and controlling power consumption in the LDPC encoder:

The graph presented in Fig. 13 provides a comparative analysis of the power reduction percentage achieved by the system across different frequency ranges, highlighting the impact of the controller's presence on power consumption. The results demonstrate a clear correlation between frequency and energy consumption, with higher frequencies leading to increased energy usage. Notably, significant power reduction values are observed in the low and medium frequency ranges, with approximately 90% reduction in the low frequency range and around 60% reduction in the medium frequency range. The implementation of the controller plays a crucial role in effectively managing and reducing power consumption. For instance, at a frequency of 90 MHz, the controller achieves a power reduction of 14.5%, representing the lowest achievable limit for the system.

These findings emphasize the importance of integrating the controller into the system design to achieve efficient power management. By leveraging the capabilities of the controller, LDPC encoders can substantially decrease overall power consumption across various frequency ranges, ultimately leading to enhanced energy efficiency in their operation.

Furthermore, a comprehensive comparison is conducted between the proposed work and related works, which are outlined in Table 1. The objective is to highlight the distinctions and advancements achieved in terms of power consumption. Table 5 is specifically designed to present these differences and improvements, providing a clear overview of the findings.

6. Comparative analysis

CMOS technology based:

In this study, we utilized 16-nm CMOS technology, which is known to offer lower power consumption compared to larger technology nodes. Generally, as the technology node decreases, power consumption tends to decrease as well. The power reduction achieved can vary, ranging from approximately 30% to 50% or even more, depending on the specific circuit and implementation [26]. Based on this, the proposed power controller in our study demonstrates an advantage in terms of power consumption compared to previous studies that utilized different technology nodes. For instance, studies using 65-nm [13, 15], 28-nm [16, 18], or even 90- and 45-nm CMOS technology [17, 22] may experience higher power consumption compared to our proposed approach. By leveraging the benefits of 16-nm CMOS technology, our power controller contributes to reducing overall power consumption, making it a promising solution for efficient power management in LDPC encoders.

Error correction performance based:

This study successfully maintains the error correction performance of the LDPC encoder despite implementing the fuzzy logic and DVFS approach in its logic circuit. As a result, it outperforms other approaches used in previous studies such as [13, 16],

and [20]. It also offers advantages over other studies that involve trade-offs, such as [18] or [19]. By effectively integrating the fuzzy logic and DVFS techniques, the proposed method achieves optimal error correction performance while simultaneously reducing power consumption. This highlights the superiority of our approach in maintaining high-quality LDPC encoding without compromising on power efficiency.

System integration based:

The proposed system exhibits remarkable flexibility in operating across various frequency ranges, as shown in Fig. 5. In contrast to the limited applicability mentioned in [15], our system is capable of seamlessly adapting to different standards with minimal verification required. Therefore, this stands in contrast to previous studies such as [17] and [22], which faced limitations in terms of applicability and required extensive verification processes. The flexibility of our system allows for its efficient deployment in diverse scenarios, accommodating a wide range of frequency requirements and standards. This characteristic enhances its practicality and usability in real-world applications without compromising on performance or necessitating extensive verification procedures.

Complexity based:

Our proposed power manager surpasses the performance of the RU algorithm utilized in [13] and [20]. It achieves this by eliminating the need for encoding additional code bits, resulting in significant reductions in resource and power wastage, while maintaining encoder speed. Additionally, we have successfully managed LDPC performance by reducing complexity and addressing concerns related to coding delays as highlighted in [14]. Moreover, we have eliminated the high parallel design employed in [16] and the pre-processing steps that consume system resources mentioned in [21]. Furthermore, unlike the pipeline usage mentioned in [19], which can suffer from complexity overheads and require modifications for larger matrix dimensions, our algorithm is adaptable and compatible with large matrix dimensions and different frequency ranges. These improvements collectively contribute to the overall efficiency and effectiveness of our power manager, making it a compelling alternative when compared to the methodologies discussed in the referenced studies.

7. Conclusion

This study emphasizes the significant role of LDPC in communication systems as a channel encoder and decoder, particularly focusing on the importance of power management in multi-frequencies. It recognizes the necessity for circuits to address power consumption and frequency-related challenges, which is particularly relevant for handheld devices aiming for extended battery life and high-end circuits aiming to mitigate complex cooling arrangements and reliability issues. The study provides a comprehensive overview of LDPC in communication systems and briefly discusses the challenges encountered in previous research. It then delves into the logic circuit design for the LDPC encoder, introduces a power control method, and highlights the enhancements compared to previous studies.

The results clearly demonstrate the effectiveness of combining LDPC, one of the most efficient forward error correction methods, with the power control technique of DVFS. The proposed system not only achieves substantial power savings but also provides notable flexibility in frequency management. By utilizing a fuzzy logic controller to regulate the voltage level entering the system, the proposed system achieves an impressive 90% reduction in power consumption in the low and medium frequency ranges, as well as a 20%-14.5% reduction in the high frequency range. Importantly, these power savings are achieved without compromising error correction performance, throughput, complexity, and time delay, setting the proposed system apart from previous studies.

Overall, this study highlights the significant importance of LDPC in communication systems and presents a comprehensive approach to power management. The proposed system delivers significant power savings, enhances the freedom in frequency management, and improves the overall efficiency of the system. It represents a notable advancement in the field, offering a promising solution for efficient power management in communication systems.

Conflicts of interest

The authors declare no conflicts of interest. We confirm that there are no personal or financial circumstances that could be perceived as influencing the representation or interpretation of the reported research results.

This manuscript is the original work of the authors, and no external parties or organizations have influenced the content or findings presented in this

paper. We have complied with the guidelines and requirements of the journal regarding conflicts of interest and have provided this statement to ensure transparency and maintain the integrity of our research.

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Qusay Al-Doori: Conceptualization, Methodology, Validation, Writing—review and editing, Supervision.

Omar Alani: Conceptualization, Methodology, Writing—review and editing, Supervision, Project administration.

All authors have made substantial contributions to the research reported in this manuscript. They have collectively contributed to the conceptualization and methodology of the study. Noora Nazar has played a key role in data collection, analysis, and the initial draft preparation of the manuscript. All authors have actively participated in the review and editing process, ensuring the accuracy and quality of the content. Noora Nazar has taken the lead in the writing of the manuscript, with the guidance and supervision of Qusay Al-Doori and Omar Alani.

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