Received: June 2, 2020. Revised: August 25, 2020.

International Journal of
Intelligent Engineering & Systems

http://www.inass.org/

Carrier-based PWM Method for Indirect Matrix Converters based on Space Vector Analysis

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Abstract: In this paper, a novel approach to realize the carrier-based pulse width modulation (CBPWM) method for indirect matrix converter (IMC) is presented. The advantage of the proposed CBPWM method is that only one triangular carrier signal with constant gradient falling and rising edges is used to generate the PWM to the power switches in both the rectifier and the inverter stages of IMC. The analysis of the proposed CBPWM method is based on the space vector approach and the relationship between CBPWM and space vector pulse width modulation (SVPWM) methods is provided. In this paper, four CBPWM methods called: sinusoidal PWM, third harmonic injection PWM, symmetrical PWM and discontinuous PWM are presented. These different CBPWM schemes are established according to the distribution of zero vectors and the switching pattern of the SVPWM method. The comparison of output voltage performance with different CBPWM schemes are investigated. Compared to the conventional method the calculation time of the proposed method is reduced around 50%. Concretely, the calculation time of the SVPWM method is 45 μs, while the calculation time of the proposed method is 22 μs. The experiments have been carried out to show the effectiveness of the proposed method.

Keywords: Direct matrix converter, Indirect matrix converter, Space vector modulation, Carrier-based PWM modulation, DSP.

1. Introduction

The matrix converter (MC) provides many advantages: sinusoidal input and output currents, simple and compact power circuit due to the lack of electrolytic capacitors, bidirectional power flow, and controllable input power factor [1]. Recently, it has been proposed in many different application, i.e. motor drives, wind-energy conversion systems, electric aircraft systems, variable-speed diesel-generation systems [2-5].

The MC can be divided into two kinds such as direct matrix converter (DMC) and indirect matrix converter (IMC) [6]. The DMC consists of nine bidirectional switches, which are used to connect any output phase to any input phase as shown in Fig. 1.

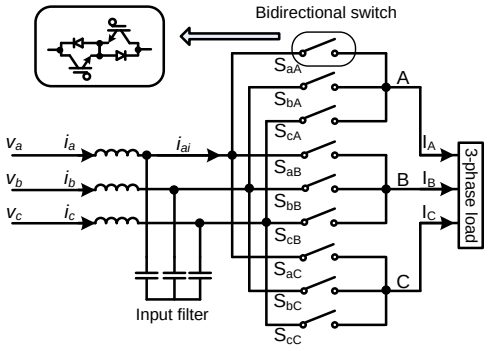

Figure. 1 DMC topology

The IMC comprises of a separated four-quadrant current source rectifier and a conventional two-level voltage source inverter, which is shown in Fig. 2. The IMC has received more attention because it has some advantages as compared to the DMC such as:

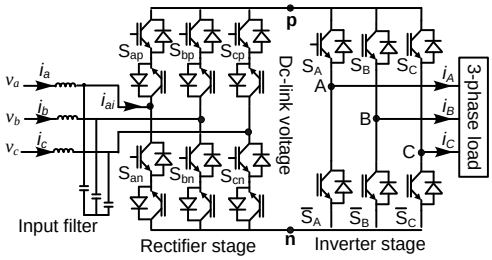

Figure. 2 IMC topology

- Simple commutation [7].
- The possibility of reducing the number of power switches [8].
- The possibility of constructing an ac-ac converter to supply multi-phase load from three-phase power supply [9]-[11].
- The possibility of supply electrical energy to an unbalanced or non-linear three-phase load by adding one more leg into the inverter stage [12].
- The possibility of improving the voltage transfer ratio by inserting the Z-source network between the rectifier and the inverter stages [13-14].

In order to produce high quality output voltage with the specific IMC topologies proposed in [8-14], the PWM strategies have received much attention recently. The PWM strategies for IMC can be divided into two groups: SVPWM and CBPWM methods. The SVPWM approach has some disadvantages. It needs complex calculations and tables to synthesize the reference input current and the reference output voltage. The implementation of SVPWM method needs to do some steps [7, 8, 15-17]: The adjacent active and zeros vectors are needed to synthesize the reference input current and reference output voltage vectors. Then, the duty cycles of these active and zero vectors are calculated and the switching patterns are arranged according to the input current and voltage vectors. In order to remove the disadvantages of the SVPWM, the CBPWM method is adopted by researchers in recent years [18, 19]. However, the carrier signal used for the rectifier stage is different from that of the inverter stage: The carrier signal used for the rectifier stage is a symmetrical triangular signal, while an unsymmetrical triangular signal with different slope in the rising and falling edge is used for the inverter stage. Moreover these rising and falling slopes are changed in every sampling period due to the variation of the dc-link voltage. And also, the type of offset voltage and its effects on the input/output performance of IMC are not explored.

For the conventional two-level voltage source inverter (VSI), which is supplied by the fixed dc-source, the complete correlation between SVPWM and the carrier-based PWM (CBPWM) has been deduced in [20]. However, in the IMC topology, the dc-link voltage generated by the rectifier stage is not constant. The average value of the dc-link voltage vacillates with the frequency of six times of input voltage frequency.

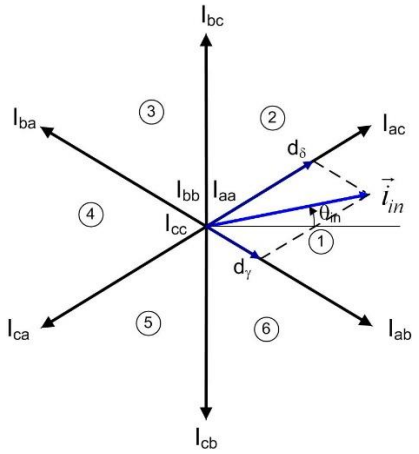

Figure. 3 Space vector diagram of the rectifier stage

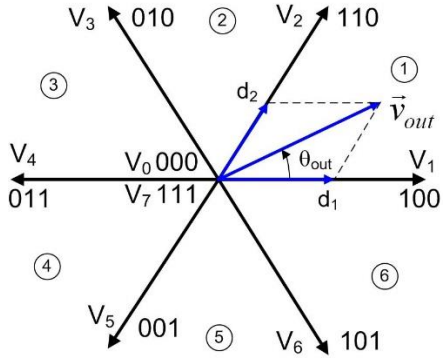

Figure. 4 Space vector diagram of the inverter stage

In this paper, a simple approach to realize the CBPWM method for IMC is investigated based on space vector analysis, which uses only one symmetrical triangular carrier signal to generate PWM signals for all switches of both the rectifier and the inverter stages, which we have already introduced succinctly in [22]. The several possibilities by adding an offset voltage to the reference output voltages in the CBPWM method are discussed according to the particular disposition and distribution of zero vectors in the SVPWM method. Three continuous CBPWM and two discontinuous CBPWM methods are presented in this paper. The effects of the offset voltage on the converter output performance are quantified.

This paper also describes the realization of proposed CBPWM method based on the cooperation of digital signal processing (DSP) TMS320F28335 and complex programmable logic device (CPLD) Alera-EPM7128. Herein, 3-bit encoded data and 10

PWMs, which are the output signals of DSP, are transmitted to the CPLD. The function of CPLD is to generate 12 gating pulses for 6 bidirectional switches in the rectifier stage and 6 unidirectional switches in the inverter stage. It is shown that the proposed CBPWM could easily be implemented due to only one up/down counter in DSP is used. Compared with the SVPWM method, the proposed method is much simpler, and the calculation time reduction is obtained. The sinusoidal waveforms of the input current/output voltage of the IMC are obtained with the proposed method.

This paper is organized as follows: the paper firstly reviews the operational principles and the space vector analysis of the IMC in Section II. Section III describes the proposed CBPWM and the relationship between CBPWM and SVPWM methods. The results of performance analysis in term of output voltage distortion with different CBPWM schemes are provided in section IV. The prototype experiments and experimental results are shown in section V to verify the validity of the proposed method. Finally, Section VI offers some conclusions.

2. Space vector modulated indirect matrix converter

2.1 Operation principle

As shown in Fig. 2, IMC topology consists of a rectifier stage at ac source side and an inverter stage at the load side. The rectifier stage is similar to the traditional one except that all the six switches are bidirectional switches. The purpose of the rectifier stage is to maintain sinusoidal input currents as well as to supply the positive dc-link voltage. In the inverter stage, the arrangement of switches as the same structure as the conventional two-level VSI. The output voltage with variable frequency and amplitude can be synthesized by controlling the inverter stage. The SVM for the IMC, was introduced in [7, 15, 17], is based on the space vectors analysis of input current and output voltage under the constraint of unity input power factor. The SVM produces a combination of vectors to synthesize the input current and output voltage vectors in the rectifier and inverter stages, respectively. Once the vectors and their duty cycles are determined, the switching pattern of the converter is obtained by combining the switching states from two stages in order to keep balanced input and output currents.

2.2 Space vector modulation

It is assumed that balanced three-phase supply voltages are given as:

$$\begin{aligned} v_a &= V_{in}\cos(\omega_{in}t) \\ v_b &= V_{in}\cos\left(\omega_{in}t - 2\frac{\pi}{3}\right) \\ v_c &= V_{in}\cos\left(\omega_{in}t - 4\frac{\pi}{3}\right) \end{aligned} \quad (1)$$

where V_{in} is the input voltage magnitude and ω_{in} is the input angular frequency.

To explain the SVM method for rectifier stage control, it is convenient to define the input current and output voltage space vectors as follow:

$$\vec{i}_{in} = \frac{2}{3}\left(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}}\right) = I_{in}e^{j\theta_{in}} \quad (2)$$

$$\vec{v}_{out} = \frac{2}{3}\left(v_A + v_B e^{j\frac{2\pi}{3}} + v_C e^{j\frac{4\pi}{3}}\right) = V_{out}e^{j\theta_{out}} \quad (3)$$

The space vector of the rectifier stage is composed of six active current vectors with fixed directions and three zero vectors as shown in Fig. 3. Each vector represents the connection of the input voltage to the dc-link bus. For example, the active current vector I_{ab} represent the connection of input phase "*a*" to the positive pole and input phase "*b*" to the negative pole of the dc-link bus, respectively. The zero vectors I_{aa}, I_{bb}, I_{cc} represent that there is no connection between the input voltage and the dc-link bus.

The SVM for the inverter stage is based on the representation of the three phase quantities as vectors in a two dimensional plane. The SVM comprises eight space vectors *V0~V7*, where *V1~V6* are active vectors and *V0*, *V7* are zero vectors as shown in Fig. 4. Each space vector refers to the connection of the output phase voltage to the dc-link. For example, the space vector V_1(100) represents the connection of the output phase *"A"* to the positive pole and *"B"*, *"C"* to the negative pole of dc-link bus, respectively.

For the sake of explaining the SVM method, we assume that both the reference input current and reference output voltage vectors are located in sector 1 without missing the generality of the analysis ($-\pi/6 \le \theta_{in} \le \pi/6$ and $0 \le \theta_{out} \le \pi/3$).

As illustrated in Fig. 3, the reference input current $\vec{i}_{in}$ can be derived from the combination of two active vectors I_{ac} and I_{ab}. The duty cycles d_δ, d_γ of two active vectors I_{ac}, I_{ab} are given by:

$$d_\delta = m_{rec}\sin\left(\theta_{in} + \frac{\pi}{6}\right) \quad (4)$$

$$d_\gamma = m_{rec}\sin\left(\frac{\pi}{6} - \theta_{in}\right) \quad (5)$$

where m_{rec} is the rectifier stage modulation index and θ_{in} is the angle of the reference input current vector $\vec{\imath}_{in}$.

In the modulation of the rectifier stage, the zero vectors are not considered in order to obtain the maximum dc-link voltage. Hence, the duty cycles of two active vectors I_{ab}, I_{ac} in Eqs. (4) and (5) are recalculated as follows:

$$d_x = \frac{d_\delta}{d_\gamma + d_\delta} = -\frac{v_c}{v_a} \quad (6)$$

$$d_y = \frac{d_\gamma}{d_\gamma + d_\delta} = -\frac{v_b}{v_a} \quad (7)$$

The average value of dc-link voltage in the sector 1 is:

$$V_{dc} = d_x(v_a - v_c) + d_y(v_a - v_b) = \frac{3}{2}\frac{V_{in}^2}{v_a} \quad (8)$$

By similar approach, the duty cycles of modulated switches, the instantaneous and average values of dc-link voltage are obtained in Table 1 (Appendix) according to the input current sector. The minimum and maximum values of the average dc-link voltage are:

$$V_{dc(min)} = \frac{3}{2}V_{in} \quad (9)$$

$$V_{dc(max)} = \sqrt{3}V_{in} \quad (10)$$

In the inverter stage, two active voltage vectors V_1, V_2 are used to synthesize the reference output voltage vector $\vec{v}_{out}$. The duty cycles of two active vectors are given by:

$$d_1 = \frac{\sqrt{3}}{2} m_{inv} \sin\left(\frac{\pi}{3} - \theta_{out}\right) \quad (11)$$

$$d_2 = \frac{\sqrt{3}}{2} m_{inv} \sin(\theta_{out}) \quad (12)$$

Two zero vectors V_0, V_7 are applied to complete the control sampling period, and the duty cycles for each zero vector are:

$$d_7 = k(1 - d_1 - d_2) \quad (13)$$

$$d_0 = (1 - k)(1 - d_1 - d_2) \quad (14)$$

where m_{inv} is the inverter stage modulation index; θ_{out} is the angle of the reference input current vector $\vec{v}_{out}$; d_1, d_2, d_0, and d_7 are the duty cycles of voltage space vectors V_1, V_2, V_0, and V_7, respectively; k is the distribution factor of two zero vector V_7 and V_0 ($0 \le k \le 1$).

The inverter stage modulation index is expressed by

$$m_{inv} = \frac{2V_{out}}{V_{dc}} \quad (15)$$

The voltage transfer ratio of IMC is defined as follows:

$$m = \frac{V_{out}}{V_{in}} \quad (16)$$

According to (8) - (16), the voltage transfer ratio m cannot be higher than 0.866 because all duty cycles should be positive.

To obtain the balanced output voltages in the same sampling period, the switching pattern of the IMC should produce all combination of the rectifier and the inverter switching states. There are two switching states in the rectifier stage. Hence, the switching states in inverter stage should be divided into two groups. The duty cycle of active vectors and zero vectors of the output voltage space vectors in each group are calculated as follows:

During the first switching state I_{ab} is applied in the rectifier stage, the duty cycles of the V_1, V_2, V_0, and V_7 are determined as shown in (17).

$$d_{1x} = d_1 d_x; d_{2x} = d_2 d_x; d_{0x} = d_0 d_x; d_{7x} = d_7 d_x \quad (17)$$

During the first switching state I_{ac} is applied in the rectifier stage, the duty cycles of the V_1, V_2, V_0, and V_7 are determined as shown in (18).

$$d_{1y} = d_1 d_y; d_{2y} = d_2 d_y; d_{0y} = d_0 d_y; d_{7y} = d_7 d_y \quad (18)$$

2.3 Switching sequence

In order to simplify the current commutation, the zero dc-link current commutation is applied to control the rectifier stage of the IMC. The inverter stage should operate in the zero vectors when the switches in the rectifier stage are commutating. Therefore, all of currents in the rectifier stage are zero during the commutation time. The switching sequence of the IMC is arranged as shown in Fig. 5 in case that both the rectifier stage and inverter stage are operated in sector 1. It can be seen that the state transitions of two switches S_{bn} and S_{cn} in the rectifier stage occur during the time when the zero vector V_0 is applied in the inverter stage.

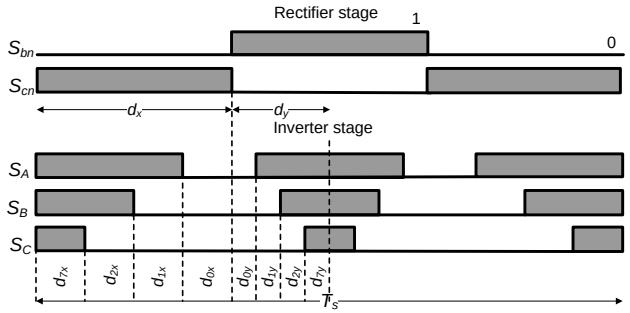

Figure. 5 Switching sequence of the IMC

3. Proposed CBPWM methods

3.1 The proposed CBPWM method

As presented in Section 2, From the above analysis, the implementation of the conventional PWM strategy for the IMC is complex. First, the selection of the effective vectors in the two stages is implemented independently, and the duty ratios of the effective vectors in the rectifier and inverter stage are determined by calculating some equations. Then, the switching states of the rectifier and the inverter stage are coordinated in order to achieve balanced output voltages and zero current commutation at the rectifier stage. In order to overcome this problem, the gating signals in the proposed method are easily made by the CBPWM method.

In the CBPWM method, the PWM signals are generated by intersection between the modulation signals and the carrier signal. In order to find the relationship between the SVPWM and CBPWM, it had to find a set of modulation signals which are compared with the carrier signal to generate PWM signals same as the SVPWM method.

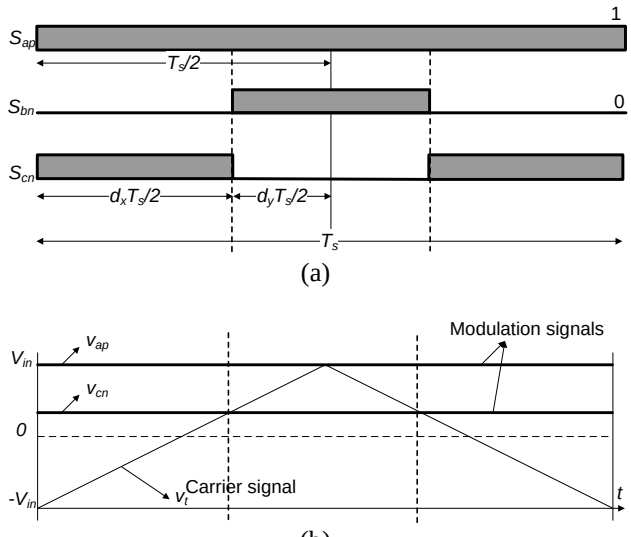

Figure. 6: (a) Switching sequence of the active switches in the rectifier stage and (b) the generated PWM signals in the rectifier stage by using CBPWM method

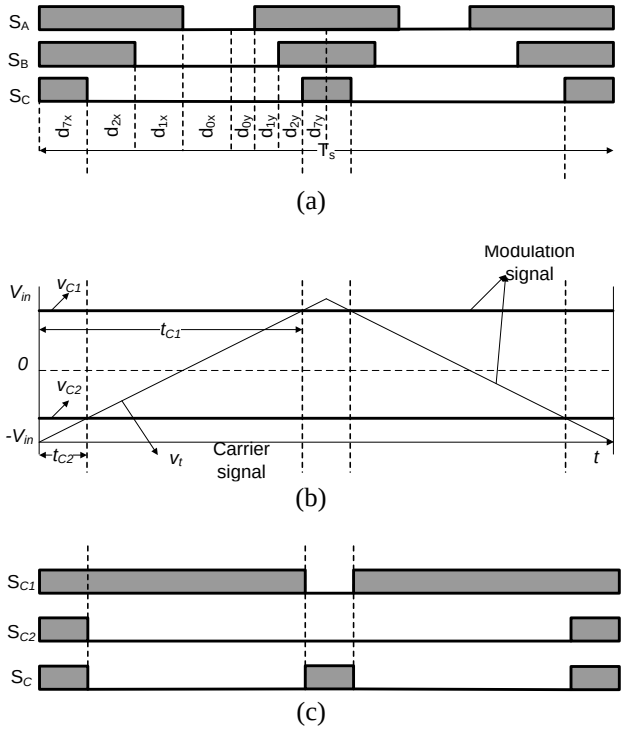

Figure. 7: (a) Switching sequence of the inverter stage by SVPWM method, (b) the modulation and carrier signals in CBPWM method, and (c) principle to generate the gating pulse for switch S_C

Fig. 6 explains the switching sequence and timing of the rectifier stage when the reference input current vector is located in sector 1 as shown in Fig. 3. In Fig 6 (a), the upper switch of phase "a", S_{ap}, is always on state, while two lower switches of two input phases "*b"* and *"c"*, S_{bn} and S_{cn}, are modulated. In half of one sampling period, the application time of the switch S_{ap} is $T_s/2$ and the application time of the two switches S_{cn}, S_{bn} are $T_{cn}/2$, $T_{bn}/2$, respectively. Fig. 6 (b) shows the intersection of the modulation signals and the carrier signal: The symmetrical triangular carrier signal is described by

$$v_t = \left(\frac{4}{T_s}t - 1\right)V_{in} \tag{19}$$

where v_t is the instantaneous value of the carrier signal, and T_s is the control sampling period.
Therefore, the two modulation signals, v_{ap} and v_{cn}, which are used to generate the gate signals for two switches S_{ap} and S_{cn}, are given as follows:

$$v_{ap} = V_{in} \tag{20}$$

$$v_{cn} = (2d_x - 1)V_{in} \tag{21}$$

The gating pulse for the switch S_{bn} is complementary to that of switch S_{cn} while all remaining switches (S_{an}, S_{bp}, S_{cp}) are off state.

Fig. 7 illustrates the switching sequence of the inverter stage when the reference output voltage vector is located in sector 1. In one control sampling period, the dc-link voltage has two values. For example, when the reference input current vector is located in sector 1, the dc-link voltage is modulated between v_{ac} and v_{ab}. Therefore, the switching sequence is separated two groups with different duty cycle. From Fig. 6 (a) and Fig. 7 (a), we can see that the inverter switching frequency is twice of rectifier switching frequency. Therefore, to generate the gate signal for each switch in the inverter stage, two modulation signals are needed. Fig. 7 (b) shows the waveforms of two modulation signals, v_{C1} and v_{C2}, and the carrier signal to produce the gate signal for upper switch S_C. The pulse S_{C1} and S_{C2} are obtained from the comparison of two modulation signals v_{C1}, v_{C2} with the symmetrical triangular signal v_t. In order to have the same switching sequence as SVPWM shown in Fig. 7 (a), the gate signal for the switch S_C can be obtained by using XNOR function as shown in Fig. 7 (c).

$$S_C = S_{C1} \bullet S_{C2} + \bar{S}_{C1} \bullet \bar{S}_{C2} \tag{22}$$

From Fig. 7(a) and (b), the turn-on time of two pulses S_{C1} and S_{C2} are obtained as follows:

$$t_{C1} = \left(1 - d_{7y}\right)\frac{T_S}{2} \tag{23}$$

$$t_{C2} = d_{7x}\frac{T_S}{2} \tag{24}$$

Substituting (21) and (22) into (17) for variable t yield:

$$v_{C1} = V_{in}\left(-2d_y\frac{v_C + v_{offset}}{V_{dc}} + d_x\right) \tag{25}$$

$$v_{C2} = V_{in}\left(2d_x\frac{v_C + v_{offset}}{V_{dc}} - d_y\right) \tag{26}$$

By similar calculation, two modulation signals v_{A1}, v_{A2} used to generate the gate signal for the switch S_A and two one v_{B1}, v_{B2} used to generate the gate signals for the switch S_B are given as follows

$$v_{A1} = V_{in}\left(-2d_y\frac{v_A + v_{offset}}{V_{dc}} + d_x\right) \tag{27}$$

$$v_{A2} = V_{in}\left(2d_x\frac{v_A + v_{offset}}{V_{dc}} - d_y\right) \tag{28}$$

$$v_{B1} = V_{in}\left(-2d_y\frac{v_B + v_{offset}}{V_{dc}} + d_x\right) \tag{29}$$

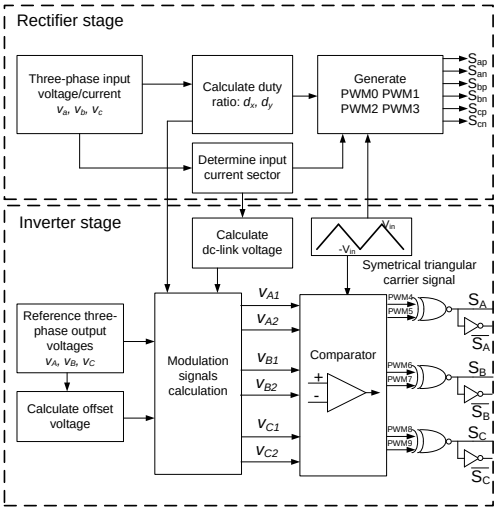

Figure. 8 The block diagram of the CBPWM method

$$v_{B2} = V_{in}\left(2d_x\frac{v_B + v_{offset}}{V_{dc}} - d_y\right) \tag{30}$$

where the offset voltage v_{offset} is determined in (31) and v_A, v_B, v_C are three reference output voltages.

$$v_{offset} = -\left[(1-2k)\frac{V_{dc}}{2} + kv_A + (1-k)v_C\right] \tag{31}$$

Eqs. (25)–(30) are obtained when the reference output voltage vector is located in sector 1. Generally, when the offset voltage is chosen as (32), these equations are valid in case that the reference output voltage vector is located in other sector.

$$v_{offset} = -\left[(1-2k)\frac{V_{dc}}{2} + kv_{max} + (1-k)_{min}\right] \tag{32}$$

where v_{max}, v_{min} are the maximum and minimum value of three reference output voltages.

$$v_{max} = max(v_A, v_B, v_C) \tag{33}$$

$$v_{max} = min(v_A, v_B, v_C) \tag{34}$$

Fig. 8 shows a block diagram of the CBPWM for the IMC. It can be seen that the implementation of generation of gating pulse in the rectifier and the inverter stages are independent. All required functions are easily implemented without complex calculations, and there is no need to coordinate the switching state of the rectifier and the inverter stages.

3.2 Relationship between SVPWM and CBPWM

Eqs. (11)-(18) and (25)-(30) represent the relationship between the SVPWM and CBPWM

methods. In the SVPWM method, the duty ratio of effective vectors which are used to synthesis the reference vectors are calculated based on the position of reference vectors and different distributions of two zero vectors V_0 and V_7 lead to different SVPWM schemes. By choosing suitable offset voltage, the CBPWM can be matched with the SVPWM method. Distribution of two zero vectors can be determined by using (32) for arbitrary offset voltage. There are typical four kinds of offset voltage, which are described as follows:

1) Sinusoidal PWM

v_{offset}=0 leads the sinusoidal carrier-signal PWM (SPWM). According to the (31), its equivalent distribution of two zero vectors is

$$d_0 = \frac{1}{2}(1 - m_{inv}\cos\theta_{out}) \tag{35}$$

$$d_7 = 1 - d_0 - d_7 \tag{36}$$

Considering the fact that $d_0 \geq 0$, the maximum modulation index in the inverter stage is inferred to be 1. Therefore, from (9), (15) and (16), the maximum voltage transfer ratio of the IMC with the SVM method is 0.75.

2) Third harmonic injection PWM (3rdHPWM)

This is the results of $v_{offset} = -\frac{m_{inv}}{6}\frac{V_{dc}}{2}cos(3\theta_{out})$ leads to third harmonics injection PWM (3rdHPWM). The equivalent distribution of two zero vectors is obtained using (31) as

$$d_0 = \frac{1}{2}\left(1 - m_{inv}\cos\theta_{out} - \frac{1}{6}cos(3\theta_{out})\right) \tag{37}$$

$$d_7 = 1 - d_0 - d_7 \tag{38}$$

Due to the positive of duty cycles of zero vectors, (37) determines the maximum modulation index in the inverter stage to be $\frac{2}{\sqrt{3}}$. Therefore, the maximum voltage transfer ratio of the IMC with the 3rdHPWM is 0.866.

3) Symmetrical PWM (SYPWM)

The distribution is equal for two zero vectors, $k=0.5$. Therefore, the result of offset voltage is $v_{offset} = -\frac{1}{2}(vmin_{max})$ and the obtained maximum voltage transfer ratio is 0.866. The corresponding of d_0 and d_7 is given as

$$d_0 = d_7 = \frac{1}{2}(1 - d_1 - d_2) \tag{39}$$

4) Discontinuous PWM (DPWM)

In this method, only one zero vector is chosen in the switching pattern. The DPWM method is classified into two types. In the first DPWM method (DPWM1), the sequence of the switching is selected as V_0–V_1–V_2–V_2–V_1–V_0. In the second DPWM method (DPWM2), the sequence of the switching is selected as V_7–V_2–V_1–V_1–V_2 –V_7.

For the DPWM1, the duty cycles of the two zero vectors are:

$$d_7 = 0 \tag{40}$$

$$d_0 = 1 - d_1 - d_2 \tag{41}$$

The SVPWM method with the distribution of zero vectors shown in (40), (41) equivalents the CBPWM method when the offset voltage is given as

$$v_{offset} = -\frac{V_{dc}}{2} - v_{min} \tag{42}$$

For the DPWM2, the duty cycles of the two zero vectors are:

$$d_0 = d_7 = \frac{1}{2}(1 - d_1 - d_2) \tag{43}$$

The SVPWM method with the distribution of zero vectors shown in (40), (41) has matched the CBPWM method when the offset voltage component is chosen as (44)

$$v_{offset} = \frac{V_{dc}}{2} - v_{max} \tag{44}$$

4. Experimental setup and results

4.1 Experimental setup

The block diagram of the implementation of CPWM based on DSP and CPLD is shown in Fig. 9. The DSP is the main controller which executes the main programs including analog/digital converter, communicating with PC through serial communication interface (SCI) and with oscilloscope through peripheral communication interface (SPI). The function of DSP is to generate PWM signals by comparing the modulation signals with the triangular carrier signal. These PWM signals are fed to the CPLD. The pulse signals, which are used to control the power devices in the inverter stage, are obtained by using XNOR and NOT functions. These functions are implemented by CPLD.

To validate the performance of the CPWM method, the experiments are carried out by using the balanced three-phase power supply, three-phase *RL*

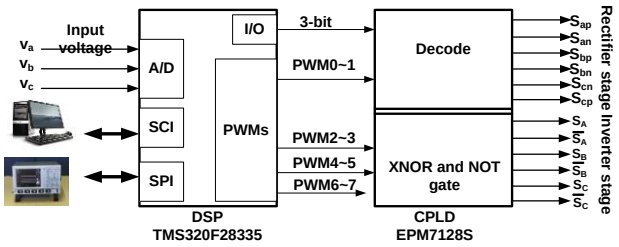

Figure. 9 The block diagram of the CBPWM

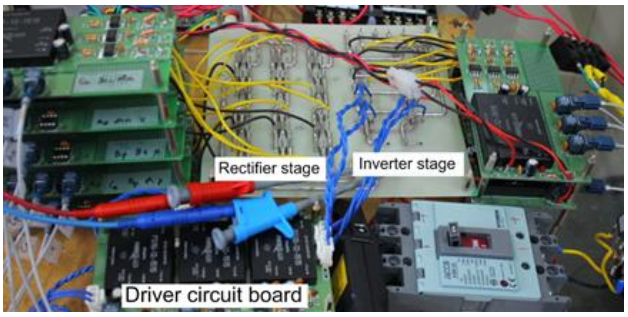

Figure. 10 The experimental setup of IMC.

load and *LC* filter. The parameters of the experimental system are given section IV. The control system is implemented by a 32-bit DSP TMS320F28335 operating with a clock frequency of 150 MHz and a CPLD EPM7128SLC84-15. The power switch IGBTs – G4PF50WD – have been used to implement the power circuit in the rectifier and the inverter stage. The carrier signal is 10 *kHz* symmetrical triangular signal, which is generated by up/down counter in DSP. The laboratory IMC prototype is shown in Fig. 10. The system parameters are given as following:

- Three-phase power supply for the IMC is set at 100V (V_{in}=100V) and the input frequency is 60Hz (f_{in}=60Hz).
- Input filter inductance L=1mH, input filter capacitance C=25μF.
- Three-phase RL load: R= 12Ω, L= 10mH.
- The output frequency: f_{out} = 50Hz.
- The voltage transfer ratio: m=0.6.
- Carrier frequency $f_{carrier}$=10kHz (T_s =100μs).

4.2 Experimental results

Figs. 11-15 show the waveform of input and output performances with DPWM1, DPWM2, SPWM, 3rdHYPWM and SYPWM, respectively. As can be seen, all input and output currents are almost sinusoidal waveforms except for the ripple due to the switching behavior. There is a small displacement angle between the input voltage and input current due to the input filter effect.

From the experimental results, it can be seen that the performance of the IMC such as sinusoidal

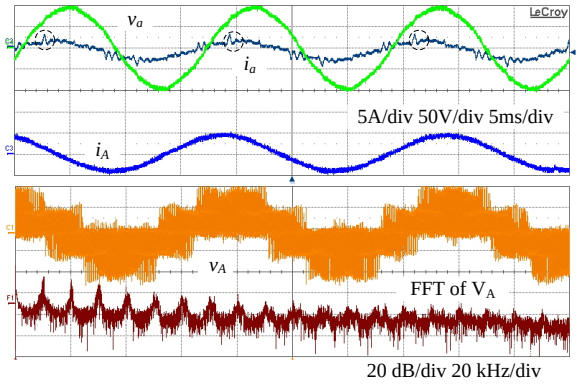

Figure. 11 Input voltage (v_a), input current (i_a), output voltage (v_A), output current (i_A) with DPWM1 strategy

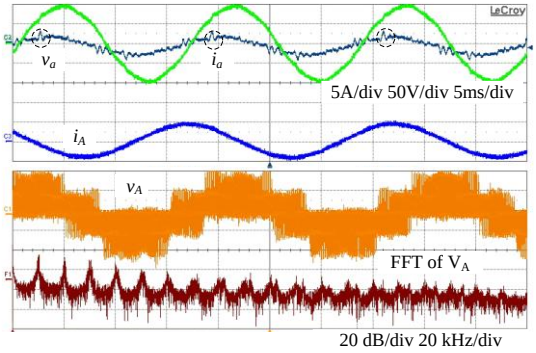

Figure. 12 Input voltage (v_a), input current (i_a), output voltage (v_A), output current (i_A) with DPWM2 strategy

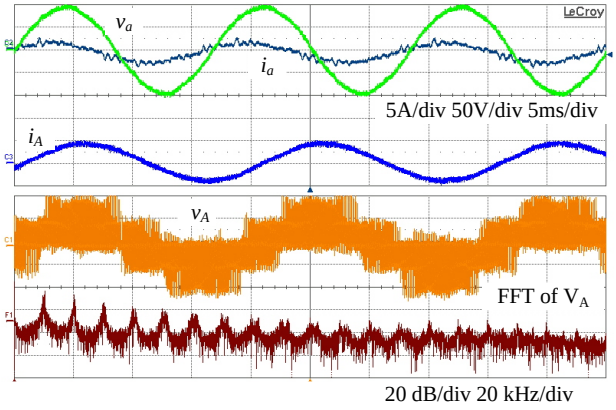

Figure. 13 Input voltage (v_a), input current (i_a), output voltage (v_A), output current (i_A) with SPWM strategy

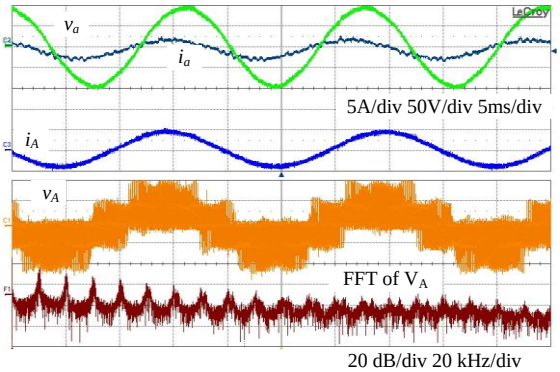

Figure. 14 Input voltage (v_a), input current (i_a), output voltage (v_A), output current (i_A) with 3rdHPWM strategy

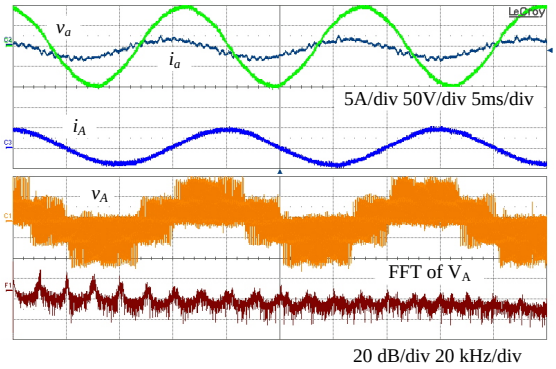

Figure. 15 Input voltage (v_a), input current (i_a), output voltage (v_A), output current (i_A) with SYPWM strategy

waveforms for both the input and output currents can be achieved by using the proposed CBPWM methods.

In DPWM1 and DPWM2 methods, only one active vector is used to synthesize the reference output voltage in the inverter stage. Therefore, in order to guarantee the zero dc-link current commutation in the rectifier stage, we have to insert a small interval for zero vectors at the sector transition. Therefore, the narrow pulses during sector transition in the rectifier stage cause some unexpected peaks in the input currents, as shown in Figs. 12 and 13. In a comparison with the input current waveform of DPWM method, input current waveforms of SPWM, 3rdHPWM and SYPWM do not contains the unexpected peaks.

4.3 Output voltage quality

The notion of harmonic flux on per-carrier cycle is useful to evaluate the waveform quality. The analysis of harmonic flux produced by the changing of the selected input current and output voltage vectors is adopted in [22, 23].

The per-carrier cycle harmonic flux error of the output voltage is calculated as follows:

$$\psi_h = \int_0^{T_s} (v_k - v_{out})\, dt \tag{45}$$

where vk is the output voltage vector of the k'th state, it changes according to the selected switching sequence of the rectifier and the inverter stages within the carrier cycle.

The per-carrier cycle harmonic flux error is normalized with respect to fundamental flux which is calculated by product the magnitude input phase voltage and half of control sampling period.

$$\psi_n = \frac{2}{T_s V_{in}} \psi_h \tag{46}$$

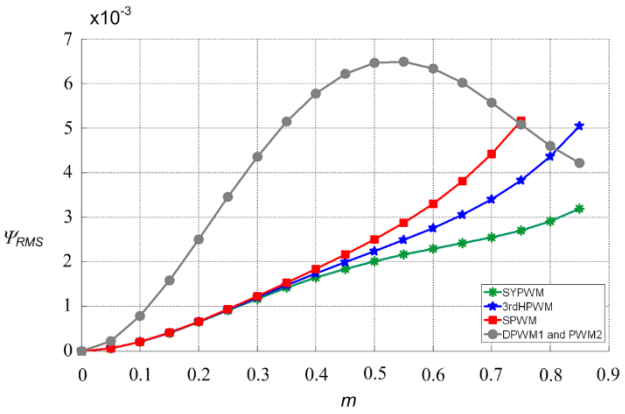

Figure. 16 The RMS value of harmonic flux as a function of voltage transfer ratio

The mean square ripple of the harmonic flux of output voltage during the carrier cycle can be calculated as shown in

$$F_\psi^2 = \frac{1}{T_s} \int_0^{T_s} \psi_{nr}^2 + \psi_{ni}^2\, dt \tag{47}$$

where ψ_{nr} and ψ_{ni} are the real and image components of the normalized harmonic flux error ψ_n.

The total RMS harmonic distortion factor is defined as the RMS flux ripple over an input sector and an output sector, as follows:

$$\psi_{RMS} = \sqrt{\frac{9}{\pi^2} \int_0^{\pi/3} \int_{-\pi/6}^{\pi/6} F_\psi^2 d\theta_{in} d\theta_{out}} \tag{48}$$

Fig. 16 shows the mean square ripple of the harmonics flux of output voltage as a function of the input current angle θin and output voltage angle θout at the voltage transfer ratio m of 0.6. Fig. 12 shows the RMS value of the harmonic flux of output voltage with different modulation schemes for various values of voltage transfer ratio. As can be seen, the best quality of the output voltage can be obtained with the SYPWM method.

5. Conclusion

In this paper, the novel CBPWM for the IMC is presented. The algorithm is easy to implement because it uses only one symmetrical triangular carrier with the fixed slopes to generate PWM signals. Furthermore, the proposed CBPWM is generalized by analysing the correlation between the CBPWM and SVPWM. The relationship between the distribution of zero vectors in SVPWM method and the type of the offset voltage in CBPWM method is derived and it is proven the proposed CBPWM method can generate any kind of the space vector

modulation scheme in SVPWM. A comparative evaluation of output performance with different CBPWM schemes is presented. It is shown that the sinusoidal input and output currents are obtained with all the CBPWM schemes. Furthermore, with this proposed CBPWM method, the calculation time is significantly reduced. The calculation time of the SVPWM method is 45 μs, while the calculation time of the proposed method is 22 μs.

Conflicts of Interest

Declare conflicts of interest or state "The authors declare no conflict of interest." Authors must identify and declare any personal circumstances or interest that may be perceived as inappropriately influencing the representation or interpretation of reported research results.

Author Contributions

Conceptualization, Dinh Tuyen Nguyen; methodology, Dinh Tuyen Nguyen; software, Dinh Tuyen Nguyen, and Hoai Phong Nguyen; validation, Dinh Tuyen Nguyen; formal analysis, Dinh Tuyen Nguyen, and Minh Thuyen Chau; investigation, Dinh Tuyen Nguyen; resources, Hoai Phong Nguyen, and Hoai Phong Nguyen; data curation, Dinh Tuyen Nguyen; writing—original draft preparation, Minh Thuyen Chau; writing—review and editing, Minh Thuyen Chau; visualization, Dinh Tuyen Nguyen, and Hoai Phong Nguyen; supervision, Dinh Tuyen Nguyen, and Hoai Phong Nguyen; project administration, Dinh Tuyen Nguyen; funding acquisition, Dinh Tuyen Nguyen, etc.

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Appendix

Table 1. Modulated switches, duty cycles of active vector and dc-link voltage according to the input current sector

Input sector	$\omega_{in}t$	**ON switch**	**Modulated switches and duty cycles**				**Instantaneous dc-link voltage (v_{dc})**		**Average dc-link voltage (V_{dc})**
1	$-\pi/6 .. \pi/6$	S_{ap}	S_{cn}	$-v_c/v_a$	S_{bn}	$-v_b/v_a$	v_{ac}	v_{ab}	$3V_{in}^2 / 2v_a$
2	$\pi/6 .. \pi/2$	S_{cn}	S_{ap}	$-v_a/v_c$	S_{bp}	$-v_b/v_c$	v_{ac}	v_{bc}	$-3V_{in}^2/2v_c$
3	$\pi/2 .. 5\pi/6$	S_{bp}	S_{an}	$-v_a/v_b$	S_{cn}	$-v_c/v_b$	v_{ba}	v_{bc}	$3V_{in}^2/2v_b$
4	$5\pi/6 .. 7\pi/6$	S_{an}	S_{bp}	$-v_b/v_a$	S_{cp}	$-v_c/v_a$	v_{ba}	v_{ca}	$-3V_{in}^2/2v_a$
5	$7\pi/6 .. 9\pi/6$	S_{cp}	S_{bn}	$-v_b/v_c$	S_{an}	$-v_a/v_c$	v_{ca}	v_{cb}	$3V_{in}^2/2v_c$
6	$9\pi/6 .. 11\pi/6$	S_{bn}	S_{ap}	$-v_a/v_b$	S_{cp}	$-v_c/v_b$	v_{cb}	v_{ab}	$-3V_{in}^2/2v_b$