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A review: Area, Power and Delay Efficient Multipliers

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Abstract:

Multipliers play an important role in today's digital signal processing (DSP) and various other applications. Multiplication is the most time consuming process in various signal processing operations like convolution, circular convolution, auto-correlation and cross-correlation. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. However area and speed are two conflicting constraints. So improving speed results always in larger areas. So here we try to find out the best trade off solution among the both of them. To have features like high speed and low power consumption multipliers several algorithms have been introduced .In this paper, we describes Multipliers by using various algorithm in VLSI technology.

Keywords— **Multipliers, VLSI design.**

I. INTRODUCTION

Multipliers play an important role in today's digital signal processing (DSP) and various other applications. Multiplication is an operation of scaling one number by another multiplication operation such as convolution, Discrete Fourier Transform, Fast Fourier transform etc. As there is need for greater computing power on battery-operated mobile devices, design emphasis has shifted from optimizing conventional delay time, area size to minimizing power dissipation while still maintaining the performance.

Traditionally multiplication algorithm "Shift and Add" has been implemented to design, which is not suitable from VLSI implementation and delay point of view. In order to achieve fast multiplication some important algorithms have been proposed in literature. These algorithms have been used in VLSI implementation of multiplier to achieve fast multiplication in circuits.

There are two multiplication schemes:

Serial Multiplication- [1] It is computing a set of partial products and then summing the partial products together. So it uses a successive addition algorithm. They are simple in structure because both the operands are entered in a serial manner. The multiplication result needs to be shifted by its position in the serial chain. Each processing element takes the result of the multiply and adds it to partial sum after it has been shifted. Therefore, the physical circuit requires less hardware and minimum amount of chip area. However, the speed performance of the serial multiplier is poor due to operands being entered sequentially. Therefore the physical circuit requires minimum amount of area and less hardware with increase in the rate of speed and delay. The multiplier bit bi are used to control 2:1 multiplexer, if bi=0, and n bit 0 word is sent to the adder, while bi=1 directs the multiplicand A to the input. Output of the adder is given to the product register. And this process repeats n number of times. The factor of 2n multiplying A is used to compensate for the 2^-n introduced by the right shift at the end of calculation.

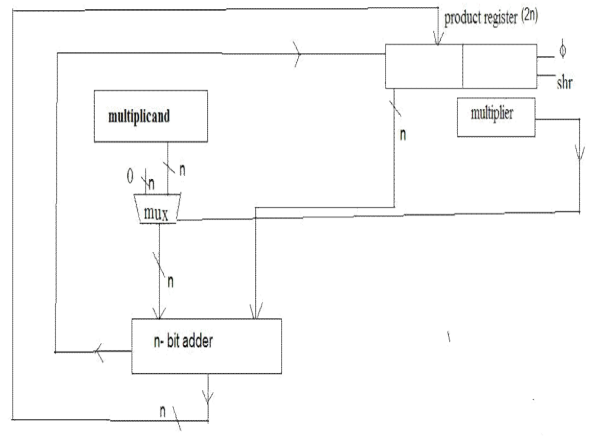

Fig 1-Block Diagram Serial Multiplier

Parallel Multiplication- [1] Partial products are generated simultaneously parallel implementations are used for high performance machine, when computation latency needs to be minimized. Improvements in Partial-Product Bit Reduction Techniques and then optimization of the Final Adder for the uneven signal arrival profile from the Multiplier Tree.

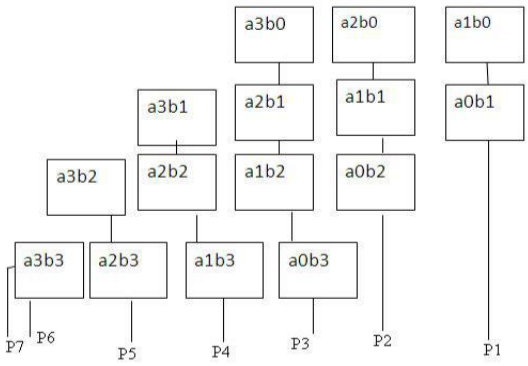

Fig 2- Block Diagram Parallel Multiplier

Advantages of parallel multiplication: -Comparing fig.1 and fig.2 both, parallel multiplication has more advantages than serial multiplication. As parallel type utilize lesser steps comparing serial one. So it is faster than serial multiplication.

The rest of the paper is organized as follows: related work is discussed in Section 2. The proposed system is explained in Section 3. In section 4, the conclusion and future work is described.

II. RELATED WORKS

Multipliers are one of the most important units of many digital computing systems. These circuits are generally implemented to perform multiplication serially or parallelly. It is found that the parallel multipliers are faster than the serial multiplier due to reduction in the number of processing steps. A lot of work has been done in this area to increase the field and compactness of array multiplier circuit. And also there are different algorithms like Booth's algorithm, Wallace tree algorithm, Dadda algorithm, etc. proposed in literature for this purpose. Some of the recent paper with their features, advantages and disadvantages are discussed in the proceeding paragraphs.

[2] In 1998, D.G. Crawley and G.A.J. Amaratunga proposed 8x8 bit time-optimal multiplier using Dadda scheme implemented as a 7-stage linear pipeline. The design uses automated layout techniques to avoid the problems associated with the irregularity of the scheme. It uses new pipelined carry look-ahead adder in final summation which contribute to the performance of multiplier. This multiplier is expected to operate at a maximum clock frequency of at least 50 MHZ. In this system it would permit the construction of a large, regular multiplier from smaller multiplier blocks that are themselves irregular. This would avoid the irregularity at the macro level.

[3] In 2009, Young-Ho Seo and Dong-Wook Kim proposed a new MAC architecture to execute the Multiplication- accumulation operation, which is key operation, for digital signal processing and multimedia information processing. By combining multiplication with accumulation and devising a hybrid type of carry save adder, it improves the performance. But the delay due to MAC operation was large. Hence merging it to the compression process of the partial products, has improved the overall performance of MAC almost twice then the previous work. But the proposed MAC required the hardware resources as much as pervious research.

Even though the performance has been increased about twice then the previous one but the problem with this system is delay has been slightly increased compared to previous research.

[4] In 2010, Ron S.Waters and Earl E.Swartzlander design Wallace high-speed multiplier by using half adders and full adders in their reduction phase. Half adders do not reduce the partial product bits. So we need to reduce half adders so as to reduce complexity. For this, modified Wallace reduction has been designed to reduce 80% of half adder by slightly increasing number of full adders. But then also both conventional Wallace reduction and modified Wallace reduction have same number of stages and ensure the same delay as conventional Wallace reduction. So the problem with this design is that it has more number of gates which increases the delay and area.

III PROPOSE SYSTEM

The proposed system has been traditionally used for the multiplication of two numbers in the decimal and binary way.

To reduce the delay, area and power, a 4x4 Multiplier is implemented using 4 2x2 multipliers and adders.

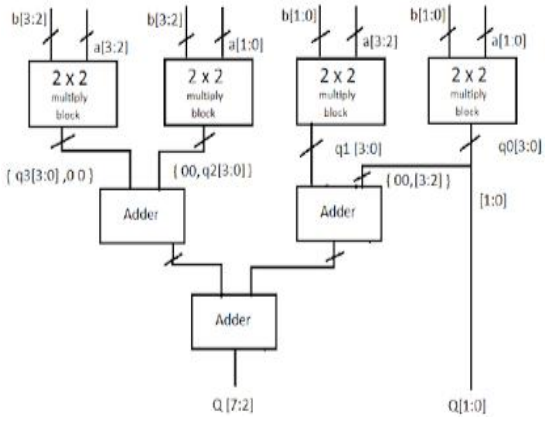

Fig 3- Block diagram of 4X4 Multiplier.

Generally as we know multiplication goes in two basic steps Partial product and then addition. So we tried to design different adders and compare their speed and complexity of circuit i.e. the area occupied.

While comparing the adders we found out that Ripple Carry Adder had a smaller area while having lesser speed, in contrast to which Carry Select Adders are high speed but possess a larger area. And a Carry Look Ahead Adder is in between the spectrum having a proper tradeoff between speed and area complexities. Hence among the three, Carry Look Ahead Adder has the least AREA DELAY PRODUCT. Hence we are going to use Carry Look Ahead Adder when it comes to optimization with both Area and Time.

After comparing the adders we turned to multipliers which perform partial product. By using various techniques in multipliers they compared the speed and Power consumption in them.

Initially here we have used 2x2 multiplier which is been inputted by two 4bit numbers A (A3A2A1A0) multiplicand and B (B3B2B1B0) multiplier. In this block the initial steps of multiplication is been done using various techniques so as to reduce the power and increase the speed. The output the 2x2 multiplier is given to the adder block so as to get optimize area. And at final output we get (7:0) product which will provide efficient delay, area and power.

IV. CONCLUSION

Multipliers are extensively used in digital signal processing (DSP) and various other applications. Multiplication can be done either serially or parallelly. But it is found that the parallel multipliers are faster than serial one's because it reduces the number of processing steps. The methods of multiplication process in propose multiplier is done by using simple logical operations than conventional multiplier. The primary objective of the propose system is to study and analysis high speed, compact area, high performance and low delay. Thus we propose 4X4 multiplier in VLSI technology to achieve these primary objectives. 4X4 multiplier will provide high speed, less area, low power consumption and delay.

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