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An Analysis of Novel CMOS Ring Oscillator Using LECTOR Technique with Minimum Leakage

Chandramohan K and Nikhil Saxena

Department of Electronics & Communication Engineering, ITM Gwalior, India
sathvikkadambala@gmail.com

ABSTRACT

when we require developing digital integrated circuits, then we are facing many challenges like the way of greater energy consumption. The mixture of minor procedure geometries, greater functional integration and higher clock speed shave contributed to important enhanced in power density, so there are many methods which can be utilized to decrease leakage power in the efficient way. In this paper we proposed a newest method known as LECTOR for designing CMOS Ring oscillator that significantly cuts down the leakage current without increasing the dynamic power dissipation. In this work we calculated leakage power and leakage current. We found that after using this novel technique, circuit leakage parameters reduces drastically. We used SPICE tool for simulation with 45nm technology mode. 0.7v and 1.0v supply voltage is used in this work.

Key words: CMOS ring oscillator, Leakage power, leakage current, LECTOR

INTRODUCTION

Power dissipation is a significant view in the design of CMOS VLSI circuits. Higher power consumption leads to diminish in the battery life in the circumstance of battery-powered usages and affects also packaging, and cooling costs and credibility. The power dissipation sources are:

- Capacitive power dissipation which is considering that the load tank age discharging and charging;
- Short-circuit currents due to the being of a conducting path amid the voltage supply and ground for the concise duration through that a logic gate create a transition; and
- Leakage current comprises of sub-threshold currents and reverse-bias diode. The former is due to the kept charge amid the bulk and groove of active transistors while the latter is due to the carrier diffusion amid the drain and OFF transistors source [1].

In this article ring oscillator exploiting CMOS technique can be realized thru connecting odd no. of inverter in closed loop as seem in figure1, whose output oscillates amid two voltage phase, representing false and true. The inverters are added in a sequence and the o/p of the final inverter is suggestions into first. An electronic oscillator is an electronic circuit which produce oscillating electronic signal, a periodic, mostly a square or a sine wave. Oscillators change direct current (DC) from a PS (power supply) to an alternating current (AC) signal. They are broadly exploited in several electronic devices. General instance of signals produced thru oscillators. Comprise signals broadcast through radio and clock signals which quartz clocks, and regulate pc and the sounds generate via video games and electronic beepers.

Oscillators are mostly characterized thru the frequency of their o/p signal:

- A low-frequency oscillator (LFO) is electronic oscillators that generate a frequency below ≈20 Hz. This term is usually exploited in the region of auditory synthesizers, to be different it from an audio frequency oscillator.
- It produces the auditory oscillator frequencies in the auditory range, around 16 Hz to 20 kHz.
- An RF oscillator produces signals in the radio frequency (RF) range of around 100 kHz to 100 GHz.

The ring oscillator is a factor of the TD (time delay) oscillator's. A time-delay oscillator comprises of a reverse amplifier with a delay factor amid the amplifier o/p and its i/p. The amplifier can have a grow larger than 1 at the intended oscillation frequency. Consider the first case where the amplifier o/p and i/p voltages are moment balanced at

a stable point. A little quantity of noise can cause the amplifier o/p to rise slightly. Later passing thru the time-delay factor, this minute o/p voltage alter will be presented to the amplifier i/p. The amplifier has a negative gain of greater than 1, thus the o/p will modify in the direction reverse to this i/p voltage. It'll modify thru a quantity larger than the i/p value, for an increase greater than 1. This reversed and amplified signal propagates from the o/p thru the time-delay and return to i/p where it is inverted and amplified again. The outcome of this in order loop is a square-wave signal at the amplifier o/p with the stage of all half of the square wave like to the TD. The square wave will develop unless the amplifier o/p voltage reaches its limits, the place it will stabilize. A more exact study will seem that the wave which grows from the primary noise may not be square as it grows, but it will become square as the amplifier arrive at its o/p limits.

Oscillators planned to produce higher-power AC o/p from a DC supply are generally called as inverters. Oscillator activate, when power is initial applied, random noise is produced in active device after which amplified. This noise is feedback positively thru frequency elective circuits to the i/p where it's amplified once more etc. CMOS ring oscillator huge range of frequency of oscillations, lower power consumption and reliable realization on Si with reduced die size and hence a suitable option for implementing system on chip. Hence it's a defy to design a ring oscillator with higher frequency range, lower power consumption and reduce area. The proposed three phase ring oscillator designed with the object of obtaining better performance in word of these parameters.

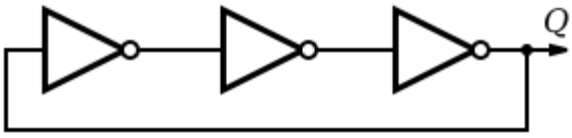
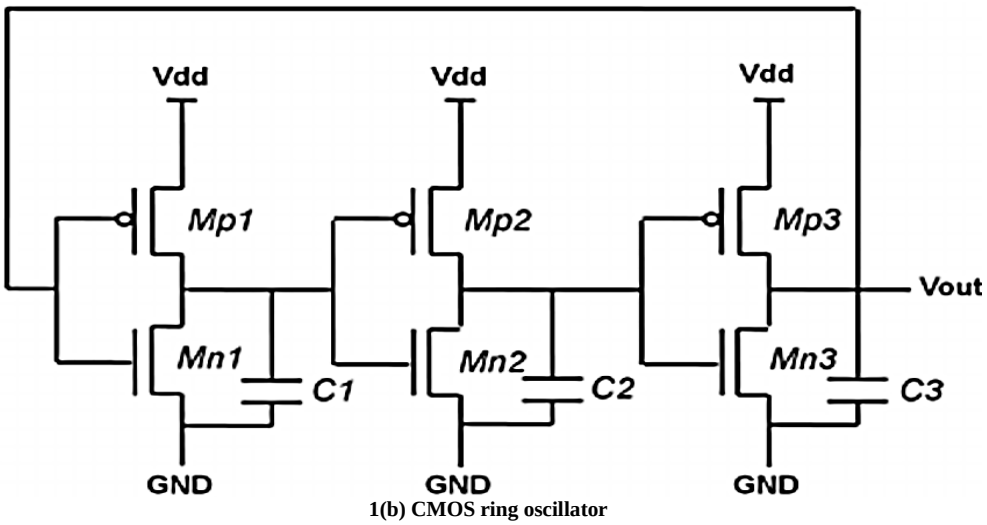


Fig. 1(a) Symbol diagram of ring oscillator



1(b) CMOS ring oscillator

Fig. 1 (a) Symbol diagram of ring oscillator (b) CMOS ring oscillator

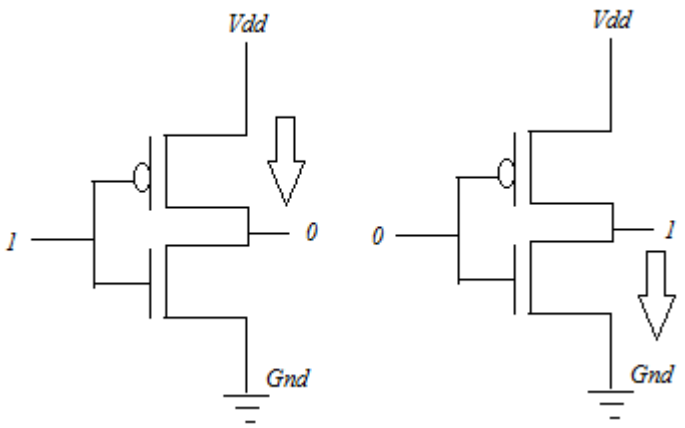


Fig. 2 CMOS Invertors

Invertors

Static CMOS circuits exploit NMOS pull-down and PMOS pull-up network to implement logic gates or logic function in integrated circuit. Leakage power (LP) of a CMOS transistor is dependent on oxide width and gate length. To lessen the dynamic power, the supply voltage (SV) is decreased which leads to the performance degradation. To speed increase the device, the threshold voltage will have to even be scaled down together with the SV that outcomes in exponential rise in the sub-threshold leakage current, thus enhance in the static power dissipation. The main elements of leakage current in a MOS transistor are illustrating in Fig. 2[2]. Sub-threshold leakage current; which is the reverse current fluent via the OFF transistor, indicated with arrows in Figure2. As the technology scales below that is the decrease of characteristic size of transistor, the channel length reductions, thus growing the quantity of LP in the whole power dissipated [2].

LECTOR Technique

The advent of digital integrated circuits is dominated by higher power consumption. It's a trade-off amid technology static power and scaling power consumption in CMOS integrated circuit design. In current CMOS technology, LP consumption is very significant. International Technology Know-how Road map for semiconductors info which LP consumptions dominates the whole chip power consumption as technology advances to nanoscale. In mobility computing and mobility communication usage powered thru battery, the battery life is a premier worry. LP loss is delicate in CMOS VLSI circuits like it leaks the battery even when tools are in idle state. To reduce sub-threshold LP with total power in CMOS ring oscillator circuits a new circuit technique LSSR technique is proposed in this work. This method decreases highest quantity of LP during deep sleep mode, greatest power decrease during dynamic (clocked) mode and has a provision of preserving state in lowest power sleep mode i.e. state retention.

In the proposed method, we present two LCT (an n-type and p-type) inside the logic gate for that all LCT (leakage control transistor) gate terminals are controlled the other source. In this arrangement, some of the LCTs is mostly '*near it is cut-off voltage*' for any I/P combination. This enhanced the opposition of the path from V_{dd} to GND, leading to important reduction in leakage currents. The vital characteristic of LECTOR is which it works effective in both idle and active phase of the circuit, resulting in improved leakage reduction equated to other methods.

In LECTOR method, two leakage manage transistors are presented amid pull-down inboard and pull-up n/w the logic gate (one NMOS for pull-down and one PMOS for pull-up) for that the gate terminal of all LCT is managed via the way of the supply of the other. Fig. 4 make sure which a LCTs always retard in its neighbouring cut-off area [2]. The LECTOR CMOS gate topology is seeming in Fig. 4. The all LCT gate terminal is controlled via the sender of the other, hence named as self-organized stacked transistors. As LCTs are no external circuit, self-controlled is necessary; thus the restriction with the sleep transistor method has been control. The LCTs introduction are raises the resistance of the path from V*dd* to Gnd, thus lessening the leakage current. LECTOR approach is seemed with the circumstance of an inverter in detail. A LECTOR INVERTER is illustrated in Fig. 4. A PMOS is presented as a NMOS and LCT1 as LCT2 amid two nodes of inverter. The inverter o/p is taken from the linked drain nodes LCT2 and LCT1. The LCT2 and LCT1 are sources nodes for N2 and N1 nodes separately the pull-down and pull-up logic. The LCT2 and LCT1 gates are controlled thru the potential on LCT1 and LCT2 source terminal separately. This connection each time saves one of the two LCTs in it is neighbouring cut-off region for any input [2].

When input A = 0, V*dd* = 1V, the voltage at the node N2 is 800 mV. LCT1 can't be wholly turned OFF as the voltage is not enough. Therefore, the LCT1 counteraction will be neighbouring to but slightly lesser than it's OFF counteraction, allowing conduction. The resistance provided by LCT1, even though not equal to the OFF resistance, rises the counteraction in the route of SV to ground, so scarcity the sub-threshold leakage current, attaining lack in leakage power. Similarly, when input A = 1, the voltage at the node N1 is 200 mV; hence LCT2 will be operated in near cut-off state. Every transistors phase in the LECTOR inverter for every viable i/p are show in Table -1[1].

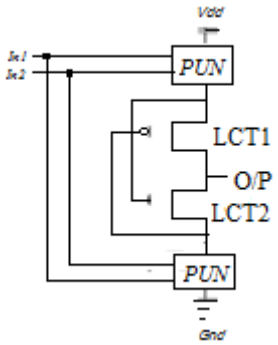


Fig. 3 Lector CMOS Gate

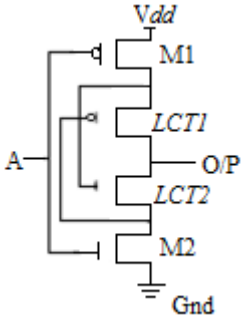


Fig. 4 LECTOR based CMOS Inverter

Table -1 State Matrix of LCT Inverter

Transistor Reference	Input Vector(A)	
	0	1
M1	ON State	OFF State
M2	OFF State	ON State
LCT1	Near Cut-off State	ON State
LCT2	ON State	Near Cut-off State

Along with the resistance within the path, the gate propagation delay moreover will get amplified. The transistors of LCT inverter are sized such that the propagation delay is diminished or similar to its base case. In the sleep related technique, the sleep transistors may be capable to isolate the PS and/or ground from the rest of the transistors of the gate. Hence, they necessity to be creates bulkier dispel more dynamic power. This offsets the savings yielded when the circuit is idle. Sleep transistor method based on I/P vector and it requirements extra circuitry to monitor and control the switching of sleep transistors, consuming power in both idle and active states. In assessment, LECTOR generates the required control signals within the gate and is also vector independent. Two transistors are added in LECTOR method in every path from V*dd* to GND irrespective of number of transistors in pull-down and pull-up network. While, forced stacks have 100% area overhead. The loading requisite with LCTs is a regular that is much lesser. Whereas, the loading necessities with forced stacks dependent on no. of transistors added and are huge. Hence, the performance degradation is in important in the circumstance of LECTOR, and we control the disadvantage faced thru forced stack method [1].

PROPOSED CIRCUIT

Various circuit applications of the LECTOR method are explored in this section. The LECTOR methods are applied to the CMOS circuit and calculate the quantity of LP diminished by LECTOR technique.

Lector based CMOS Ring Oscillator

In LECTOR implementation, needs only two extra transistors to be placed between the pull-down and pull-up network at the node. Three lector dependent CMOS inverters are linked continuously in Fig. 5. First Inverter's o/p is exploited as a input for second inverter and the second inverters output is the third inverters input and the o/p of the last inverter is feedback to first, 3-stage CMOS ring oscillator implement with first invertors connected LCT1, LCT2 between M1 and M2, second invertors connected LCT3, LCT4 between M4, M3 and third invertors connected LCT5, LCT6 between M5 and M6. Two LCT (PMOS) and (NMOS) are presented amid the nodes and the pull-up - pull-down logic of the CMOS oscillator. The drain nodes of each transistor are linked gather to form the o/p node of the CMOS oscillator. The transistors source nodes are linked to nodes and of pull-down and pull-up logic, respectively. The switching of transistors is control via the voltage potentials at nodes. This wiring configuration makes sure that one LCTs is continually *near its cut-off region*, irrespective of I/P voltage applied to the CMOS oscillator [2].

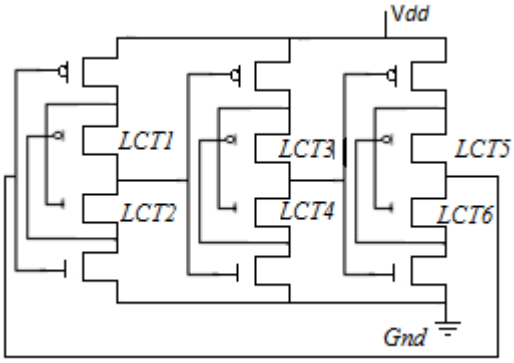


Fig. 5 LACTOR Based Ring Oscillator

RESULTS AND SIMULATION

Parameter	Abhay Kumar 2015	Yusuf Jeme H Bozorg 2014	Conventional CMOS Oscillator	Proposed work	Proposed work
Technique	Tail current Improvement	Differential Gilbert cell Structure	-	LECTOR	LECTOR
Supply Voltage	1.8V	1.0V	1.0V	1.0V	0.7V
Channel Length	180nm	65nm	45nm	45nm	45nm
Leakage power	0.2mw	1.49mw	207.2803u	95.4835u	20.0960u
Leakage current	-	-	207.2803u	95.4835u	28.7086u

CONCLUSION AND FUTURE WORK

In this article we use LACTOR technique on CMOS ring oscillator. It is very effective technique for reducing leakage in digital circuits. After simulation performed on SPICE tool with 45nm technology node we found that the power consumption, leakage current is reduced drastically in comparison to conventional CMOS ring oscillator. It is very effective technique for diminished the leakage of CMOS circuit. We can further lessen the leakage of CMOS ring oscillator by exploiting dissimilar leakage diminished method available for CMOS circuit. In this work we use 45nm technology node with 1.0V and 0.7V PS we can also further scale down the technology node (channel length) upto 32nm, 22nm and so on. For improvement in results like propagation delay, leakage power, leakage current etc.

REFERENCES

[1] Narender Hanchate and Nagarajan Ranganathan, LECTOR: A Technique for Leakage Reduction in CMOS Circuits, *IEEE Transaction on VLSI*, **2004**, 12,196-2052.
[2] Jyoti Tiwari and Sachin Bandewar, To Reduce the Leakage Power of CMOS Logic Circuit through LACTOR Technique, *International Journal of Emerging Technology and Advanced Engineering*, **2015**, 5, 261-269.
[3] AP Chandrakasan and RW Brodersen, Minimizing Power Consumption in Digital CMOS Circuits, *IEEE Proceedings of IEEE*, **1995,** 83 (4), *498-523*.
[4] JP Halter and F Najm, A Gate-Level Leakage Power Reduction Method for Ultralow-Power CMOS Circuits, *Proceedings of IEEE Custom Integrated Circuits Conference*, **1997**, 475–478.
[5] L Wei, Z Chen, M Johnson and K Roy, Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits, *Proceedings of 35th Design Automation Conference*, **1998**, 489–492.
[6] S Narendra, S Borkar, V De, D Antoniadis and AP Chandrakasan, Scaling of Stack Effect and its Application for Leakage Reduction, *Proceedings of IEEE ISLPLED*, **2001**, 195–200.