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Design and Evaluation of PUC (Packed U Cell) Topology at Different Levels & Loads in Terms of THD

Rajanand Patnaik N and Ravindranath Tagore Y

Department of Electrical & Electronics Engineering, VLITS, Guntur, AP, India
rajanand.ee@gmail.com

ABSTRACT

Now a day's industrial applications need high power equipment for conversion of power. At medium voltage applications, to associate one and only power semiconductor switch directly could be a not much productive concept. To conquer this multilevel power converter structure has been presented and concentrated on as an elective in high power and medium voltage applications. Renewable sources like photovoltaic, wind, fuel cells are often handily interfaced to a multilevel converter for high power applications. This paper discussing about PUC converter which is the most advanced topologies of all multilevel converters and having a merit of reduced device count. A comparison is going to be shown for 7, 15, 31 levels of PUC converter with different loads in terms of Total Harmonic Distortion (THD)%. The simulations are performed by using MATLAB/Simulink software.

Key words: Multilevel Converter**,** Packed U Cell design, THD, Variable Loads

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INTRODUCTION

Now a day's the usage of Multilevel Converters (MLC) are widely used in industry for medium voltage and high power operations. MLC are playing a vital role due to their low harmonic content in output. By varying the switching states of MLC it has various output voltage levels can be produced. In multilevel concept as increasing the voltage levels the THD% in output voltage waveform reduces. Existing concepts of multilevel topologies are following: neutral point-clamped topology (NPC) proposed by Nabae *et al.* [1]; flying capacitor topology (FC) proposed by Meynard *et al.* [2]; and classic cascaded H-bridges proposed by Peng *et al.* [3], in these topologies abounding drawbacks are found if voltage levels are increased. Usually multilevel converter comprises of number of switches, capacitors and DC voltage sources by increasing the voltage level the device count also increased, results in more price and it is difficult in implementation.

So researchers are focused in creating the new ideas in multilevel converters with more benefits in each and every aspect. In existing concepts, such as Cascaded H-bridge topology had more dc voltage sources it may result in the more no of transformers [4]-[8]. So in perspective of all these, a transformer-less converter arrangement is outlined in this paper which is called Packed U Cell (PUC) [9] topology. It accomplishes high power conversion quality by reducing the device count and low switching disturbances with respective to decreased in cost, circuit complexity at higher voltage levels there by avoids in bulky installations compared to existing topologies.

DESIGN AND EVALUATION OF PUC (Packed U Cell) TOPOLOGY

It contains of packed u cells (PUC). Each U cell has an arrangement of two switches and one capacitor. It offers high-energy conversion quality using a small amount of capacitors and power devices, and appropriately they have low production cost. It is very simple in terms of interconnection of components [9]. In this topology number of levels can be recognized by using the following equation:

$$2^{n+1} - 1 = \text{Number of levels} \qquad \text{where n=1,2,3…} \tag{1}$$

No of capacitors can be recognized by using the following equation:

$$N = 2^{Nc+1} - 1 \tag{2}$$

where N is the no of voltage levels, Nc is the number of capacitors Similarly the quantity of voltage levels N with individual to the quantity of switches Nsw given by following equation:

$$N = 2^{\frac{Nsw}{2}} - 1 \quad (3)$$

In fact, that above equations show the advantages of this topology not only utilizing single DC source but also the reduced number of power switches used to generate the desired voltage levels. For the 7, 15, 31, PUC topology six, eight, ten active switches and two, three, four sources are required compared to the other topologies and the comparison Table 1 give the clear performance of this topology. The main applications of this topology are PV applications, Motor drives etc. It offers better power quality in terms of achievable number of voltage levels, against other multilevel topologies and reliability of this system is more.

Evaluation of Seven Level

The output voltage levels are recorded in Table 2. It should be described that Sd, Se and Sf are working in complementary of Sa, Sb and Sc. So each brace of (Sa, Sd), (Sb, Se) and (Sc, Sf) cannot conduct at the same time. The switching voltage sequence can be given in Table 2. From the table the voltages are as V1, V1-V2, V2, 0, -V2, V2-V1, -V1 and the voltage values are 150 and 50 [10]. Here IGBT switches are used because it is a sort of transistor which works with a greater amount of power transfer and contains a higher switching speed with high efficient. 6IGBT switches are utilized in 7level PUC topology and it can be divided into 2 legs, hence three switches from one leg which is as show in Fig. 1.

Table-1 Comparison of Various Topologies with PUC Topology

Topologies	7-level			15-level			31-level		
	Capacitors	Diodes	Switches	Capacitors	Diodes	Switches	Capacitors	Diodes	Switches
NPC	6	10	12	14	26	28	30	58	60
FC	6	0	12	14	0	28	30	0	60
CHB	3	0	8	7	0	28	15	0	60
HCHB	2	0	8	3	0	12	4	0	16
PUC	2	0	6	3	0	8	4	0	10

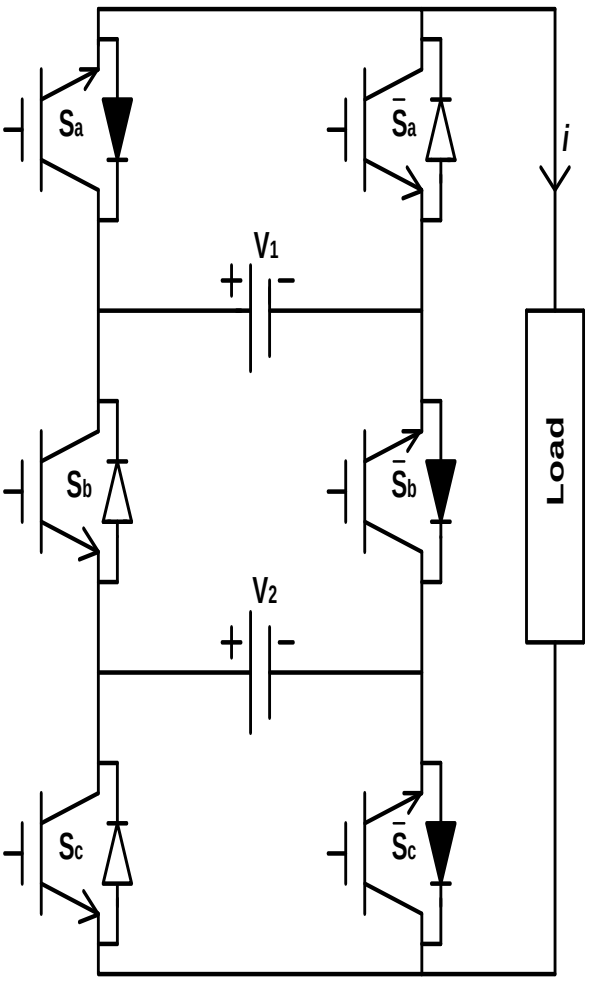

Fig.1.Seven level converter

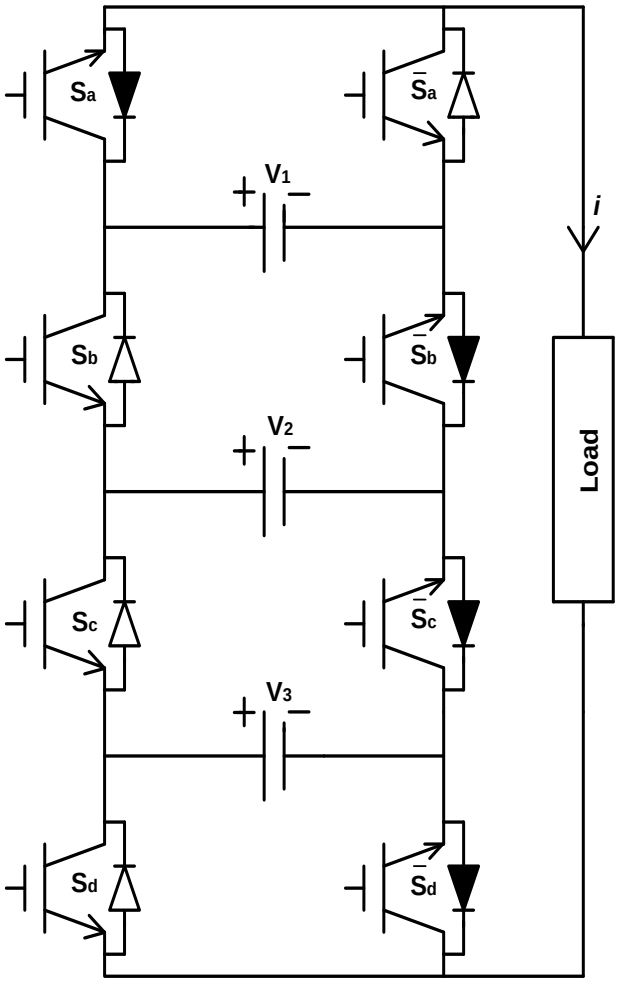

Fig.2.Fifteen level converter

Table-2 Switching States for 7-level

State	Sa	Sb	Sc	Voltage
1	On	Off	Off	V1
2	On	Off	On	V1-V2
3	On	On	Off	V2
4	On	On	On	0
5	Off	Off	Off	0
6	Off	Off	On	-V2
7	Off	On	Off	V2-V1
8	Off	On	On	-V1

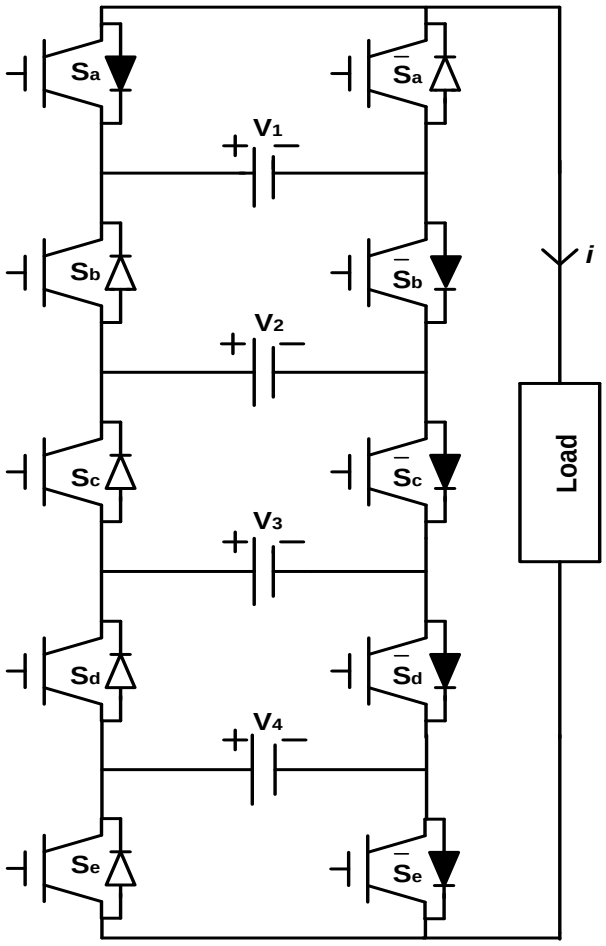

Fig.3. Thirty-one level converter

Table-3 Switching States for 15-level

States	Sa	Sb	Sc	Sd	Voltage
1	On	Off	Off	Off	V1
2	On	Off	On	Off	V1-V2+V3
3	On	Off	Off	On	V1-V3
4	On	Off	On	On	V1-V2
5	On	On	Off	Off	V2
6	On	On	Off	On	V2-V3
7	On	On	On	Off	V3
8	On	On	On	On	0
9	Off	Off	Off	On	-V3
10	Off	Off	On	Off	V3-V2
11	Off	Off	On	On	-V2
12	Off	On	Off	Off	V2-V1
13	Off	On	On	Off	V3-V1
14	Off	On	Off	On	V2-V1-V3
15	Off	On	On	On	-V1

Table-4 Switching States for 31-level

State	Sa	Sb	Sc	Sd	Se	Voltage
30	On	Off	Off	Off	Off	V1
29	On	Off	Off	On	Off	V1-V4
28	On	Off	Off	Off	On	V1-V3+V4
27	On	Off	Off	On	On	V1-V3
26	On	Off	On	Off	Off	V1-V2+V3
25	On	Off	On	On	Off	V1-V2+V3+V4
24	On	Off	On	Off	On	V1-V2+V4
23	On	Off	On	On	On	V1-V2
22	On	On	Off	Off	Off	V2
21	On	On	Off	On	Off	V2-V4
20	On	On	Off	Off	On	V2-V3+V4
19	On	On	Off	On	On	V2-V3
18	On	On	On	Off	Off	V3
17	On	On	On	On	Off	V3-V4
16	On	On	On	Off	On	V4
15	On	On	On	On	On	0
14	Off	Off	Off	On	Off	-V4
13	Off	Off	Off	Off	On	-V3+V4
12	Off	Off	Off	On	On	-V3
11	Off	Off	On	Off	Off	-V2+V3
10	Off	Off	On	On	Off	-V2+V3-V4
9	Off	Off	On	Off	On	-V2+V4
8	Off	Off	On	On	On	-V2
7	Off	On	Off	Off	Off	-V1+V2
6	Off	On	Off	On	Off	-V1+V2-V4
5	Off	On	Off	Off	On	-V1+V2-V3+V4
4	Off	On	Off	On	On	-V1+V2-V3
3	Off	On	On	Off	Off	-V1+V3
2	Off	On	On	On	Off	-V1+V3-V4
1	Off	On	On	Off	On	-V1+V4
0	Off	On	On	On	On	-V1

Evaluation of Fifteen Level

Table 3 shows the switching sequence of the fifteen level operation operated in case of $\frac{V1}{V2}=\frac{3}{7}$ and $\frac{V2}{V3}=3$ and design is shown in Fig. 2. Switches S_a and $\bar{S}_a$ are operated as complimentary, but only S_a, S_b, S_c, S_d switch is considered in table. Here we have taken the values as V1=420V, V2=180V and V3=60V [11].

Evaluation of Thirty-One Level

The switching Table 4 shows the analysis of switching operation for thirty-one level and Fig. 3 shows the topology of 31 level inverter. The pure sinusoidal waveform can be obtained by increasing the voltage levels hence the input voltages are [12]

$$V1=Vdc, V2=Vdc\frac{7}{15}, V3=Vdc\frac{3}{15}, V4=Vdc\frac{1}{15}$$

RESULTS AND DISCUSSION

Simulation of seven, fifteen, thirty-one levels of multilevel inverter at R, RL, RLC, Motor loads are performed by using matlab software and the comparison for Total Harmonic Distortion of voltage and current is shown for every loads at each level are performed.

Analysis of Seven Level Inverter

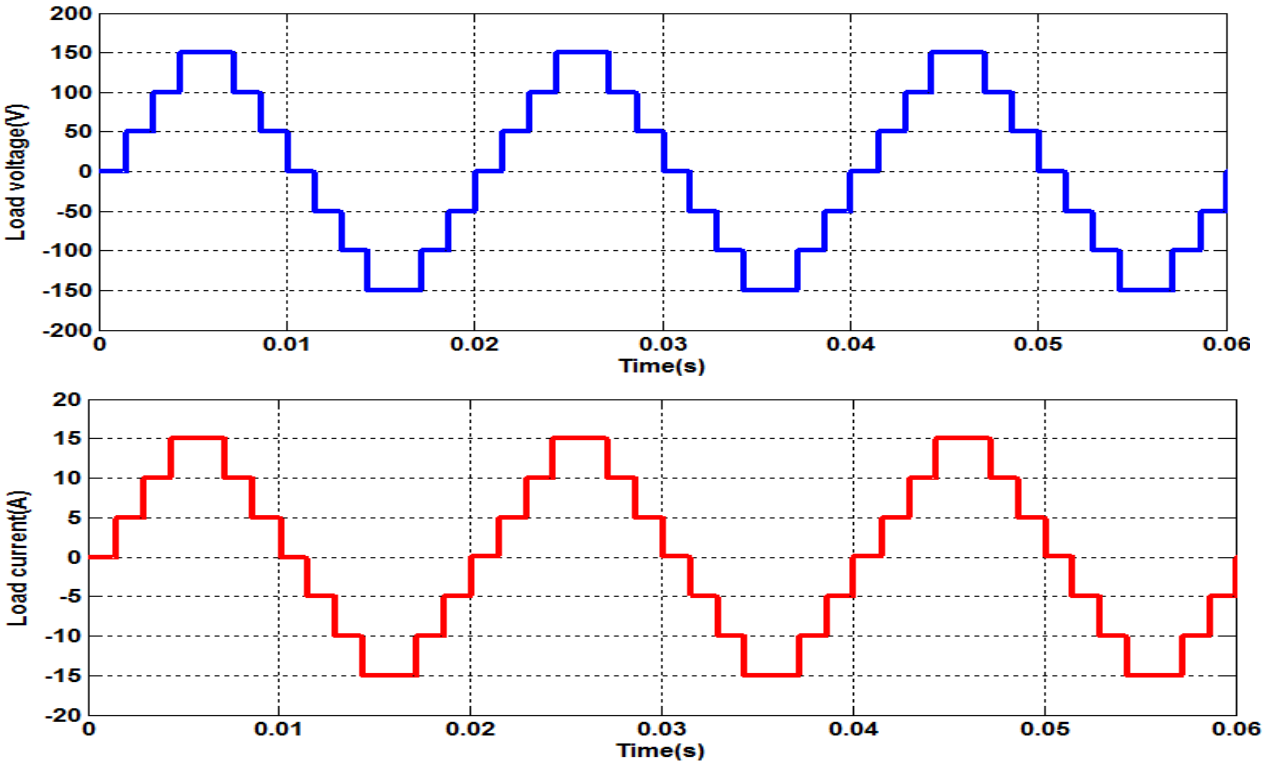

Fig.4. Output voltage current for Seven level R-load

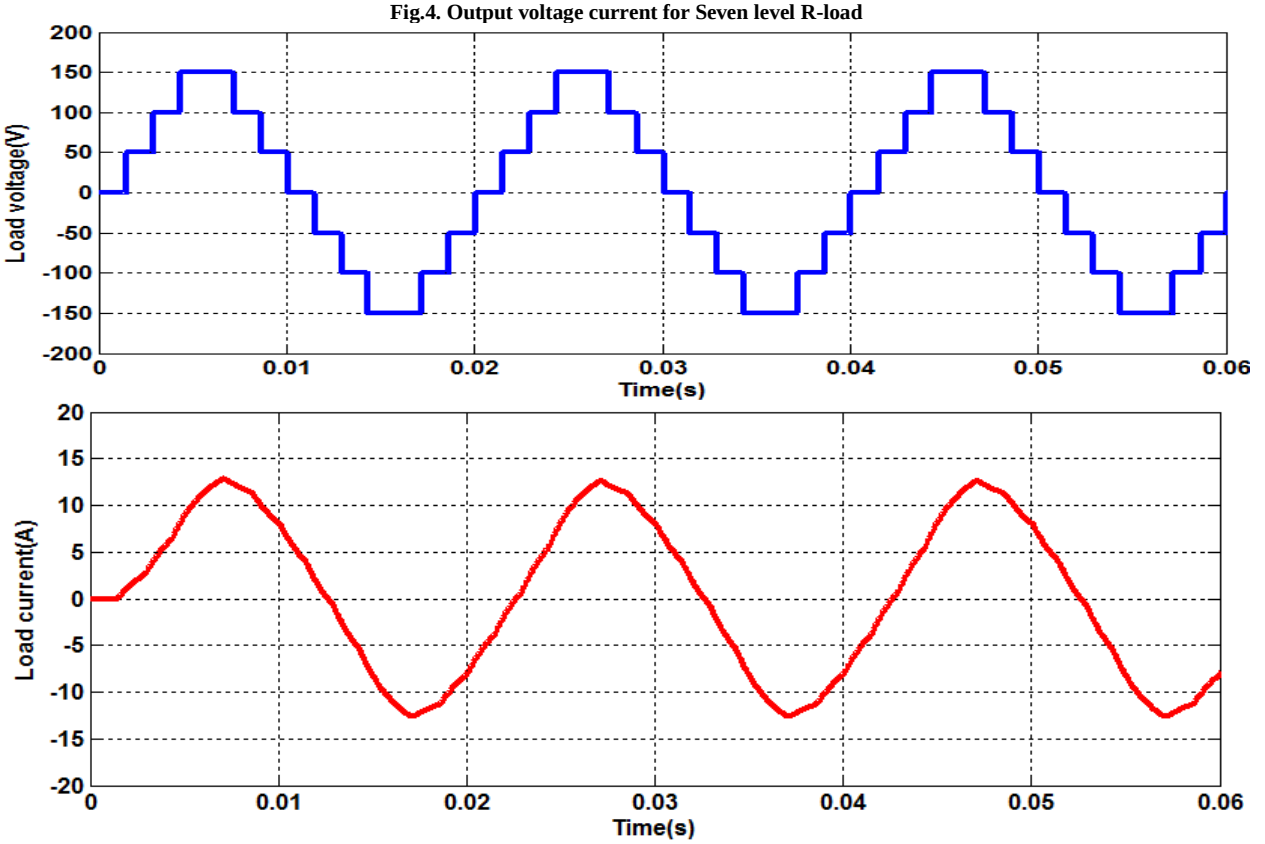

Fig.5. Output voltage current for Seven level RL-load

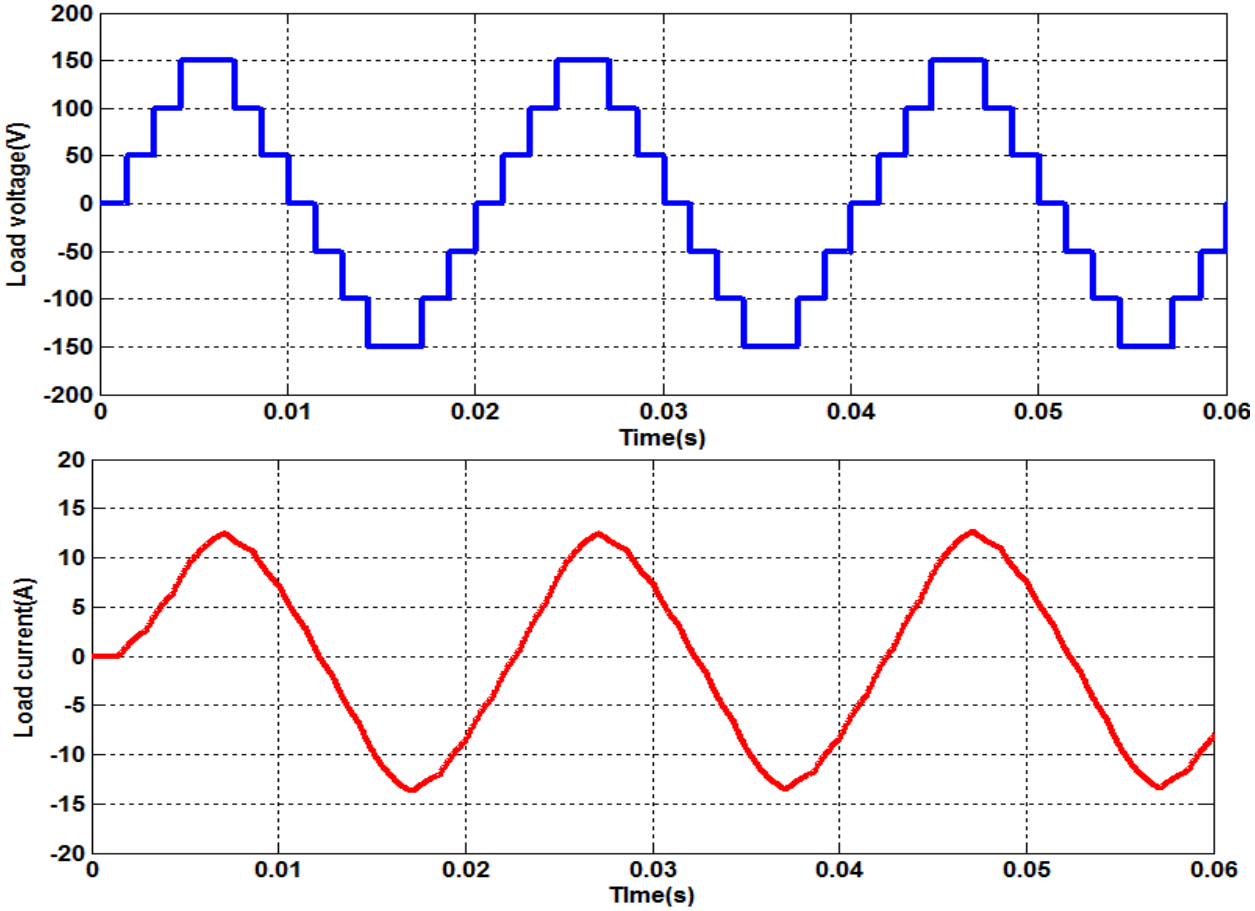

Fig.6. Output voltage current for Seven level RLC-load

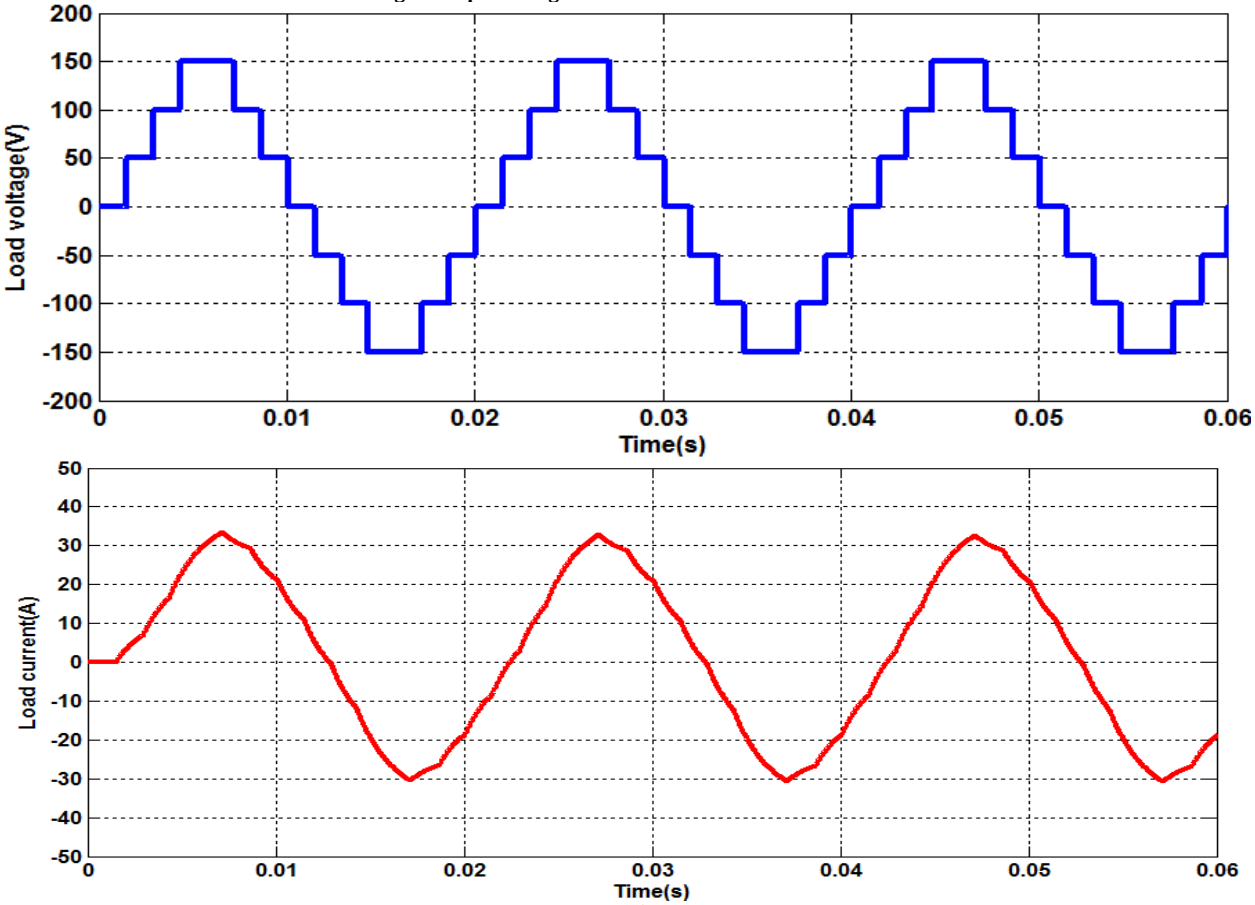

Fig.7. Output voltage current for Seven Level Motor-load

Analysis of Fifteen Level Inverter

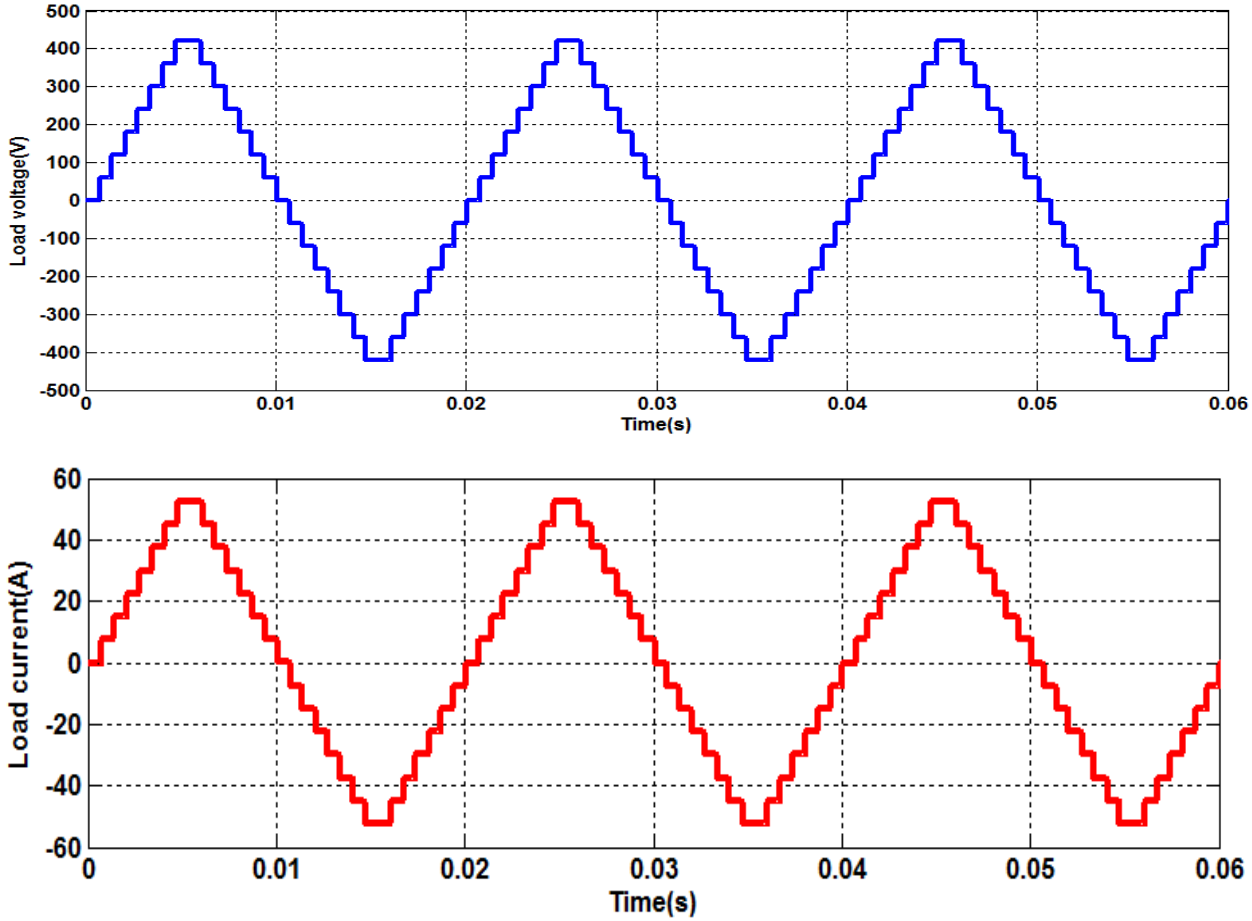

Fig.8. Output voltage current for Fifteen level R-load

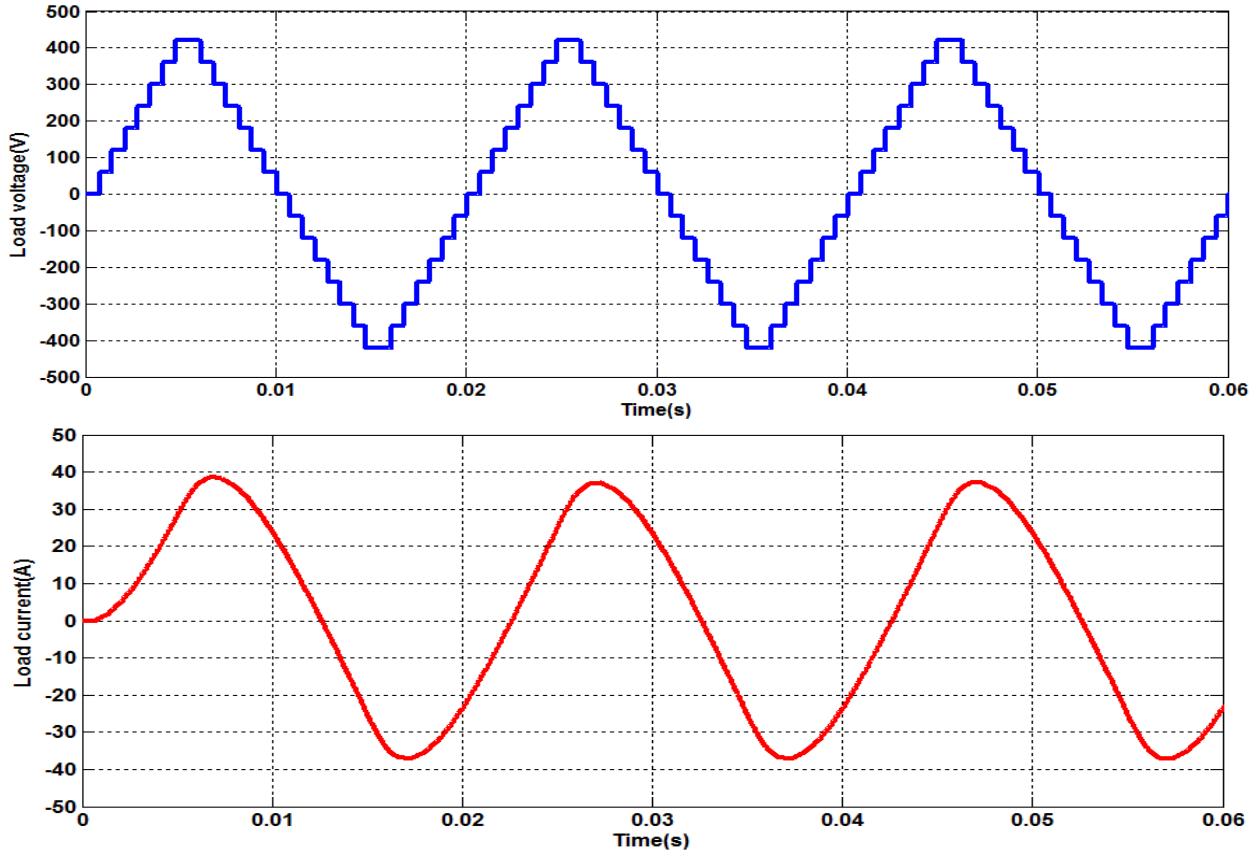

Fig.9. Output voltage current for Fifteen level RL-load

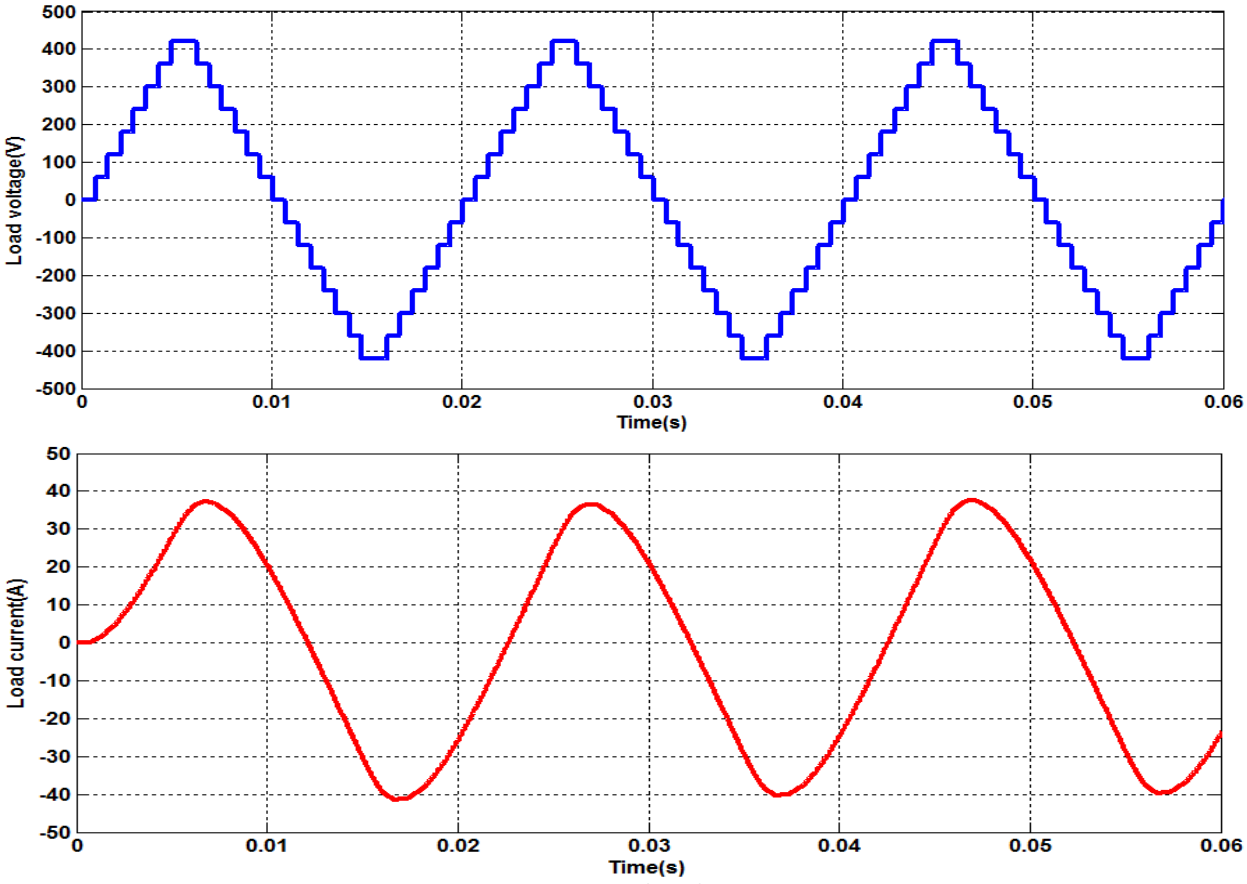

Fig.10. Output voltage current for Fifteen level RLC-load

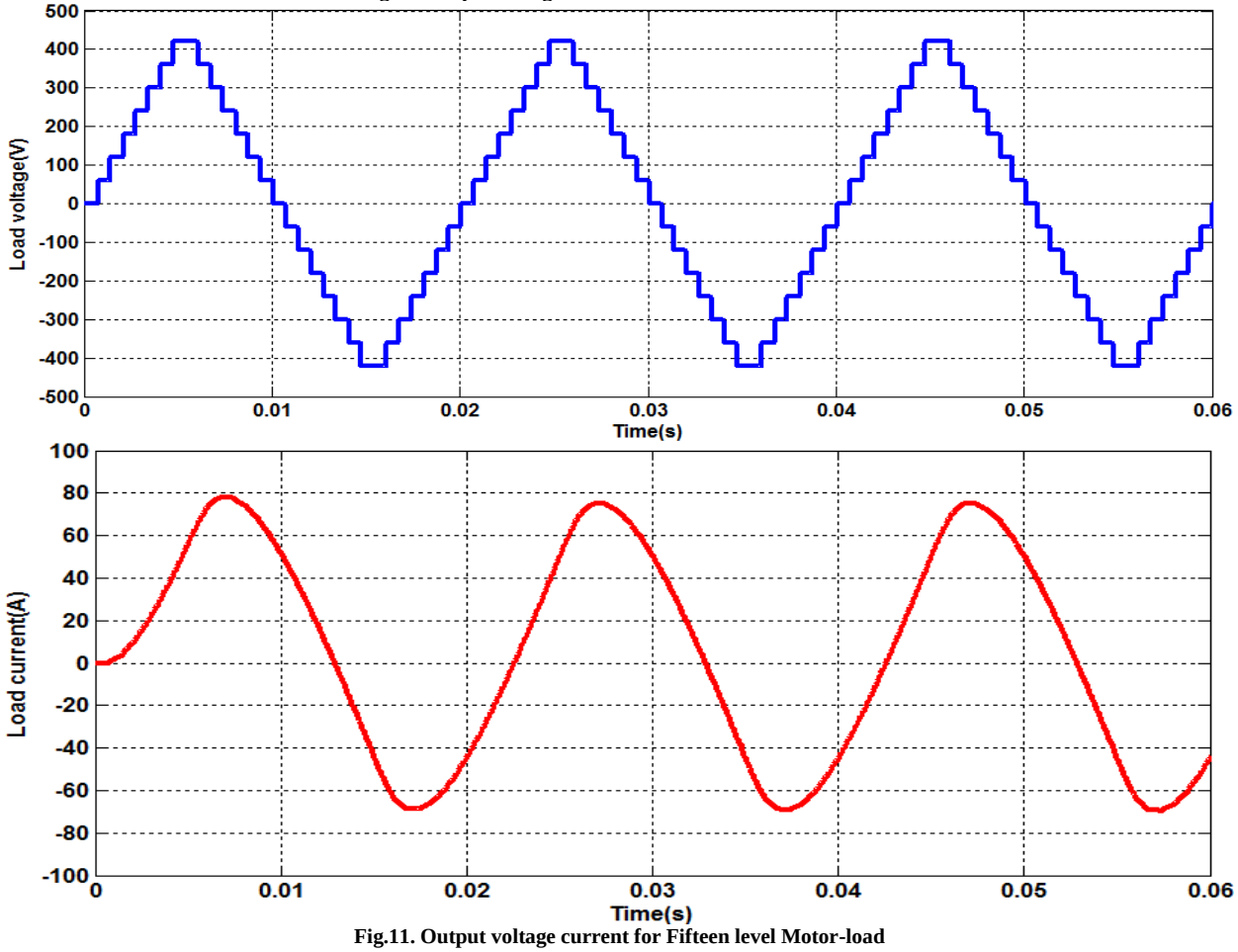

Fig.11. Output voltage current for Fifteen level Motor-load

Analysis of Thirty-one Level Inverter

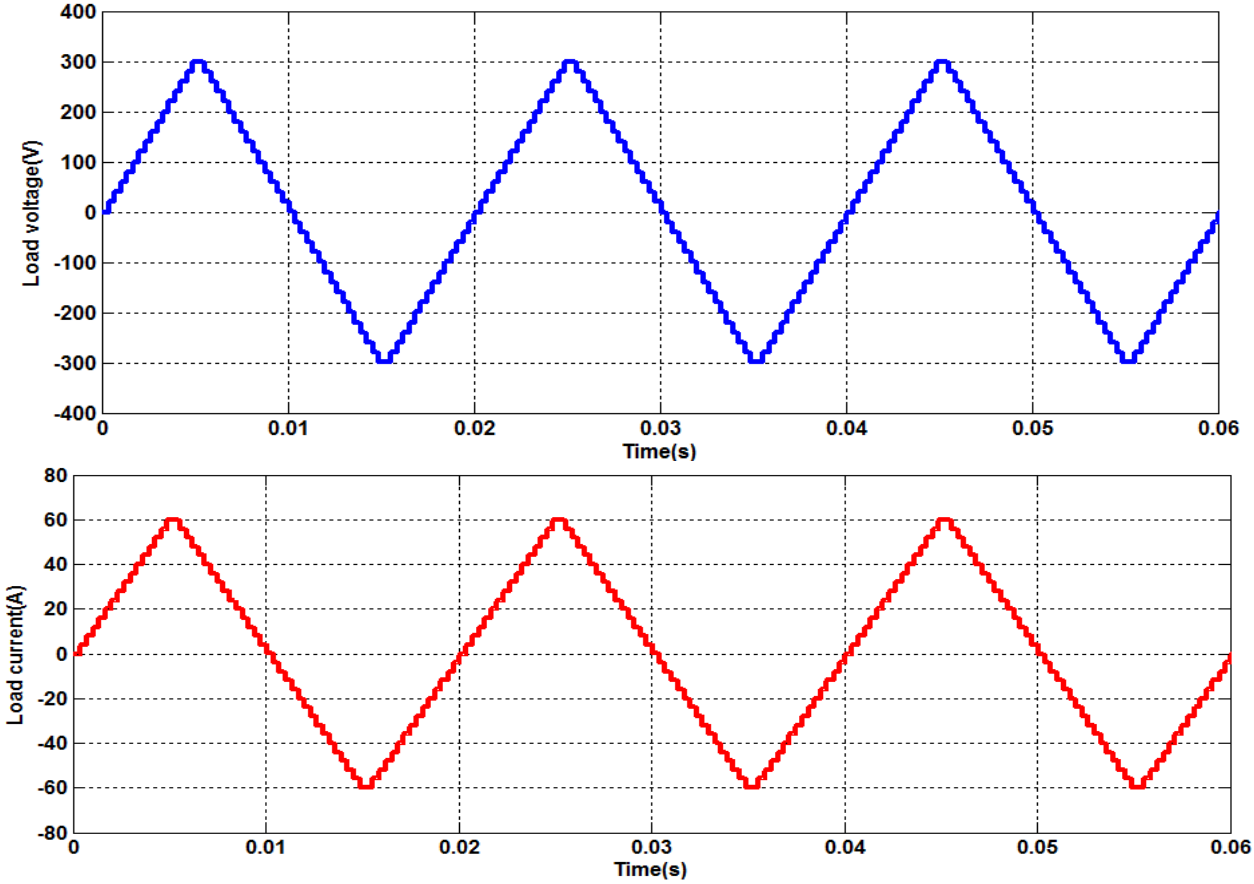

Fig.12. Output voltage current for Thirty-one level R-load

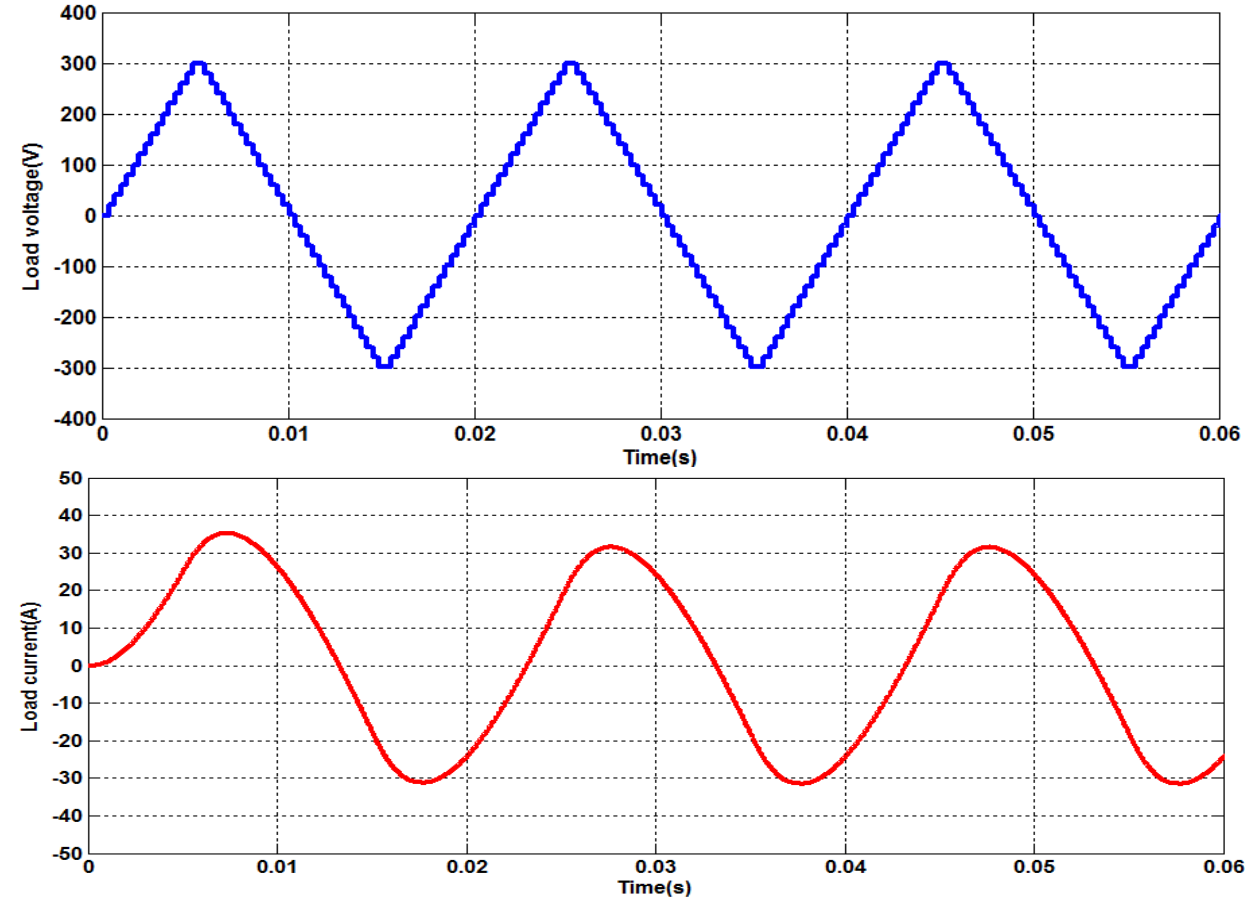

Fig.13. Output voltage current for Thirty-one level RL-load

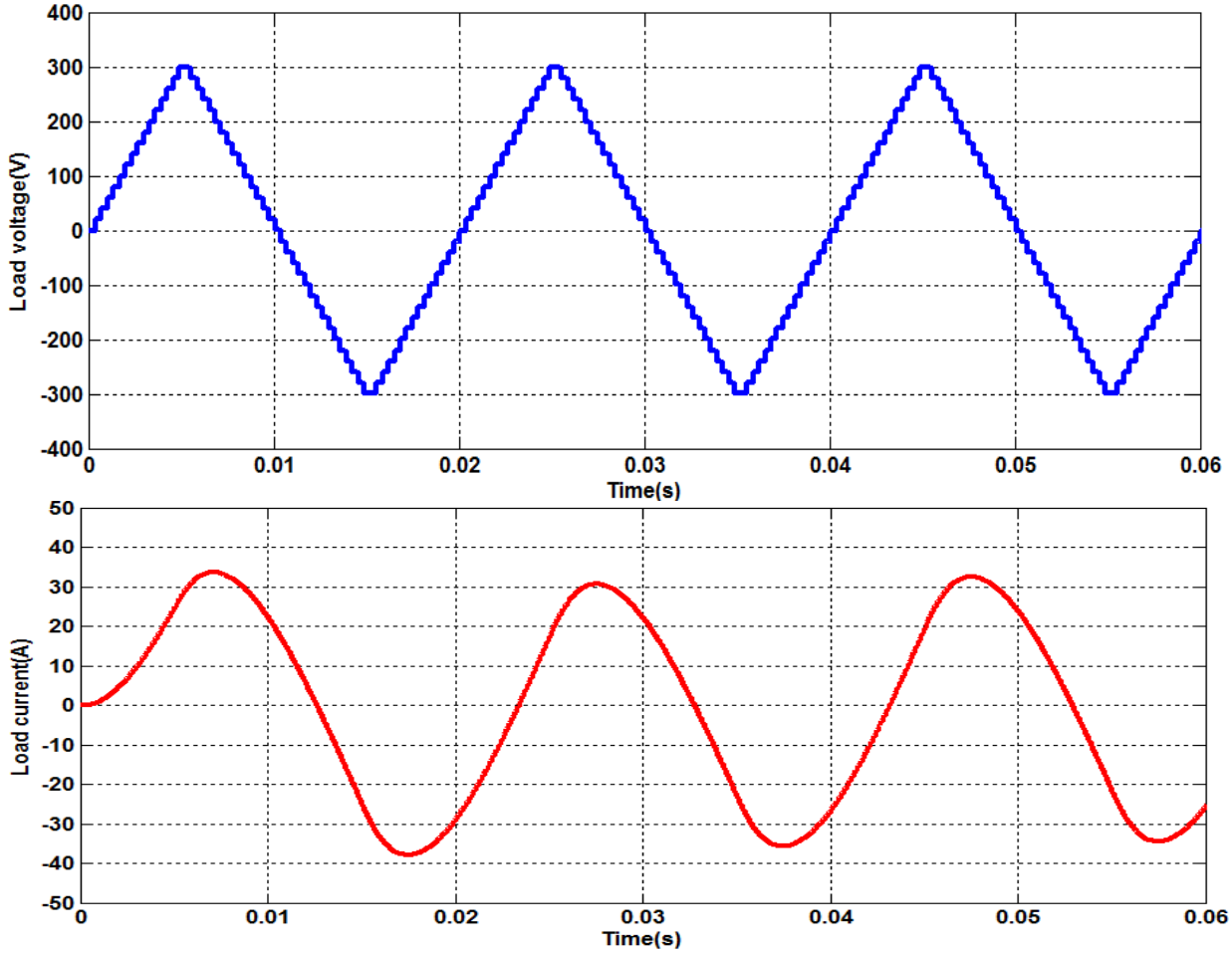

Fig.14. Output voltage current for Thirty-one level RLC-load

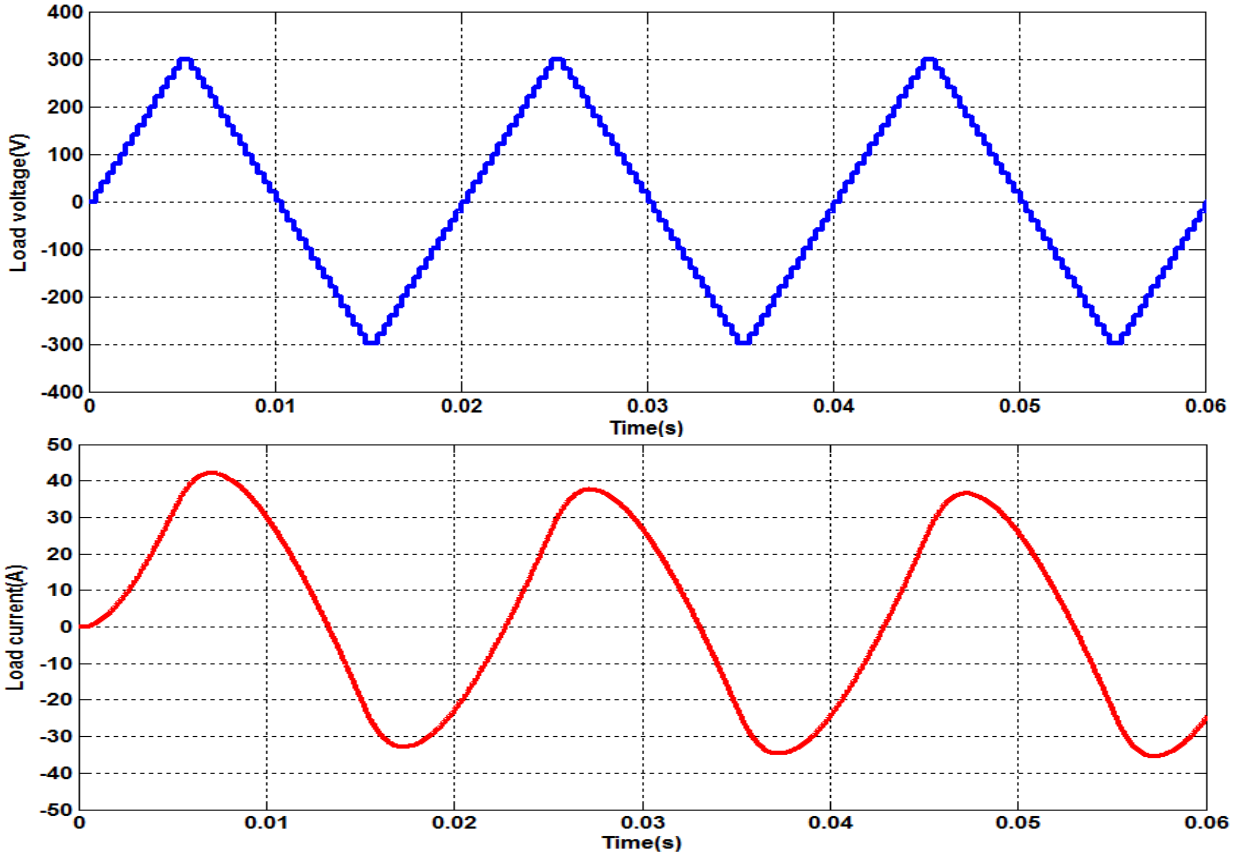

Fig.15. Output voltage current for Thirty-one level Motor-load

Harmonic Analysis multilevel PUC Inverter at different Levels

The following graphs shows the THD comparisons for 7, 15 and 31 levels at various loads are analyzed and which is as shown in the graphical representation for each level. Hence by increasing the levels the THD percentage reduces which is as shown in the graphs Fig 16-18.

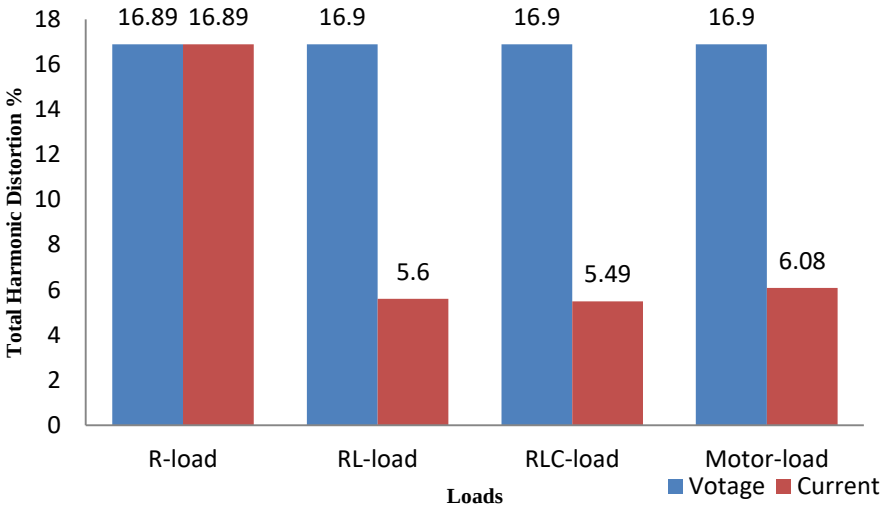

Fig.16. Graph shows the THD for 7-level at variable loads

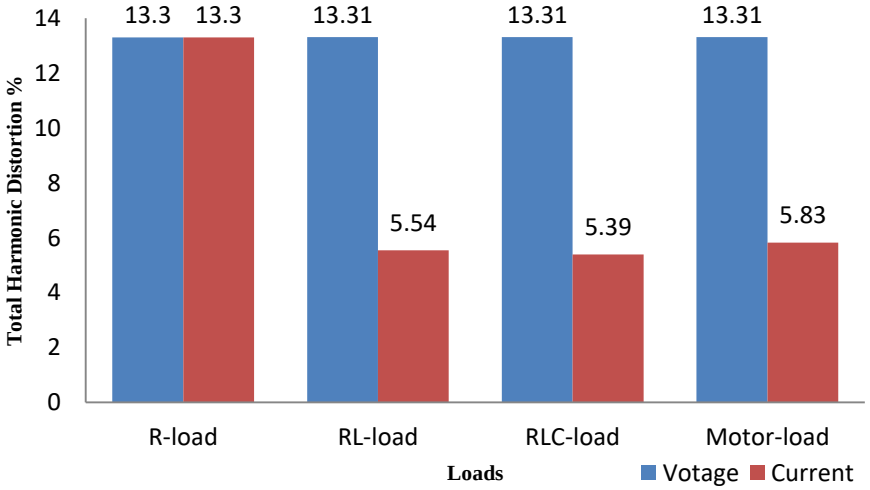

Fig.17. Graph shows the THD for 15-level at variable loads

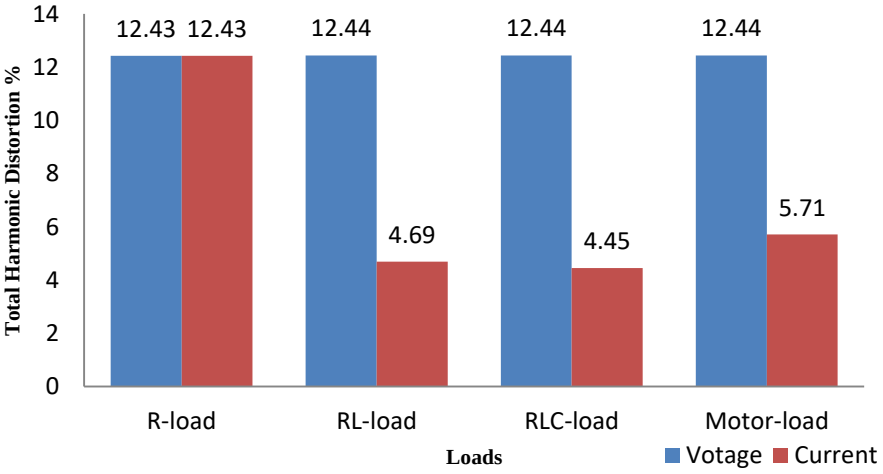

Fig.18. Graph shows the THD for 31-level at variable loads

Table-4 Comparison for Various Loads and Levels in terms of THD%

Variable Loads	Total Harmonic Distortion %					
	7-level		15-level		31-level	
	V	I	V	I	V	I
R	16.89	16.89	13.30	13.30	12.43	12.43
RL	16.90	5.60	13.31	5.54	12.44	4.69
RLC	16.90	5.49	13.31	5.39	12.44	4.45
MOTOR	16.90	6.08	13.31	5.83	12.44	5.71

CONCLUSION

The simulation of PUC (Packed U Cell) topology is performed for 7,15,31 levels at variable loads of R, RL, RLC & Motor using MATLAB/SIMULINK software. When the load is resistive, the %THD for 7,15,31 levels of output voltages are found to be 16.89%,13.30%,12.43%. In the cases of RL, RLC & Motor loads the %THD found be same at each load 16.90%,13.31%,12.44% respectively for output voltage and also for output current they are found to be 5.60%,5.54%,4.69% at RL-load, 5.49%,5.39%,4.45% at RLC-load, and 6.08%,5.83%,5.71% at Motor load respectively Table 4. The FFT analysis of each load case is fulfilled through graphical representation. It is evident that as the output voltage levels increases the %THD gets reduced. The figure of merit of this topology is reduction in the number of switches as level increases. Hence, it reduces the cost of implementation besides topology complexity compared to other existing topologies such as Neutral Point Clamping, Flying Capacitor, Cascaded H-Bridge and Hybrid Cascaded H-Bridge.

REFERENCES

[1] A Nabae, I Takahashi and H Akagi, A New Neutral Point Clamped PWM inverter, *IEEE Transactions on Industrial Applications*, **1981**, IA-17 (5), 518-523.

[2] T Meynard and H Foch, Multi-level conversion: High Voltage Choppers and Voltage-Source Inverters, *Power 23rd Annual IEEE Electronics Specialists Conference PESC'92 Record,* Toledo, **1992**, 397-403.

[3] F Z Peng, JS Lai, JW McKeever and J Van Coevering, A Multilevel Voltage-Source Inverter with Separate DC Sources For Static Var Generation, *IEEE Transactions on Industrial Applications*, **1996**, 32 (5), 1130-1138.

[4] A Ajami, M Oskuee, A Mokhberdoran and A Van Den Bossche, Developed Cascaded Multilevel Inverter Topology to Minimise the Number of Circuit Devices and Voltage Stresses of Switches, *IET Power Electronics*, **2014**, 7 (2), 459-466.

[5] M Veenstra and A Rufer, Control of a Hybrid Asymmetric Multi-Level Inverter for Competitive Medium-Voltage Industrial Drives, *IEEE Transactions on Industrial Applications*, **2005**, 41 (2), 655-664.

[6] LG Franquelo, J Rodriguez, JI Leon, S Kouro, R Portillo and MAM Prats, The Age of Multilevel Converters Arrives, *IEEE Industrial Electronics Magazine*, **2008**, 2 (2), 28-39.

[7] LH Tey, PL So and YC Chu, Improvement of Power Quality using Adaptive Shunt Active Filter, *IEEE Transactions on Power Delivery*, **2005**, 20(2), 1558-1568.

[8] ER Ribeiro and I Barbi, Harmonic Voltage Reduction using a Series Active Filter Under Different Load Conditions, *IEEE Transactions on Power Electronics* **2006**, 21(5), 1394-1402.

[9] Y Ounejjar, K Al-Haddad, LA Gregoire, Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation, *IEEE Transactions on Industrial Electronics*, **2011**, 58(4), 1294-1306.

[10] Ahmed Sheir, Mohamed Orabi, Mahrous E Ahmed and Atif Iqbal, A High Efficiency Single-Phase Multilevel Packed U Cell Inverter for Photovoltaic Applications, *IEEE 36th International Telecommunications Energy Conference(INTELEC)*, Canada, **2014**, 1-6.

[11] Y Ounejjar, K Al-Haddad,V Hani, An Advanced Photovoltaic System Based On Fifteen-Level PUC Inverter, *IEEE 24th International Symposium on Industrial Electronics*, **2015,** 1056-1061.

[12] Y Ounejjar, K Al-Haddad, Averaged Model OF 31-Level Packed U Cell Converter, *IEEE International Symposium on Industrial Electronics*, **2011,** 1831–1836.