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Implementation of Mux Based Encoder for Time To digital Converters Architecture

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Abstract:

A Time to digital converter is a device for recognizing events and providing a digital representation of the time they occurred. It is a device commonly used to measure a time interval and convert it into digital (binary) output. A Time-to-digital converter (TDC) is similar to an analog-to-digital converter (ADC), except that, instead of quantizing voltage or current, the TDC quantizes time intervals between two rising edges. It is originally developed for nuclear experiments to locate single-shot events, the TDC is now being used in many applications such as laser range finders, space science instruments, physical instruments, phase meters, high energy particle detectors, and measurement devices. Our proposed work is to implement mux based encoder for TIME TO DIGITAL CONVERTER (TDC) with bubble error correction using Xilinx software.

Keywords-- Time to digital converter (TDC), Bubble error correction circuit (BEC), Ring oscillator (RO).

I.   INTRODUCTION

A Time-to-digital converter (TDC) is similar to an analog-to-digital converter (ADC), except that, instead of quantizing voltage or current, the TDC quantizes time intervals between two rising edges. It is originally developed for nuclear experiments to locate single-shot events , the TDC is now being used in many applications such as laser range finders, space science instruments, physical instruments, phase meters, high energy particle detectors, and digital storage oscilloscopes and measurement devices. Recently, it has been employed to measure phase in all-digital phase-locked loops (PLLs). Precise measurements of time interval are performed with the use of various methods in both the analog and digital domains. The digital methods become dominant due to ease of implementation in integrated circuits, shorter conversion time, and higher immunity to external disturbances. First, the physical quantity is converted to a time signal and then digitized by a time-to digital converter (TDC) to get the corresponding digital output. TDC architectures suffer from various errors such as quantization error, nonlinearity error, offset error, threshold error, bubble error etc. Error correction techniques can be implemented for better performance of time to digital converter. Time-to-digital converters (TDCs) have been widely used as a fundamental circuit block in all-digital phase-locked-loops (ADPLLs). Since TDC is an analog-to-digital converter (ADC) that receives input in the time domain and converts it to digital domain. The TDC used here is of flash type architecture
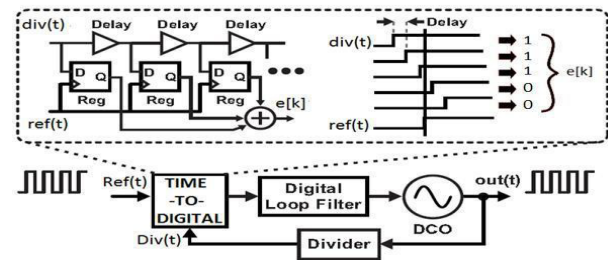

Figure 1: TDC in All-Digital Phase- Locked Loop

Modern VLSI technology is mainly driven by digital circuits. The reasons for this are the many advantages of digital compared to analog circuits: Atomic digital functions can be realized by very small and simple circuits. This results in a compact and cheap implementation of elementary logic functions and enables complex and flexible signal processing systems. A comparable complexity was not feasible with an analog implementation due to area and power consumption but also due to variability and signal integrity. Flexible means reconfigurable, adjustable or even programmable. Data can be stored easily in digital systems without any loss of information. The design of digital circuits is highly automated resulting in high design efficiency and productivity. However, the main advantage of digital signal processing is the inherent robustness of digital signals against any disturbances, i.e. noise and coupling, as well as the inherent robustness of digital circuits against process variations. It is true that these are critical issues especially for large chips fabricated in ultra deep sub-micron technologies. But compared to analog realizations digital solutions are still by far more robust.

II. BASIC THEORY OF TIME-TO-DIGITAL CONVERTERS:

The basic idea of time-to-digital converters (TDC) is to measure time difference with delay elements and to generates the digital words with respect to time difference. The concept of TDC is to sample the outputs of all delay elements at the same time. The basic operation of a TDC by discussing the shape of a TDC input and output characteristic will be explained.
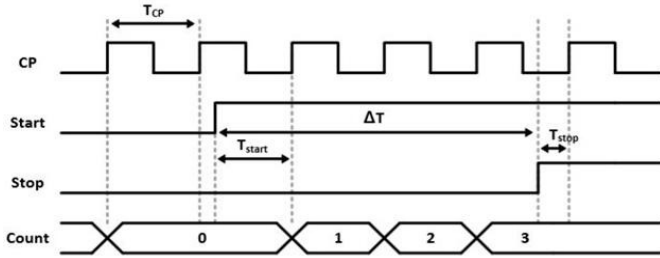

Figure 2 : Principle of counter based TDC

The strategy to provide TDCs as generic mixed-signal building blocks for various applications raises questions about the suitability in ultimately scaled CMOS technologies. Obviously this does not hold for any analog TDC which converts time domain information first into the analog and then to the digital domain. Such TDCs consist mainly of an ADC so have all the impairments of analog circuits in deep sub-micron technologies. The advantages of the time domain can be exploited only if there is no analog conversion step in the time-to- digital conversion. Only if the TDC is clearly dominated by digital circuitry the scaling and robustness arguments hold. The simplest technique to quantize a time interval is to count the cycles of a reference clock fitting into the respective measurement interval. As shown in Figure 2, the measurement interval defined by the lead and lag signal is completely asynchronous to the reference clock signal. This causes a

measurement error ÄTlead at the beginning and ÄT lag at the end of the time interval. The measurement interval ÄT can be expressed as

$$ÄT = N×TCP + (TCPÄTlag) − (TCPÄTlead)$$
$$= N × TCP + åT \qquad \text{....(1)}$$
$$ÄTlead \in [0;TCP]$$
$$ÄTlag \in [0;TCP]$$
$$åT = ÄTlead − ÄTlag \in [TCP;TCP] \text{ ....(2)}$$

Where N is the counter value and TCP the reference clock period. ÄT lead and ÄT lag are the time intervals between the start and stop signal, respectively, and the next rising edge of the clock signal. The quantization error of the ÄT measurement is –TCP and +TCP is limited to twice the period of the clock signal. The measurement accuracy can be increased by a higher clock frequency, however, the higher clock frequency the higher power consumption for the generation and the

processing of the clock signal.

III . BUBBLE ERROR CORRECTION FOR TIME TO DIGITAL CONVERTERS

As a result of development of storage system, optical communication, and ultra-wideband communication, the demand for high-speed analog to digital converter (ADC) [1] has being increased. Among different ADC architectures, flash ADC offers the highest sampling rate with low resolution. Until now, flash ADC is the only architecture satisfying the high sampling rate requirement of those areas. ADC is a mixed signal device that converts analog signal to digital. Performance of ADC is affected due to some invalid transitions in the input thermometer code known as Bubble error – there are one or some logical 1 above sequence of logical 0 in the thermometer code . Bubble error can also affect the output of TDC. Different source of bubble error are meta stability error, device mismatch , offset voltage , clock jitter , cross talk, uncertainty in sampling instant etc. Thermometer to binary encoder is vital component of time to digital converter (TDC). Bubble error can also appear in the thermometer code, which is output of TDC. To improve the performance of TDC, three methods that encode thermometer code to binary code is implemented. Wallace tree encoder, fat-tree method, and MUX-based method. By implementing we can eliminate first, second and third order bubble error in the thermometer code.

MUX-BASED ENCODER :

MUX-based TM2B encoder has many advantages such as low power consumption, low circuit complexity, etc [2],[3]. In previous researches, however BEC circuit remove first-order bubble error only, but the proposed circuit removed bubble error up to third order.
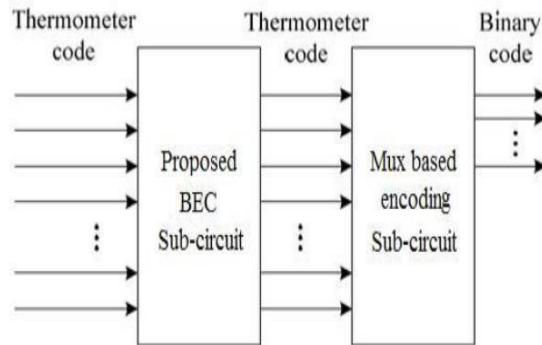

Figure 3 : Proposed MUX-based TM2B Encoder with BEC sub circuit.

In this research, we propose a MUX-based TM2B encoder that can correct bubble error up to third-order. The structure of our

proposed circuit is shown in figure 3. A new sub-circuit is added before the MUX-based encoding sub circuit. The new circuit remove bubble error in the thermometer code .

The circuit is implemented using simple 2-input OR gates. As shown in the figure 4, a circuit with $2n-1$ inputs requires $2n-2$ 2-intput OR gates.
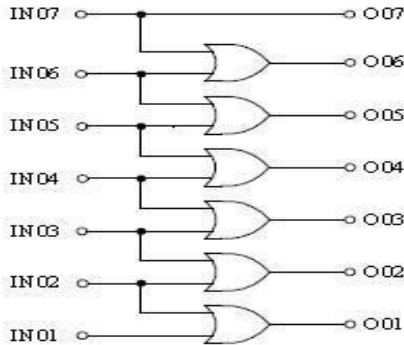

Figure 4 : A 7-to-3 MUX-based TM2B Encoder for first order BEC

The proposed BEC circuit can correct single bubble error, i.e. only one input is invalid between two valid inputs. If there are more than one bubble errors, the output of proposed circuit are still incorrect. This circuit clear only first order bubble error in the input thermometer code. If the order of error increases then output of this circuit remains incorrect. Previous research proposed first order BEC circuit for multiplexer based encoder. For first-order bubble error, BEC circuit implement by 2-input OR gate and for second/third-order bubble error, BEC circuit implement by 3-input OR gate. Here we propose a circuit which can eliminate up to-third-order bubble error correction scheme for the same. The circuit is implemented by using simple BUFFER and OR gates
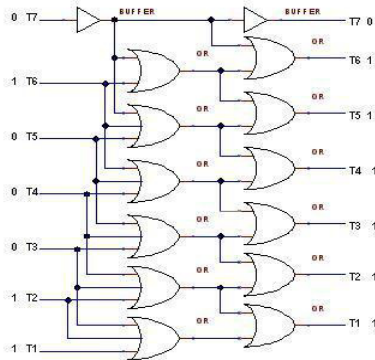

Figure 5 : A 7-to-3 MUX-based TM2Bencoder for third order BEC.

Table I illustrates output of proposed scheme. Column T1, T2 & T3 shows input thermometer code with first order, second order & third order bubble error respectively.

Input thermometer code With bubble error			Output of proposed Scheme (corrected thermometer code)		
T1	T2	T3	T1	T2	T3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
1	0	0	1	1	1
0	0	0	1	1	1
1	1	1	1	1	1
1	1	1	1	1	1

TABLE I : OUTPUT OF PROPOSED SCHEME

It can be observed from the table that proposed circuit can correct error in the code up to third-order. Then by implementing the MUX based encoder we can convert the thermometer code to binary code.

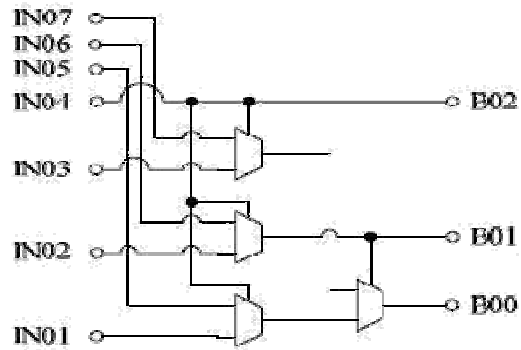Mux-based TM2B encoder converts thermometer code to binary code directly as shown in figure 6.

Figure 6: A 7-to-3 MUX-based TM2B Encoder

Simple algorithm behind MUX based decoder is presented here [3]. The multiplexer-based encoder can be found by observing that the most significant bit (MSB) of the encoder output is equal to the middle digit in the thermometer code. The MSB-1 bit is found from the chosen scale in the same way as MSB was found. We select lower half if the 2N-1 (middle digit) is zero, otherwise the upper half. This is continued recursively until all output bits are found. The algorithm is illustrated by the figure5.

The regular structure of multiplexer based encoder can be easily expanded for higher resolution bits. CMOS logic circuit uses particularly pmos and nmos which passes strong 1 and strong 0 respectively and also degraded zero's and ones's in their respective cases of pmos and nmos so to remove degraded output the nmos and pmos are combined together for strong output level. The CMOS transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission for logic ones.

We implement 2:1 mux by using CMOS Transmission gate as shown in figure 7 .
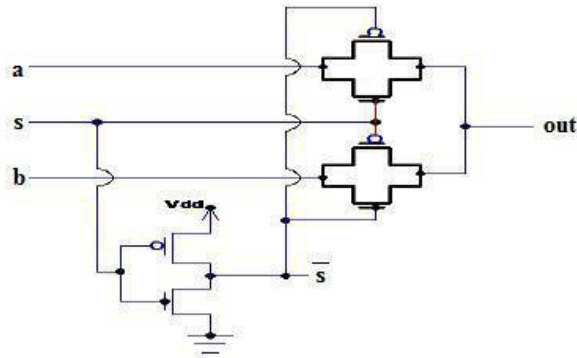
Figure 7 :CMOS Transmission Gate.

CMOS Transmisson Gate has the advantage of being simple & fast , complex gates are implemented with the minimum no. of transistor (the reduced parasitic capacitance results in fast circuits) and better noise margin.

The decoder has a hardware cost-: Total no. of Mux to be implemented for any N-bit Encoder is

$$T_{Mux-decoder} = T_{Mux} \sum_{k=1}^{N-1} 2^{N-k} - 1$$

…..(3)

Where (N= no. of bits)

The critical path in units of tMux is:

$$t_{cp-Mux} = (N-1)\, t_{Mux}$$

…….(4)

By the analysis of various types of encoders, MUX-based encoder has many advantages the proposed circuit requires

lesser number of transistors and consequently consumes less power, which makes the circuit superior to the existing models, no research proposes a Third-order bubble error correction (BEC) circuit. MUX-based encoder circuit complexity slightly rises for the proposed circuit in comparison to other types of BECC's, but this trade-off is acceptable for acquiring higher speed of operation.

IV . VERNIER TYPE RING BASED OSCILLATOR:

1)Basic RO: Unlike the delay-line-based TDCs in which pulses only propagate once per conversion, in RO-based TDCs, [4], [5],[6],[7], the delay line is configured in a ring format such that pulses can propagate inside the delay ring iteratively until the conversion is completed. Fig. 1 shows the concept of such a TDC. A free-running RO, consisting of an odd number of inverters, is used to generate multiple phases at a relative high frequency. The phase from the last stage is fed to a loop counter, which is enabled by the start signal and sequentially disabled by the stop signal. The loop counter records the total

iteration number in the RO during each conversion. The sampling logic, being triggered upon the arrival of both start and stop signals, records the status of each delay stage. The measured time interval *TM*, can be represented as

$$T_M = (SL_{Stop} - SL_{Start}) \times \tau + \frac{CNT_{LC}}{f_{RO}}$$

…..(5)

where SL Start and SL Stop are the outputs of the triggering logic at the arrival time of the start and stop signals, respectively, $\hat{o}$ is the propagation delay of the delay cell, CNTLC is the output of the loop counter, and *f*RO is the oscillation frequency. Theoretically, RO-based TDCs have unlimited dynamic range, but this cannot be accomplished in practice due to the available number of bits of the loop counter and limitations in the counting rate. TDCs using RO topology usually have a time resolution limited by the propagation delay of the inverter. For example, the TDC in [80] implemented in the 90-nm CMOS technology had a resolution of 13.6 ps. Another disadvantage of a basic RO-based TDC is its high power consumption because the RO is working in free-running mode, e.g., 24 mW in [4].
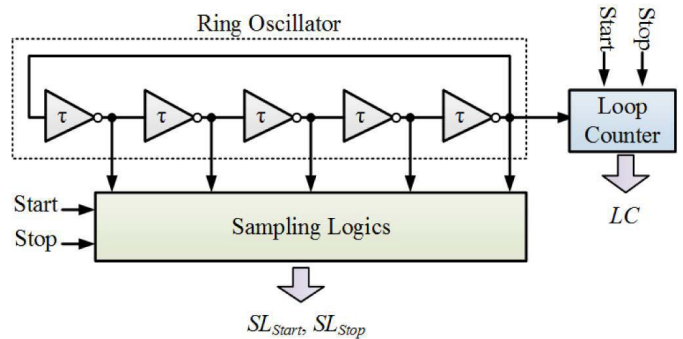

Figure 8: Diagram of basic RO-based TDC.

2)Vernier RO: An alternative technique to obtain high resolution is to adopt the Vernier scheme. Fig. 5 shows the diagram of a Vernier RO TDC. The propagation delays of elements in the slow RO and the fast RO are $\hat{o}1$ and $\hat{o}2$, respectively. With two ROs operating in the Vernier manner, the resolution is determined by the delay differences ($\hat{o}1-\hat{o}2$). Setting $\hat{o}1$ close to $\hat{o}2$, we can obtain arbitrarily fine resolution. A resolution of 3.2 ps was reported in [8]. The dynamic range of the Vernier RO-based TDC is determined by the number of delay stages in the RO and the total number of bits of the loop counter if one is deployed to record the circulation loop of the RO. However, the penalty for improved resolution is a degradation of the counting rate, which limits its applications

required for large dynamic range or high speed. In addition, the nonlinearity worsens because more stages and circulations in the ROs are needed to perform one conversion. In addition, noise and jitter from both internal and external sources are accumulated and eventually result in worse linearity.

Figure 9 : Vernier RO topology.

SIMULATION RESULT:

All the simulations have been performed using Xilinx ISE with Verilog design methodology. Simulation result shown in Figure 10(a), figure 10(b), figure 10(c), figure 10(d).

Figure 10(a)

Figure 10(b)

Figure 10(c)

Figure 10(d)

POWER ANALYZER RESULT FOR VERNIER RO:

A	B	C	D	E	F	G	H	I	J	K
Device			On-Chip	Power (W)	Used	Available	Utilization (%)		Supply	Summary
Family	Spartan3		Logic	0.000	17	1536	1		Source	Voltage
Part	xc3s50		Signals	0.000	32	--	--		Vccint	1.200
Package	pq208		IOs	0.000	20	124	16		Vccaux	2.500
Grade	Commercial		Leakage	0.024					Vcco25	2.500
Process	Typical		Total	0.024						
Speed Grade	-5									Supply Power (W)
					Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)			
Environment			Thermal Properties		37.0	84.1	25.9			
Ambient Temp (C)	25.0									
Use custom TJA?	No									
Custom TJA (C/W)	NA									
Airflow (LFM)	0									
Characterization										
PRODUCTION	v1.2,06-25-09									

CONCLUSION:

The proposed work present Time-to-digital converters using buffers and inverters implemented in Xilinx 12.4 software. Analysis of Vernier type ring oscillator TDC has performed. The output of TDC is thermometer code which can be get affected by bubble error. Hence bubble error correction for thermometer code up to third order is effectively implemented by mux-based encoder circuit. Whereas existing approaches deal with first/second-order bubble errors only, and failed with higher order of bubble errors. The simulation results illustrate that the proposed circuit requires lesser number of transistors and consequently consumes less power, which makes the circuit superior to the existing models. The simulation results gives increased dynamic range in Vernier type ring based oscillator circuit.

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