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An Inventive Design of Multiplier Using 8*8 Bit Reversible NS Gate

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Abstract:

Almost all digital system hardware, multiplier is one of the most important part. so a high speed, reduced area,reduced delay and low power consumption multiplier design will results in effective digital system design. The conventional gates AND,OR,EXOR are not reversible. Here the 8*8 reversible gate designs called NSG. The purpose of NS Gate is to implement in all logical Boolean operations.Reversible gates that carry out reversible logic synthesis are Feynman gate, Toffoli gate, fredkin gate, peres gate etc., and some other reversible gates. By using the reversible NS gate we make a multiplier that gives very efficient output.

Keywords- **Reversible Logic circuit; Reversible Logic Gate; Constant Input; Garbage Output; Low-Power VLSI etc.**

I.INTRODUCTION

Power and speed is an important term in low power VLSI circuit design. The classical digital approach has been worn the digital logic gates, which are irreversible in behavior. Recently, Reversible logic has great attentiveness due to their ability to reduce the power dissipation. Power dissipation is the major necessity in low power VLSI design. It has several applications in DNA computing, quantum computation,nanotechnology, low power CMOS and Optical information processing. Irreversible hardware computation outcome in energy dissipation due to loss in information.

A circuit is said to be reversible if the input vector can be uniquely get back from the output vector and there is a one-to-one similarity between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be get back from the outputs. Energy dissipation can be decreased or even eliminated if computation becomes Information-lossless.

Energy loss is a very main factor in modern VLSI design. Irreversible hardware computation outcome in energy dissipation due to information loss. J R.Landauer has shown that for irreversible logic computations, every bit of information lost produced KTln2 joules of heat energy, where K is Boltzmann's constant and T is the temperature at which computation performed. Reversible logic circuit doesn't have loss of information and reversible computation in a system can be executed only when the system exist of reversible gates. Reversible logic is more crucial for the construction of low power, low loss computational designs which are crucial for the design process of arithmetic circuits utilized in quantum computation, Nanotechnology and other low power digital circuits.

In Proposed system, there consists a design of multiplier and adder units by number of reversible

gates. In this design, we are using only one reversible gate called NSG gate. By utilizing this NS gate number of operations will be performed by only single gate and the garbage outputs also minimized. In this paper, we are proposed an 8-bit Multiplier unit. Multiplier unit is an inevitable part in many digital signal processing (DSP) applications involving multiplications. Multiplier unit is worn for high performance digital signal processing systems. The DSP applications comprises of filtering, convolution and inner products. Most of digital signal processing methods worn nonlinear functions such as Discrete cosine transform (DCT) or Discrete wavelet transforms (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic regulate the execution speed and performance of the whole calculation. The adder unit and multiplier will be outlined by NSG gate. The simulation output is verified using Xilinx ISE 14.5.

II.EXISTED SYSTEM

Most important arithmetic operation performed almost in all digital signal processors and systems is multiplication operation. Multiplication is involved in all digital signal and data processing. Thus performance of a system completely depends upon the performance of its multiplier unit. The speed, power consumption and area of a multiplier define performance of a system. This paper presents multiplication algorithm which is suitable for low power, low delay and high performance applications. Multipliers are utilized to implement any operation because these are fast, reliable and efficient components. These are of number of types and depending upon the application a specific type of multiplier is chosen. In a simple way multiplication is a process of adding an integer called as multiplicand to itself a number of times specified by another integer called as multiplier. Also multiplication is considered as a process of add and shift operations. But in case of digital systems multiplication has three basic concepts:

l. Generation of partial product arrays.

2. Reduction of partial product array.

3. Final Addition

To generate partial products at first stage n shifted copies of multiplicand are generated and then added according to the bits of multiplier. AND gate logic can be used at this stage. At second stage of partial product reduction mainly addition is done to perform reduction and this stage results into the optimization of design in terms of area, power and delays. It depends upon the type of technique used to perform reduction. Generally a compressor circuit is used for reduction. And final addition is done by using an efficient carry propagate adder.

Two Bit Vedic Multiplier Algorithm:

Using similar process of multiplication 2 bit binary multiplication can be performed in few numbers of steps.

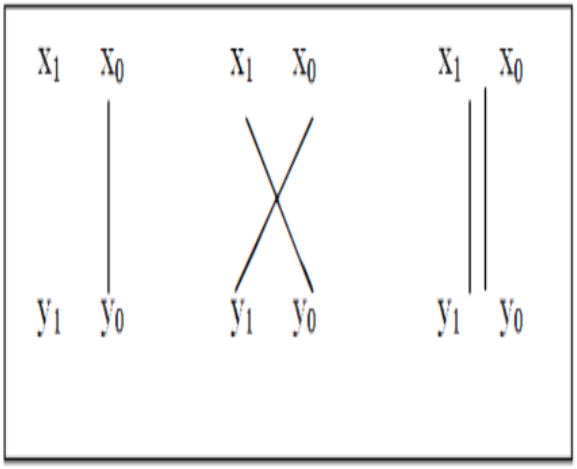

Fig. 1: Two Bit Multiplication using Vedic Methodology

Here two 2 bit binary numbers $X = X_1X_0$ and $Y = Y_1Y_0$ are multiplied using vertical and cross technique. X_0 , Y_0 are multiplied and generate LSB bit of result. Then cross multiplication of X_0 Y_1 and

X_1 Y_0 is performed and product terms are added also carry of previous stage is added to this and thus generate next bit of result. At final stage X_1 Y_1 are multiplied vertically and added with carry of previous stage and then addition is taken as MSB bits of the result. A simple architecture to perform this 2 bit multiplication can be given as shown in Fig. 2:

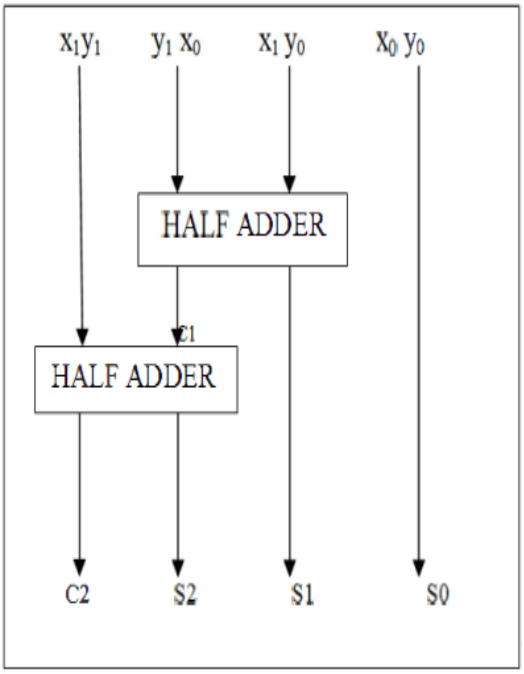

Fig. 2: Two Bit Multiplication Architecture

As seen in Fig. 2 only an AND gate logic and half adder circuitry is sufficient to perform the multiplication operation so it is clear that this methodology is very much effective in optimizing the area, delays and thus power consumption of VLSI design which is of most concern in designing.

III.PROPOSED SYSTEM

The reversible adder circuits proposed till now, NS gate is better than the previous full-adders design. The proposed full adder using NS Gate requires only one reversible gate (one NS Gate) and the NS Gate produces only 2 garbage outputs while performing operations like full adder, full subtractor, half adder and half subtractor. The proposed NS Gate can also singly perform the function of a full subtractor, half adder and half subtractor with only two garbage outputs now we design a multiplier.

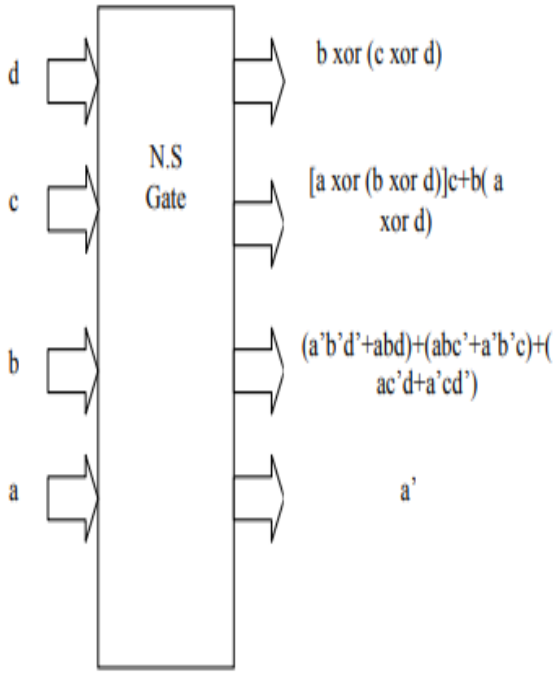

Fig 3. Proposed Reversible NS Gate

Reversible NS Multiplier:

Multiplier unit consists of a multiplier, adder and register. In this paper, 8 bit modified Reversible NS multiplier has been used. The inputs of the Multiplier are obtained from the memory location and it will be given to the multiplier block. This will be very useful in the digital signal processor of the 8 bit. The input which is being fed from the memory location is 8 bit. Since the bits are vast and also ripple carry adder produces all the output values in parallel, PIPO register is used where the input bits are taken in parallel and output is taken in parallel. The

register is taken out or fed back as one of the input to the ripple carry adder. The figure 4 shows the 8X8 NS multiplier.

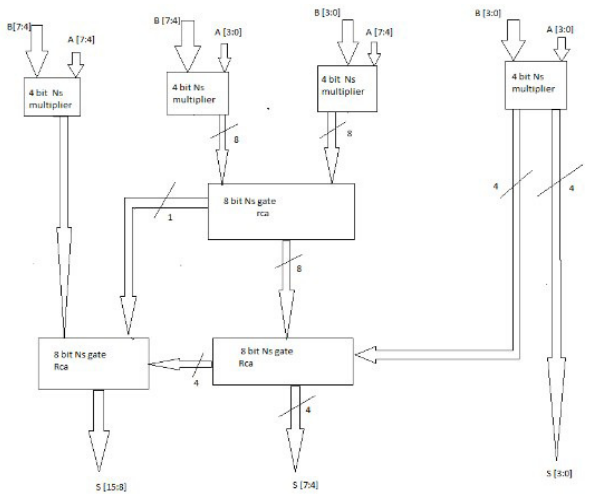

Fig 4. 8X8 NS Multiplier

IV.RESULTS

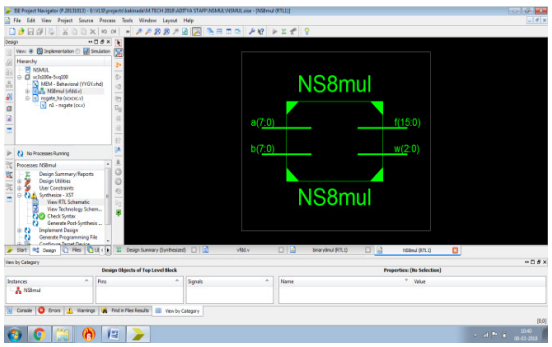

Fig 5. RTL Schematic

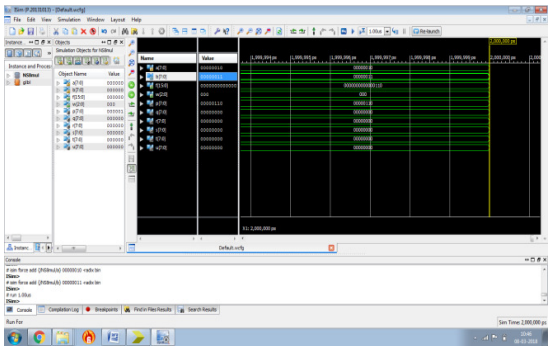

Fig 6. Output Waveform

V.CONCLUSION

Reversible multiplier can be designed with the various logical designs in conventional combinational and sequential logic. Number of gates, Number of ancillary inputs, Number of garbage outputs, is to be efficient for improving the performance of the reversible logic multiplier. Finally, these reversible logic gates are occupied less area and delay because it has a many to many input and output relations. Therefore, by utilizing of these gates we can design any large circuits with fewer components. Hence, it is the main advantage of reversible logic gates.

This paper proposed an approach to realize the multipurpose binary reversible gates. Such gates can be used in regular circuits for realizing Boolean functions. In the similar way it is possible for constructing multiple -valued reversible gates which having the similar properties. 8*8 multiplication is realized with reversible NSG gate in an appropriate and enhanced manner. This unique approach multiplier is applicable for multipurpose applications in all domains.

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