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CONVOLUTION CODE FOR BETTER PERFORMANCE OF ULTRA LOW POWER TRANSCEIVER

S.Sindhu[1], A. Balamurugan [2]

1. *Assistant Professor, Dept. of Electronics, Govt. College Chittur, Palakkad-678104, Kerala, India.*
2. *Assistant Professor, Dept. of Physics, Govt. Arts College, Ooty-643002, Tamil Nadu, India*

Abstract:

This paper proposes, convolution code for better performance of ultra low power transceiver comparing to Hamming code. It targets ultra low power consumption; with reliable Quality of Service (QoS). Low complex architecture is provided here with Application Specific Integrated Circuit (ASIC) which satisfies a good performance. Better packet synchronization and data recovery is helpful for the satisfactory functioning of the ultra low power transceiver. With a 1.1V supply and 4MHz system clock the base band transceiver can decrease the power up to 7mW.

Keywords — **Wireless Body Area Network (WBAN), Transceiver, Convolution code, Power consumption.**

I. INTRODUCTION

Wireless Body Area Networks (WBANs) provide efficient communication solutions to the healthcare systems. This provides better medical care to the people [1-2]. Many patient get benefits from continuous monitoring of their diagnostic procedures by this WBAN.

By integrating bio- sensors with mobile phones it is possible to monitor an individual's health and related behaviour. The tracking capability of such a system should also be able to provide optimal maintenance after surgical procedure and support early detection of abnormal health conditions [3]. The recent advances in the integrated circuits, sensor circuits and wireless communication technology are paving the way for developing miniature, low weight, ultralow power physiological healthcare surveillance and monitoring devices for the improvement of human lives. These devices are integrated into Wireless Body Area Networks (WBANs) for health caring and monitoring [4].

Development in wireless sensor network technologies have realized new opportunities to form WBAN for pervasive remote monitoring of the patients' vital signs at hospital and remote homecare environment, thereby improving healthcare system.

The wireless physiological body sensor node is capable of sensing and processing the vital signals as well as communication to the network coordinator for the transmission of these signals for remote monitoring [4].

A WBAN topology consist of series of different types of sensors and capable to communicate with each other or with the central node. The central node has higher computational capability and communicates with the personal server and subsequently the outside world, through a standard telecommunication infrastructure such as mobile phone network and

wireless networks. The power budget is quite strict for WBAN applications because the wireless devices are powered by a battery [3-5].

For Example, recently developed IC CC2420 from the Texas instruments can cover 20-30 m range at a power usage of 60-70mw [6-8]. However such power consumption and operational range are not a good choice for WBAN, where the transceiver design target is 1-5m operation range and also consumes low power [9-10]. We introduce a transceiver with low-complex architecture with satisfactory performance.

Most of the transceivers are designed of high data rate and high power consumption. We propose a transceiver with low data rate and low power consumption with low complexity architecture. It provides satisfactory performance. The specified data rate of this transceiver is 250kb/s. It can be used for indoor WBAN application and it's working range is1-5m. The Application Specific Integrated Circuit (ASIC) architecture can provide low complex architecture and low power consumption with satisfactory performance [11- 12].

In this paper, a digital baseband IC of low power and low data rate is proposed. The complete system requirement is provided in Table-1. The data rate is 250 kb/s and Signal-to-Noise Ratio (SNR) for 1% is 17dB. By the low complex architecture and optimized hardware implementation, the proposed Application Specific Integrated Circuits (ASIC) can achieve lower power consumption. The base band transceiver is configured with FSK (Frequency Shift Keying) modulator and demodulator. Here Hamming coder can be replaced by a convolution coder. The power is calculated by Xilinx software. The power can be decreased up to 7mw using convolution code comparing to Hamming code.

The proposed WBAN radio transceiver block diagram is given in Fig.1. FSK modulation and demodulation modules are provided for this transceiver. Physical layer architecture is introduced here to reduce the complexity of baseband processing and maintains satisfactory performance. FSK demodulator is used here to reproduce the data. A novel Synchronization and Data Recovery (SDR) is provided to recover the timing and data information from FSK.

Description	**Area/Units/Range**
Working environment	Indoor WBAN Application
Working range	1-5m
Required raw data rate	250kbps
Required SNR for 1%	17dB
Target power consumption	<100µW

TABLE-1

SYSTEM REQUIREMENT OF THE COMPLETE SYSYETM

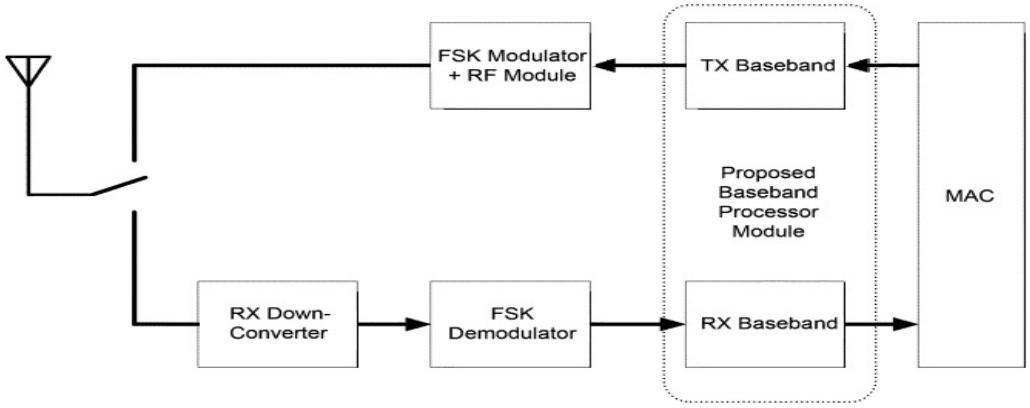

Fig .1: Block diagram of WBAN radio Transceiver

In Fig.2 the MAC (Media Access Control) layer produces the Physical Layer Service Data Unit (PSDU) and processed by the transmitter baseband processor and generates Physical layer Protocol Data Unit (PPDU) packet. The data rate of transmitter (TX) base band processor is 250kb/s.

In the transmitter baseband module, the channel coding and signal processing are performed on the PPDU and produces a raw data at a rate of 250kb/s.

The output from transmitter base band processor is modulated by the FSK and up-converted in to 2.45 GHz.

In the receiver the incoming data is down converted in to 2MHz Intermediate Frequency (IF) signal and demodulated by the FSK low power demodulator. The demodulated signal is processed by the receiver (RX) baseband processor and processed data is sent to the MAC layer as shown in the Fig.1.

II. Block Diagram of Ultra Low Power Transmitter

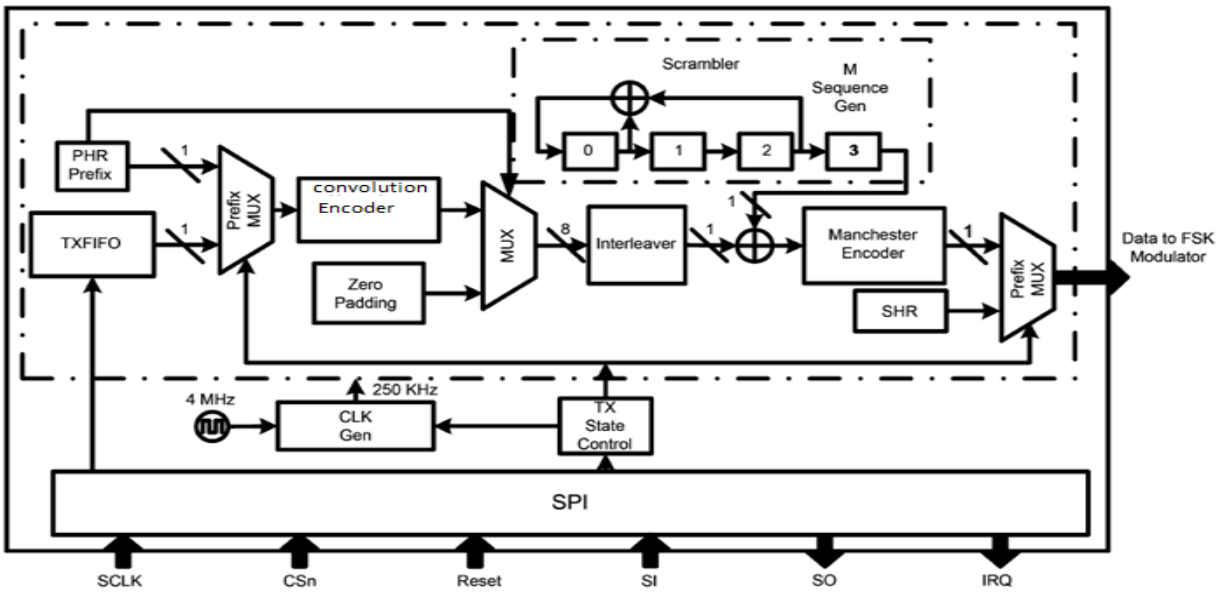

Fig.2: Block diagram of Baseband Transmitter

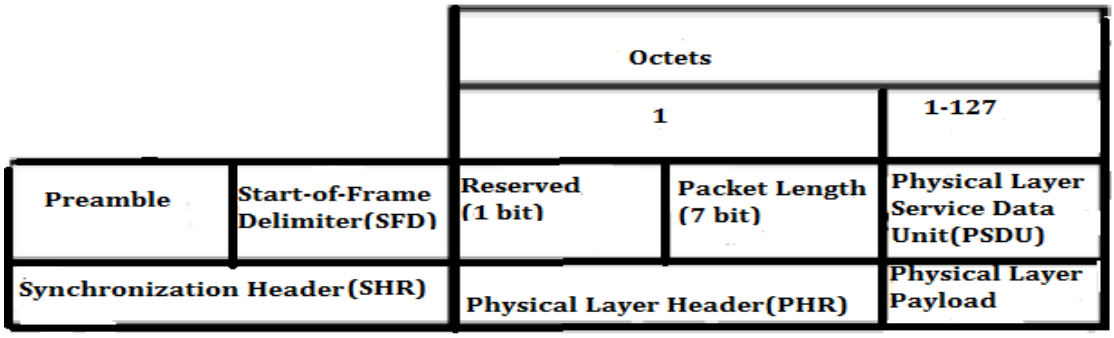

Fig.3: PPDU Packet format

The low complexity PHY (Physical layer) architecture provides low power consumption. The proposed block diagram of Transmitter (TX) is provided in Fig.2. TX module receives the Physical layer service Data Unit (PSDU) from MAC layer and constructs Physical Layer Protocol Data unit (PPDU), which is shown in Fig.3. The length of PSDU is not greater than 127 octets.

When the MAC layer produces the PSDU, feds it in to the TXFIFO (Transmitter First In First Out) register and is ready for transmission. The prefix MUX controlled by the TX state control block select the input to the convolution encoder. When the transmission command is enabled from the MAC layer, PHR (Physical Layer Header) is prefixed to the PSDU and send to the convolution encoder. Convolution encoder receives the input data in serial sequence with 1 bit word length.

Interleaver of matrix 8x4 is used here for Forward Error Correction (FEC) purpose. For each 4 bits of input data convolution encoder generates 8 bits of output data simultaneously. The output from convolution encoder sends to Interleaver, to eliminate long strings of like bits and to eliminate most periodic bit patterns that may produce undesirable frequency components. Interleaved data sends to scrambler.

The scrambler block generates bit of code in serial sequence. Here the output of scrambler is 4 bit and provides a satisfactory performance. The output of Interleaver first sent to scrambler. The interleaver output is XORed with the scrambler output. The XORed data sends to the Manchester encoder.

The Manchester encoder codes bit “0” in to “01” and “1” into “10”. So total number of “0” and ”1” is balanced. Manchester encoder is prefixed with Synchronization Header (SHR) and send to FSK modulation.

A . Convolution encoder

Convolution code is a type of forward error correcting code that generates the parity symbols. Here the input to the convolution encoder is 4 bit and converts it in to 8 bit code. The input data of convolution encoder block is in serial sequence with 1 bit word length. The (8,4) convolution encoder is adopted here as the Forward Error Correction (FEC), which has three parity check bits and one over all parity bit following every four information bits. For each consecutive 4 bits of input data, convolution encoder generated 8 bit code.

B. Interleaver

An interleaver helps to avoid burst error. It helps to avoid long strings of like bits that may impair receiver synchronization and to eliminate periodic bit patterns. That may produce undesirable frequency components. In computer memory; interleaving is a way to arrange data in a non-contiguous way to increase performance. It is typically used in error correction coding, particularly within data transmission, disk storage etc.

C. Scrambler

A scrambler is a device that inverts signals or otherwise encodes a message at the transmitter to make the message unintelligible at a receiver if not equipped with an appropriate descrambling device. Scrambling usually refers to operations carried out in the analog domain.

In telecommunication and recording, a scrambler (also referred as a randomizer) is a device that controls a data stream before transmitting. The scrambler would encode a message at the transmitter to make the message unintelligible at the receiver. If the receiver is not equipped with an appropriate descrambler the data cannot be received correctly. Scrambling is accomplished by the addition of components to the original signal or the changing of some important component of the original signal in order to make extraction of the original signal is difficult.

A scrambler is a device that manipulates a data stream before transmitting. The manipulations are reversed by a descrambler at the receiving side. Scrambling is widely used in satellite, radio relay communications. A scrambler can be an algorithm that converts an input string into a random output string of the same length, thus avoiding long sequences of bits of same value. Scrambler can enable accurate timing recovery on receiver equipment without resorting to redundant line coding. It also known as timing recovery circuit or clock recovery circuit. Scrambler would ensure accurate time recovery on receiver equipment without resorting to redundant line coding.

D. Manchester encoder

Manchester encoding is also known as Phase Encoding (PE). It is used for telecommunication and data storage purposes. It is a line code, in which the coding of each data bit has at least one transition occupies at the same time. Here it converts the bit 0 into"01" and bit 1 into "10". Synchronization Header (SHR) is added with output of Manchester encoder.

III. Block Diagram of Ultra Low Power Receiver

In receiver section as shown in Fig.4, the FSK demodulator demodulates the received data stream. Here D flip flop is used to sample and to restore the analog signal.

If the voltage of input signal is greater than the V_{HL}**(Voltage High to Low)** of the D flip- flop , the output of D flip-flop is "1" . If the voltage of input signal is lower than the V_{LH} **(Voltage Low to High)** of the D flip-flop, the output of D flip –flop is "0". In fig.4, the signals are first serially fed in to the Synchronization and Data Recovery block (SDR).

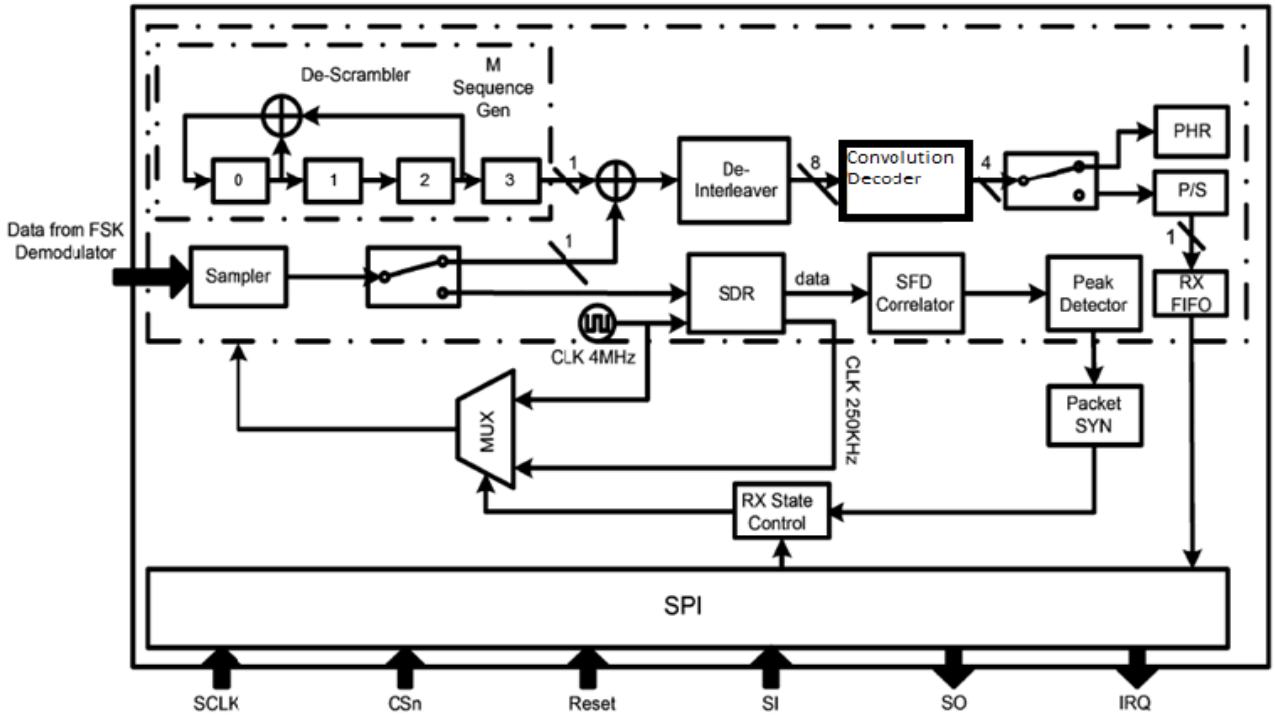

Fig. 4: Block diagram of Baseband RX

The SDR helps for synchronization and to recover the received data. Shift register matrix block in SDR, over-samples the incoming signal and calculates the correlation between the incoming data and the predefined preamble sequence to achieve bit synchronization. This helps to detect continuously the peak of the calculated correlation. Once the peak is detected, Start of Frame Delimiter (SFD) correlator block calculates the correlation between the predefined SFD sequence and the incoming data.

Peak detector helps to detect the peak. Once the peak value is detected, packet Synchronization (SYN) is confirmed. The preamble sequence and SFD is removed. Packet SYN block indicates the RX state control block that the PHR and PSDU is received. 250 KHz is the operating frequency of the receiver base band block.

Manchester decoding is performed on the received PHR and PSDU data stream by detecting the first bit for every two continuous received bits. After that, the incoming data is descrambled. The out of this descrambler is 1 bit word length. XOR operations are performed with the incoming data bit by bit.

FEC receives the PHR and PSDU, FEC includes the de-interleaving and convolution decoder block .The output of de-interleaver is 8 - bit word length and feds to convolution decoder. The convolution decoder checks whether if there is any error in the incoming data and corrects the error.

If the convolution decoder detects the error and if it cannot correct the error, the receiver will stop receiving the data and the MAC layer requests retransmission of the packet. The PHR is decoded first and thus length

of the PSDU can be obtained by the RX state control block.

The output of convolution decoder is 4 bit word length. There is a parallel to serial buffer, so the bits fed in to RXFIFO in serial sequence with1 bit word length and it is read by the MAC layer.

A. *Descrambler*

It helps to avoid the undesirable frequency components and also provides better receiver synchronization. It helps to avoid most string of like bits, that may impair receiver synchronization and to eliminate the most periodic bit patterns. These periodic pulses can produce undesirable frequency components, that can damage the data.

B. *De-interleaver*

It would de-interleave the data at the receiver and can receive the data without Burst Error.

C. *Convolution decoder*

It would convert the encoded 8 bit data in to 4 bit data in the receiver.

IV .Simulation output

A. *Ultra low Power Transmitter output using Hamming encoder*

Fig.5 shows the simulation output of Transmitter using Hamming encoder in Xilinx software. The Power used by the TX is 55mW.

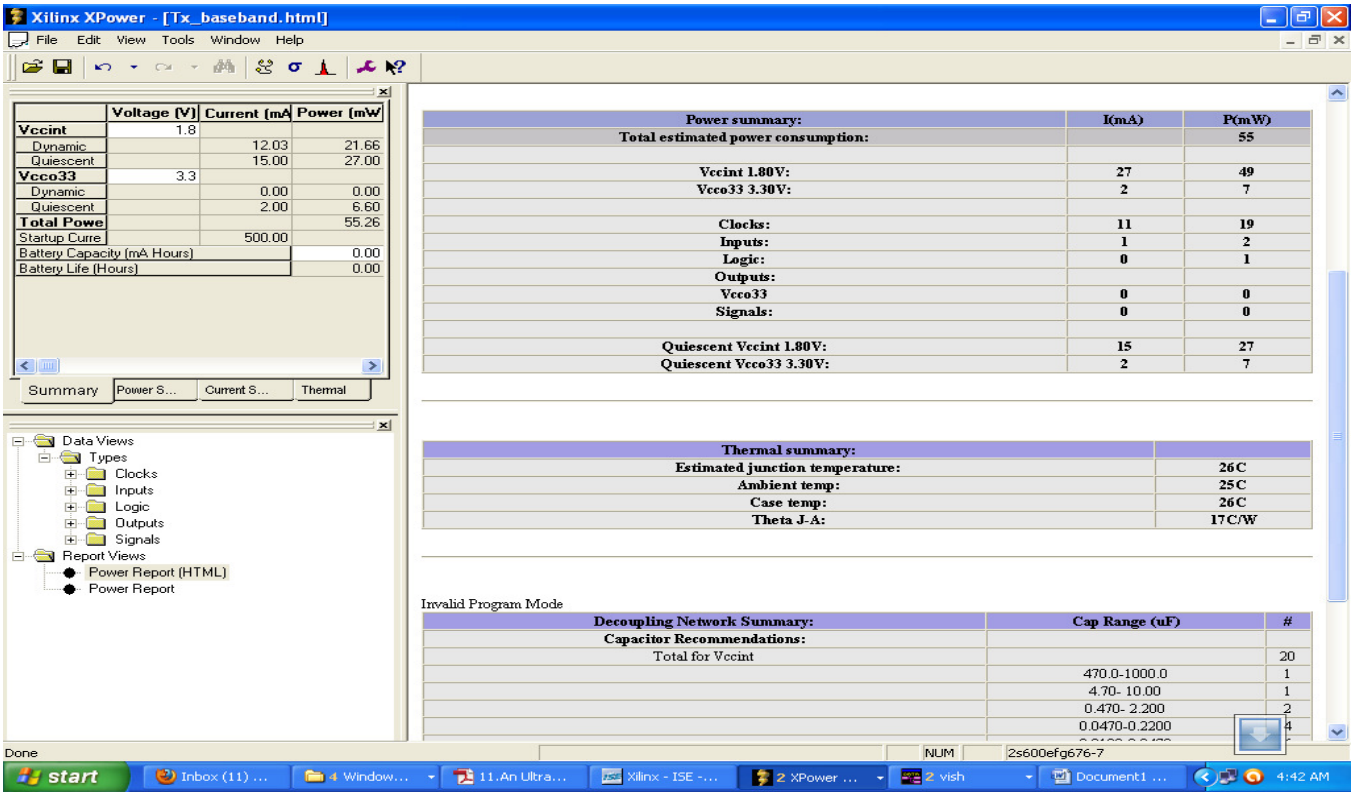

Fig 5: Simulation output of TX using Hamming encoder

B. Ultra low Power Transmitter output using convolution Encoder

Fig.6 shows the simulation output of Transmitter using convolution encoder in Xilinx software. The power used by the TX is 50mW.

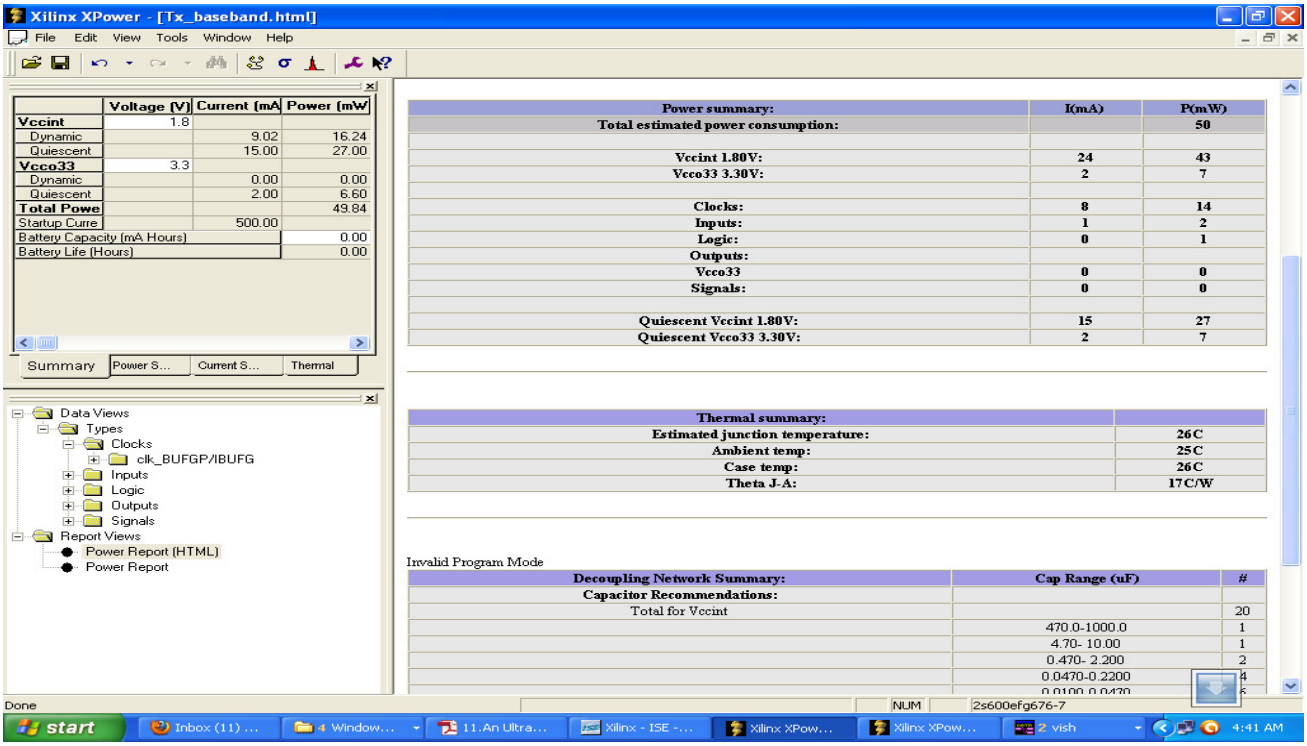

Fig. 6: Simulation output of TX using Convolution encoder

C .Ultra low Power Receiver output using Hamming decoder:

Fig.7 shows the simulation output of Receiver using Hamming decoder in Xilinx software. The Power used by the RX is 57mW.

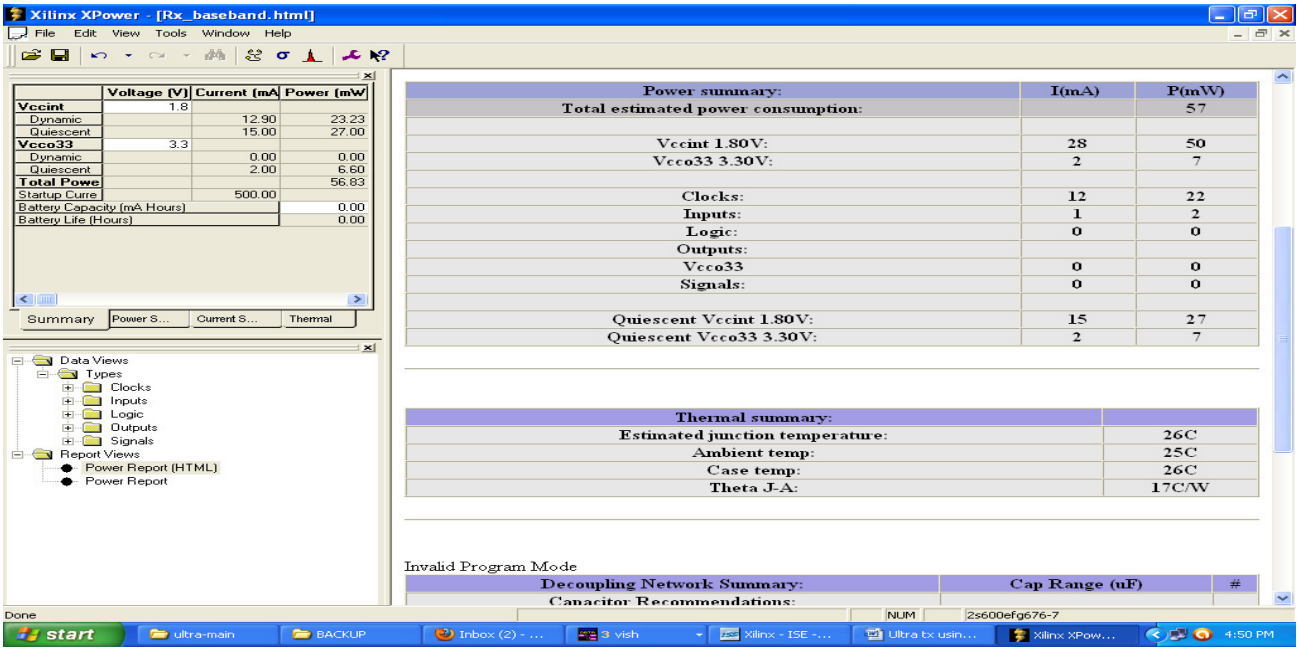

Fig 7: Simulation output of RX using Hamming decoder

D. ***Ultra low Power Receiver output using Convolution Decoder***:

Fig.8 shows the simulation output of Transmitter using convolution decoder in Xilinx software. The Power used by the TX is 55mW.

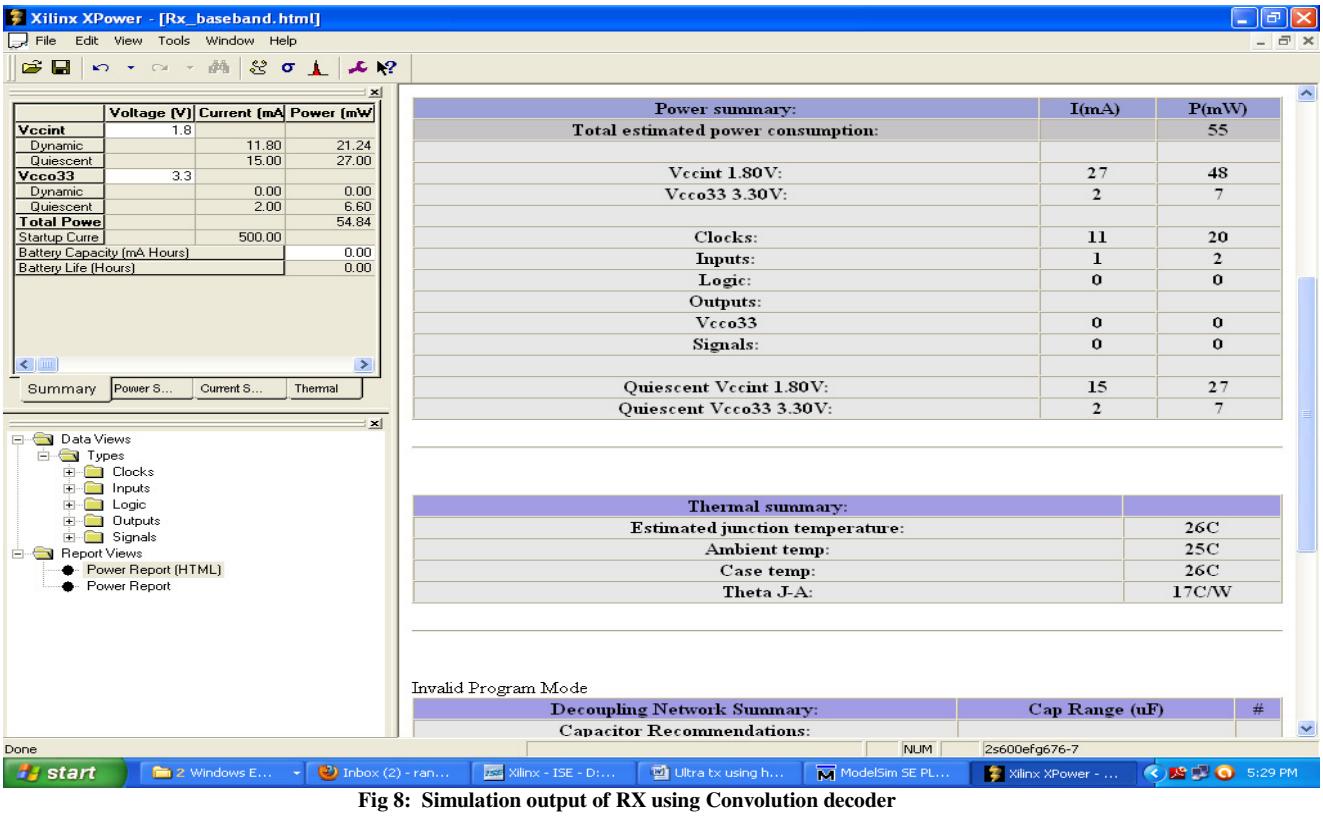

Fig 8: Simulation output of RX using Convolution decoder

E. Transmitter output Waveform using convolution encoder

Fig.9 shows the output waveform of Transmitter using Convolution encoder.

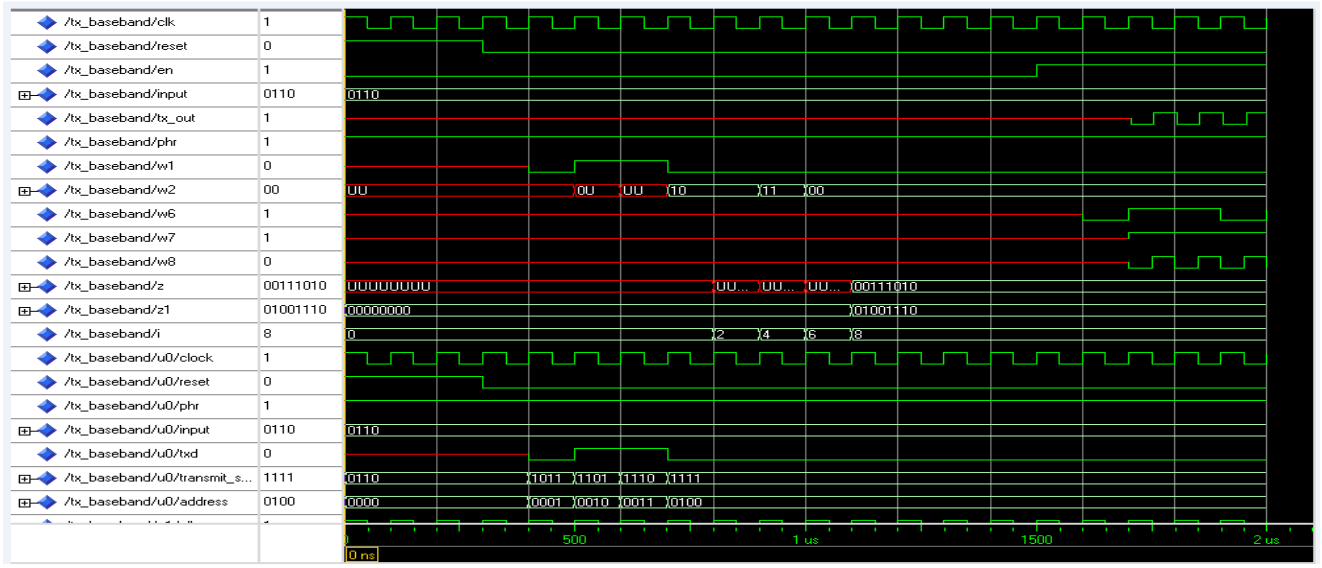

Fig 9: output Wave form of Transmitter using convolution Encoder

F .Receiver output using convolution Decoder

Fig.10: shows the output waveform of Receiver using Convolution encoder

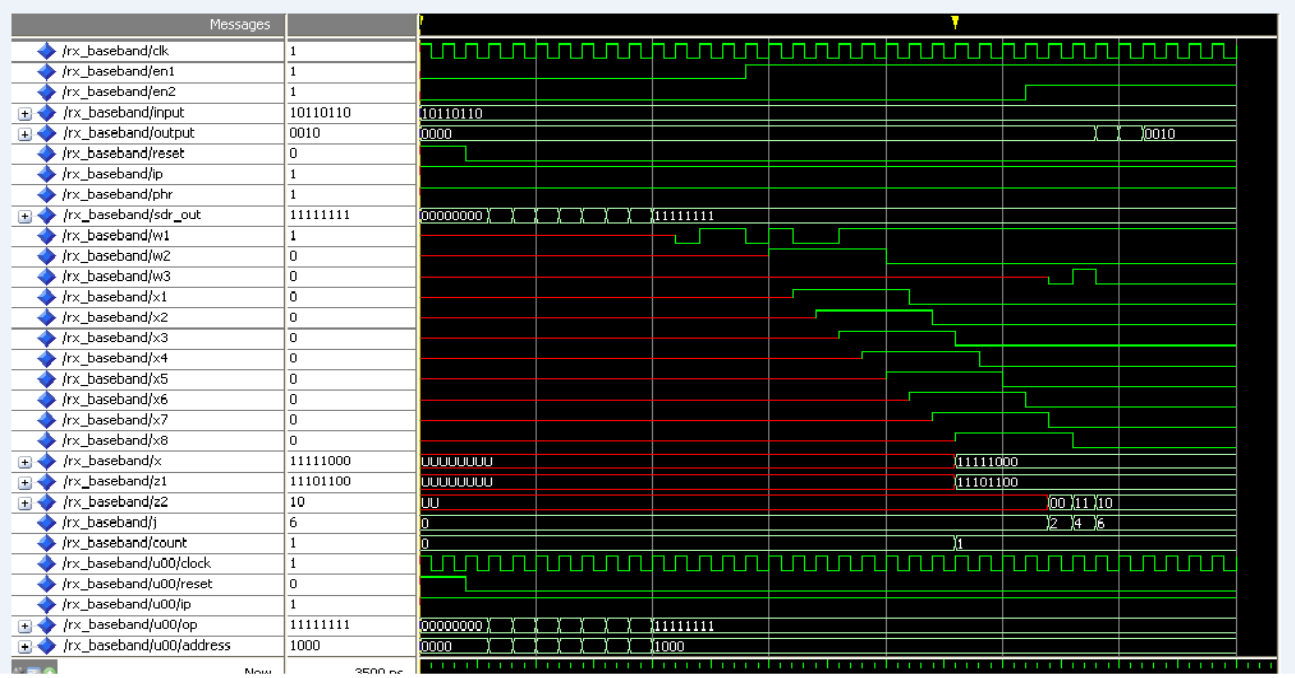

Fig 10: output Wave form of Receiver using convolution Decoder

V. Conclusion

This paper proposes a ultra Low power transceiver with convolution code for better performance comparing to hamming code. ASIC architecture is used here. That consumes low power and uses low complex circuit. This provides a satisfactory performance. This architecture works in 4MHz frequency and can be used for indoor WBAN applications. Comparing to Hamming Code the Power decreases by 7mw using the convolution code.

REFERENCES

[1] Xin Liu, Yuanjin Zheng, Bin Zhao, Yisheng Wang, and Myint Wai Phyu "An Ultra Low Power Baseband Transceiver IC for Wireless Body Area Network in 0.18-µm CMOS Technology" IEEE transactions on VLSI systems,VOL.19, No.8,August-2011

[2] R. Schmidt, T. Nörgall, J. Morsdorf, J. Bernhard, and T. Grün, "Body area network BAN, a key infrastructure element for patient-centered medical applications," Biomed. Eng., vol. 47, pp. 365–368, 2002.

[3] G. Z. Yang, Body Sensor Networks. New York: Springer, 2006.

[4]B. Lo, S. Thierjarus , R.King and G.Yaang "Body Sensor network –A wireless Sensor Platform for pervasive health care monitoring "inProc.3rd Int. Conf. Pervasive Compt.2005, PP.77-80 .

[5] J. Pansiot, R. C. King, D. G. Mcllwraith, B. P. L. Lo, and G. Z. Yang,"ClimBSN: Climber performance monitoring with BSN," in Proc.

IEEE 5th Int. Workshop Wearable Implantable Body Sensor Netw.Jun.2008,pp. 33–36.

[6] Texas Instruments, Dallas, TX, "Texas Instruments CC2420 preliminary datasheet (rev 1.4)," 2006.

[7] C. C. Wang, C. C. Huang, J. M. Huang, C. Y. Chang, and C. P. Li,"ZigBee 868/915-MHz modulator/demodulator for wireless personal area network," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.16, no. 7, pp. 936–939, Jul. 2008.

[8] C. C. Wang, J. M. Huang, L. H. Lee, S. H. Wang, and C. P. Li, "A low-power 2.45 GHz ZigBee transceiver for wearable personal medical devices in WPAN," in Proc. IEEE Int. Conf. Consumer Electron.(ICCE), Jan. 2007, pp. 1–2.

[9] S. J. Song, N. Cho, S. Kim, J. Yoo, S. Choi, and H. J. Yoo, "A 0.9 V 2.6 mW body-coupled scalable PHY transceiver for body sensor applications," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2007, pp. 366–367.

[10] H. H. Ma, J. Y. Yu, T. W. Chen, C. Y. Yu, and C. Y. Lee, "An OFDMA based wireless body area network using frequency pre-calibration," inroc.IEEE Int. Symp. VLSI Des., Autom. Test (VLSI-DAT) , Apr. 2008,pp. 192–195.

[11] Xin Liu, Yuanjin Zheng, Bin Zhao, Yisheng Wang, and Myint Wai Phyu " An Ultra Low Power Baseband Transceiver IC for Wireless Body Area Network in 0.18-□m CMOS Technology" . IEEE transactions on Very Large Scale Integration (VLSI) systems, vol. 19, no. 8, august 2011

[12]X. Liu, M. W. Phyu, Y. S. Wang, B. Zhao, and Y. J. Zheng, "An ultra low power baseband transceiver IC for wireless body area networks" in Proc. IEEE 5th Int. Workshop Wearable Implant. Body Sensor Netw. Jun. 2008, pp. 231–234.