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A Low THD Class-D Audio Amplifier with Harmonic Reduction

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Abstract

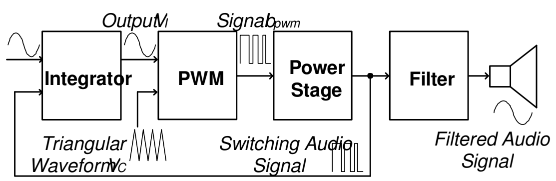
In this prroject, a class-D audio amplifier which combines the merits of the phase shifted carrier and the multiple level carrier. The proposed closed-loop amplifier includes a 2nd order integrator and a DLDPC triangular wave generator. High quality audio amplifiers should exhibit high power efficiency, while maintaining satisfying high fidelity to the human ear at the same time. Two sets of 180° out-of-phase triangular waves are used as carriers, and each set has its respectful offset voltage level with non-overlapping amplitude. By performing the double Fourier analysis, it can be found that the linearity can be enhanced and the distortion can be reduced with the proposed modulation. Experimental results shows that the proposed fully differential DLDPC PWM class-D audio amplifier feature a total harmonic distortion is lower than 0.01% with an output voltage swing of +or– 5V.

***Keywords* – Class-D, dual-level dual-phase carrier, DLDPC PWM, PSCPWM, MLCPWM, THD, IMD.**

I. INTRODUCTION

Audio amplifier design has recently been the focus of research interest with the increasing popularity of portable consumer electronics. Class-A, B, and AB audio amplifiers topologies provide the best linearity; however, due to poor power efficiency, their applications are limited to low power ear jack amplifiers . Class-D amplifiers, on the other hand, provide high power efficiency over a wide modulation index range.

Thereby, power consumption and heat dissipation can be reduced simultaneously even with high crest factor for audio and RF applications alike. Due to the switching nature of class-D amplifiers, the output signal will be affected by additional total harmonic distortion (THD) components and linearity will be degraded. Hence, in order to improve the audio quality of the class-D



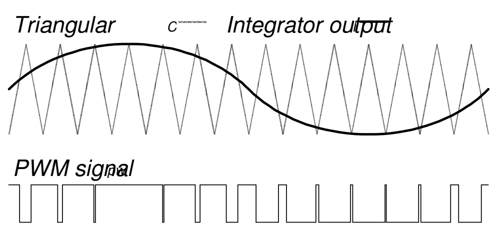
. The block diagram of a closed loop class D audio amplifier.

Audio amplifiers, THD components must be minimized Integrator PWM.

It is a switch-mode amplifier with a power stage that produces a switching audio signal. Within a given period of time, the integral of this switching audio signal should be identical to the integral of the input audio signal, V_{in}. To achieve this operation, an integrator is used to regulate the voltage feedback from the power stage with V_{in}, and is responsible for suppressing non-idealities occurring in the loop. In certain design, current feedback is also used to stabilize the loop and reduce nonlinearity . Noise injected from the power supply can also be removed from the loop to yield a high power supply rejection ratio (PSRR). For analog PWM, the integrator output V_I is modulated with a triangular waveform which serves as a carrier V_C, where as a digital PWM utilize a pulse former in the digital domain to determine the duty of the switching signal , This operation is a sampling process of V_I, which results in a square waveform

PWM signal $b_{pwm}(t)$. The duty cycle of $b_{pwm}(t)$ corresponds to the magnitude of V_I. the switching of $b_{pwm}(t)$ and the power stage occur when V_C intersects V_I. Since electromagnetic noise is generated due to the switching nature of the amplifier , the cascaded output filter is required to remove the generated high frequency components and obtain the filtered audio signal , . Notably, due to the nature of modulation, the PWM output signal will be influenced by harmonics and inter-modulation (IMD). Consequently, the THD and IMD performance of a class-D audio amplifier is deteriorated .

Fortunately, by using different types of triangular waves as carriers, the influences to the aforementioned non-idealities can be reduced. This can be achieved by adding multiple triangular wave phases and different DC levels to modify the modulation characteristics. By analyzing their influences using the double Fourier series method, it can be discovered that phase shifted carrier pulse-width modulation (PSCPWM) – single phase single level triangular wave.



A PWM signal obtained by modulating the integrator output with

Multi-level carrier pulse-width modulation (MLCPWM) with multiple numbers of phases and levels of triangular wave combination can lead to better THD and IMD performance. Since both PSCPWM and MLCPWM are designed for DC/AC inverters, the implementation of these topologies are not directly optimized for class-D audio amplifier applications. These issues will be further described in Section II. According to these results, the class-D audio amplifier compatible dual-level dual-phase carrier (DLDPC) PWM control is proposed to both the advantages of PSCPWM and MLCPWM to improve the THD. The PWM spectral characteristics of the DLDPC PWM signal exhibits similar components with those of PSCPWM and MLCPWM, but the power stage is re-designed to accommodate the control signal generated by the DLDPC PWM logic circuit. A test chip was fabricated in a standard 0.5μm CMOS process, and is presented to verify the proposed DLDPC class-D audio amplifier.

II. COMPARISON OF PWM, PSCPWM, AND MLCPWM

In a class-D audio amplifier, operation and output waveform of the power stage are directly controlled by $b_{pwm}(t)$. Hence, Fourier analysis can be applied to $b_{pwm}(t)$ to characterize its frequency components and determine its THD and IMD performance. Unfortunately, since the switching point in the PWM waveform is determined by the trigonometric equation involving both ω_I and ω_C (the angular frequencies of V_I and V_C, respectively), the Fourier analysis has to be performed over the interval according to the number of fundamental cycles. Thus, the resulting numerical solution will quickly become intractable. In order to overcome the aforementioned problem, the double Fourier series method can be applied instead. The derivation on the spectral components of $b_{pwm}(t)$ with double Fourier series can be found in and its result can be expressed

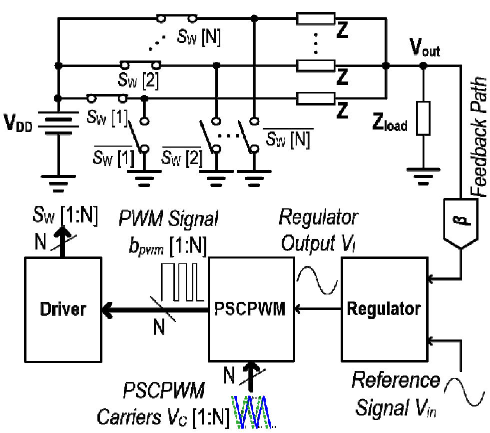
The first term represents the audio component in terms of ω_I, where M is the modulation index. The second term represents the carrier components in terms of ω_c, where m and n are the coefficients for ω_I and ω_c. The third term represents the IMD components generated by ω_I and ω_c. From , it is apparent that reduction of carrier harmonic and IMD is possible by reducing the coefficients of the second and third terms. This can be achieved by PSCPWM and MLCPWM techniques used in DC/AC inverters, which utilize different modulation schemes are described as follows.

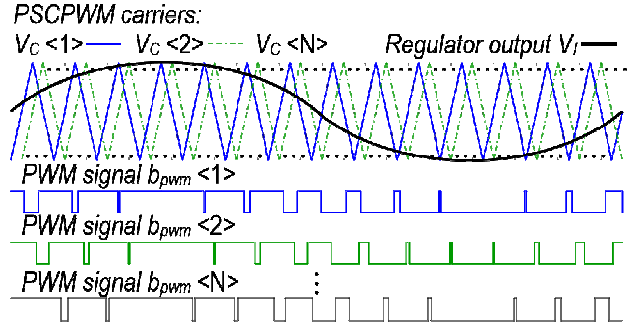
A. Phase shifted carrier pulse-width modulation (PSCPWM)

The PSCPWM scheme modulates V_I with multiple triangular waves as carriers. Each triangular wave has a 360°/N phase shift compared to the adjacent triangular waves, where N is the number of phases in the modulator of the PSCPWM controller. The

power stage is composed of N switching legs, each with its output impedance, Z. Basically, all the output impedances have identical values, and all the currents sum up at the load impedance, Z_{load}.
In a closed-loop implementation, the regulator is used to sense and regulate V_{out} from the feedback path β with V_{in}. Signals b_{pwm} <1:N> are generated to control their respective switches S_W <1:N>. To visualize this operation is drawn with b_{pwm} <1:N> plotted with N carriers and V_I. A N-phase PSCPWM results in N+1 PWM decision levels, and the effective discrete voltage levels at the output is increased by a factor of N compared to its conventional PWM counterpart. This type of implementation reduces the amplitudes of high frequency components, where the total number of m in is reduced from 1, 2, 3 ...+∞ to N, 2N, 3N, Hence, the harmonic components of the carrier and IMD are reduced by a factor of N, enhancing the fidelity of the amplifier significantly.

Unfortunately, the power stage required by the PSCPWM scheme has to be implemented by N impedances through the use of costly inductors. Furthermore, since the time constant of each inductor and the speaker resistance creates a pole in the frequency domain, the discrepancy of inductance values in each inductor would result in different phase shift to each switching leg, increasing harmonics. Hence, this modulation scheme is not preferred.



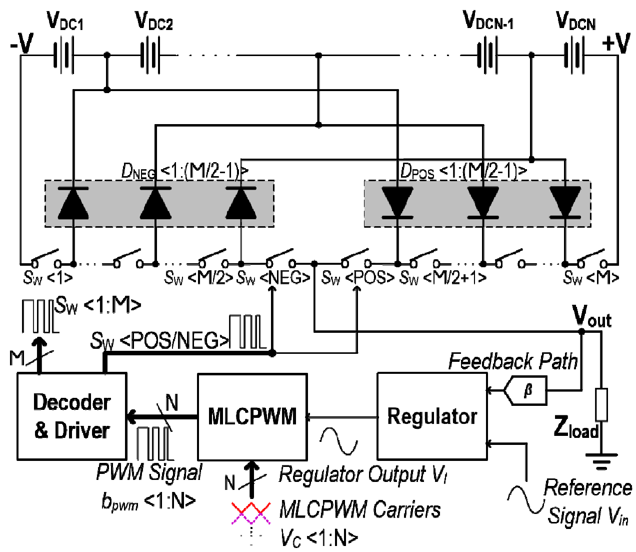


(b)

(a) DC/AC inverter with the PSCPWM technique. (b) PWM waveforms of the PSCPWM.

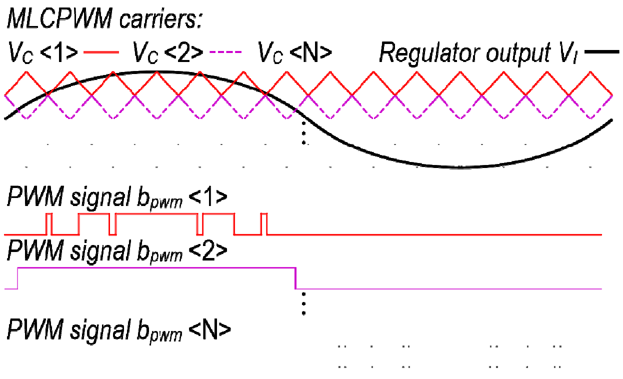
B. Multi-level carrier pulse-width modulation (MLCPWM)

The MLCPWM modulates the integrator signal V_I with N carrier levels, resulting in N-levels of supply voltages at the power stage. N stacked V_{DC} voltage sources are used to generate different voltage levels to drive Z_{load}. PWM b_{pwm} <1:N> signals. Unlike the PSCPWM PWM, only the PWM signal with an associated triangular wave that intersects with V_I is switching, while other PWM signal may remain static for an indefinite period of time. The MLCPWM decoder and the driver are used to



(a)

convert b_{pwm} <1:N> to the switch control signal, S_W <1:M>.



(b)

(a) A DC/AC inverter and (b) PWM waveforms of the MLCPWM technique.

The MLCPWM approach has two major issues. The forward conduction voltages of the diodes D_{POS} and D_{NEG} in the conduction path of the power stage cause additional distortion to class-D audio amplifier applications. Furthermore, as the number of N becomes increases, it is difficult to maintain low conduction loss while more transistors are stacked.

The voltage level is equivalent to V_{DC} multiplied by$N$-1, resulting in a similar effect on the high frequency components of b_{pwm}, analogous to the PSCPWM technique.

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Having addressed the advantages and disadvantages of both the PSCPWM and MLCPWM techniques, it is clear that neither approach is ideal for class-D audio amplifier applications if used directly, yet each approach has its potential of reducing harmonic components. Therefore, the dual-level dual-phase carrier (DLDPC) PWM control is proposed to combine the benefits of both the PSCPWM and MLCPWM techniques, in order to achieve low harmonics.

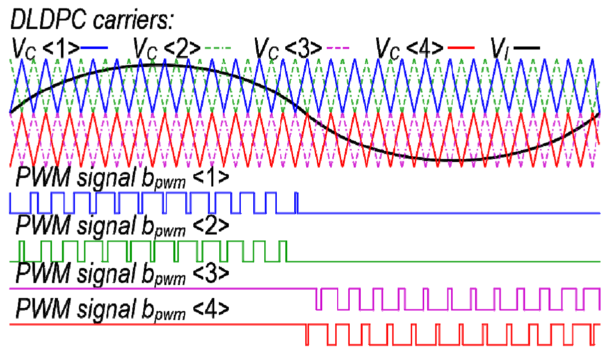


Fig. 5. Waveforms of the proposed DLDPC PWM control technique.

III. DESIGN OF A CLASS-D AUDIO AMPLIFIER WITH THEPROPOSED DLDPC PWM

The proposed DLDPC PWM control requires two sets of non-overlapping triangular waves which are separately biased at its corresponding offset voltage levels with non-overlapping amplitudes. Each set of triangular waves is composed of two 180° out-of-phase triangular waves

To obtain its spectral characteristics, the double Fourier series is applied again to a PWM carrier with multiple phases and DC offset voltage levels. By defining N_1 as the number of triangular wave phases, and N_2 –1 as the number of triangular wave DC offset voltage levels, b_{pwm} can be expressed.

The circuit realization of DLDPC PWM requires four comparators for single-ended implementation, and eight comparators for fully-differential implementation to compare the integrator output with their respective triangular wave. As shown in Fig. 6, the proposed closed-loop class-D audio amplifier utilizes a generic 2nd order integrator to achieve high signal to noise ratio (SNR). The fully differential class-AB operational amplifier along with common-mode feedback (CMFB) to stabilize DC operating points, and bias circuit and (c), respectively.

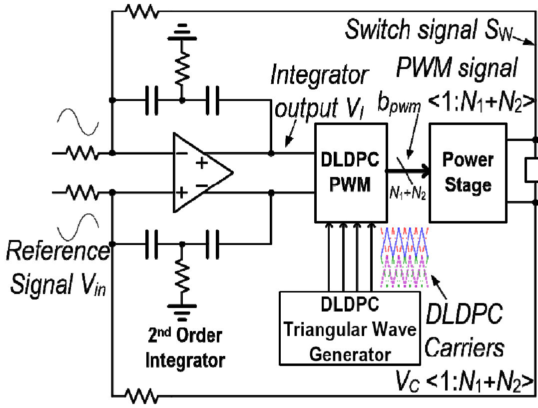
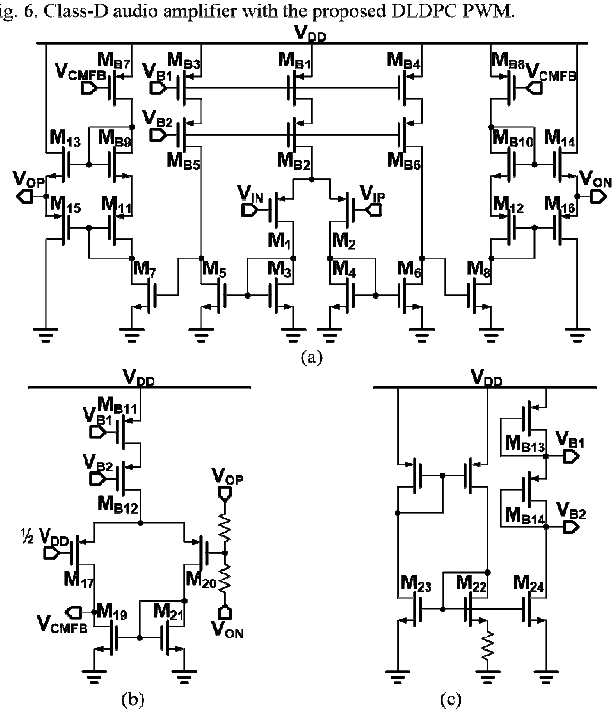


Fig. 6. Class-D audio amplifier with the proposed DLDPC PWM.



(a) A fully differential Class-AB operational amplifier, (b) CMFB, and (c) bias circuit (start-up circuit not shown).

A four-phase triangular wave generator is used to emulate the DLDPC triangular waves. The power stage is controlled by the DLDPC PWM with an 8-bit output. The detailed descriptions of the DLDPC triangular wave generator and the DLDPC PWM are described in the following sub sections.

A. DLDPC triangular wave generator

Level high and level low triangular waves must be biased at an appropriate voltage level, and must not be overlapped. Failure in preventing the triangular waves from overlapping will cause the integrator output to be sampled twice, and the power stage will be erroneously triggered, which results in double-sampling and undesired switching loss at the power stage. On the contrary, if the non-overlapping gap is too large, a dead-band will be generated. Both phenomena causes severe degradation to THD performance. Moreover, since the triangular waves are not controlled by the closed-loop, the 2nd order integrator will not be able to suppress the distortions caused by the dead-band. A deteriorated THD performance negates the purpose of using DLDPC PWM.

To ameliorate this issue, a four-phase triangular wave generator is used. This circuit includes a master integrator, a ripple counter, an encoder, and a 4-bit integrator. The master integrator is implemented to serve as an oscillator which generates a pulse signal, Q_1. Since the master integrator circuit has identical behavior with the 4-bit integrators, the pulse signal Q_1 can adapt to the characteristics of the 4-bit integrators. The operation of this master integrator can be described as follows: Assume the integrator is initially charging and its voltage begins to build up at its output. When 4V is reached, the Q_2 of the SR_2 latch is triggered to logic high, M_{I1} is switched off, and the voltage of the integrator will remain still. When the external CLK signal set SR_1 to logic high, M_{I3} is switched on and the voltage of the integrator begins to decrease. When 1V is reached, the Q of both SR latches becomes logic low, M_{I1} and M_{I2} begin to conduct and the voltage of the integrator begins to increase. These operations repeat indefinitely. Since the capacitor of the master integrator is only half the capacitance compared to the capacitors of the 4-bit integrator, the oscillation frequency of Q_1 is doubled in comparison with the output of the 4-bit integrator, V_C'. An encoder is used to generate the 4-bit phase control signal The CMFB circuits of the fully differential OP-AMPs will also help to stabilize the DC level of the output triangular waveforms. Due to the large value of capacitors used, the layout is widely spread across the chip. In the event of device mismatch and offset, the triangular waves may saturate near 1V or 4V by several millivolts, and THD performance will be deteriorated at the peak output power of 1.56W. However, since the THD performance is already poor due to the influence of clipping at the peak power output and other non-idealities, the deterioration contributed by the triangular waves is negligible. For this reason, the analysis is performed with the assumption that the output power is not saturated.

The $V_{C'}$ waveforms generated by the four phase triangular generator are not directly compatible with the DLDPC modulation. In order to realize an operation equivalent to the waveforms in Fig. 5, the voltage comparator used for PWM operation has to be re-designed. As shown in Fig. 9, an analog multiplexer is incorporated into the input stage of the comparator, and transistors M_{C2} and M_{C3} are connected to 180° out-of-phase triangular waves. An output inverter is used to deliver the binary signal to the power stage. In order to evaluate the impact on the accuracies of DLDPC triangular wave generator, FFT is applied to b_{PWM} with MATLAB. The THD of the class-D audio amplifier is evaluated over a wide range of non-idealities including the triangular wave phase shift and offset of DC levels.

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IV. *DLDPC power stage and signal flow*

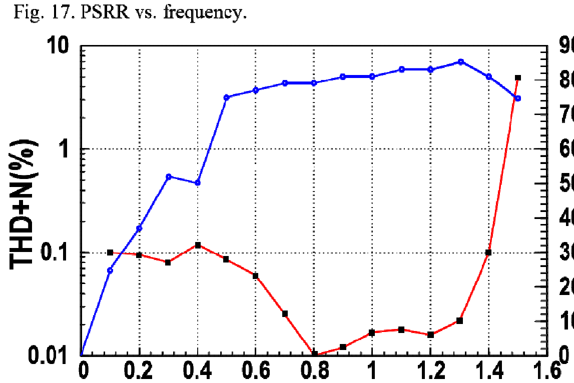
The proposed sequenced gate drive circuit, is used to switch gradually. Delay elements are inserted between the gate drive of staggered-size power transistors. When the SR latches are triggered to logic high, the ON signal propagates from the smallest to the largest transistor. If the values stored in the SR latches are reset to logic low, the OFF signal propagates from the largest to the smallest transistors. The geometric progression on the aspect ratio of the power transistors is set to 4 to optimize between transition time and shoot-through current. This approach can avoid THD and EMI caused by dead-time, and allows a higher switching frequency of 700-kHz. When the switching frequency is higher, smaller passive components can be used to implement the filter and to reduce the overall size of the system at a cost of efficiency.

Each set contains two N-type and P-type MOSFETs, which are used to produce differential output levels from 0, ¼ V_{DD}, ¾V_{DD}, V_{DD} at SPKP and SPKN to drive the BTL differentially. When all power MOSFETs are turned off, small power MOSFETs are used to short SPKN and SPKP, resulting in a voltage near ½ V_{DD}. The ability to bias the BTL at a voltage of ¼V_{DD} and ¾ V_{DD} lowers switching loss when driving a signal at lower amplitude.

V. *MEASUREMENT RESULTS*

The test chip shown in Fig. 13 is fabricated using a 0.5-µm CMOS process, with an area of around 2mm^2. CLK is provided externally at 2.8-MHz to generate $V_{C'}$. A single-inductor a value of -88dB for a 200mV perturbation at V_{DD}. The efficiency and THD+N is plotted against output power in Fig. 18. The output power of the proposed class-D audio amplifier must be larger than 0.39W for the DLDPC modulation to show advantages. If the output power is smaller than 0.39W, the power transistors connected to V_{DD} and GND will not conduct. This situation will limit power efficiency at light load, and efficiency approaches 80% at a 0.6W output. Finally, a comparison is made in Table I to compare the proposed DLDPC class-D audio amplifier with prior arts.

Fig. 17. PSRR vs. frequency.



VI. CONCLUSIONS

In this Project, the PSCPWM and MLCPWM techniques which were used in DC to AC inverter applications were compared and discussed, which leads to the proposed DLDPC

The proposed 2nd order closed-loop class-D audio amplifier with the DLDPC PWM is capable of achieving high performance and mitigates THD by implementing dual levels and dual phases of triangular waves. Thanks to low fabrication cost of the 0.5µm CMOS process, additional transistors can be used to realize the proposed technique without increasing overall price significantly. In comparison with PSCPWM and MLCPWM techniques which require additional external components such as diodes and inductors, the DLDPC PWM technique only requires the use of a SIMO converter instead of a boost converter to achieve a low THD of -80dB (0.01%).

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