RESEARCH ARTICLE OPEN ACCESS

Level Converting Retention Flip-Flop for Low Standby Power Using LSSR Technique

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Abstract

In VLSI we have an exponential increase of leakage power due to scaling of threshold voltage. We have both active power and standby power dissipation. It is important to reduce standby leakage in case of small battery operated devices. A flip-flop will hold the logic only in the active mode of operation. But a retention flip-flop will hold the data even in the standby mode of operation, with continuously given supply exclusively for the retention latch. A level converting retention flip-flop is used to turn off the voltage regulator in the standby mode of operation, to reduce standby power dissipation. The proposed retention flip-flop will reduce the standby power dissipation, in which the retention latch was designed using LSSR (LECTOR (Leakage Control transistor) Stacked State Retention) technique. The slave latch of the proposed retention flipflop constructed by using thick oxide transistors, i.e. the length of the transistor has taken as 350nm. The architecture of retention flip-flop depends on VDD,IO scheme, in which VDD,core and VDD,IO are two different voltages. VDD,IO is higher than the VDD,core. The level up conversion from VDD,core to VDD,IO is achieved by NMOS pass transistor level conversion scheme, which is based on an always low signal transmission technique. The proposed retention flip-flop reduces the standby leakage compared to LECTOR based retention flip-flop, with small increase in area. The proposed retention flip-flop was designed in 130nm technology with 1.2V and 2.0V for core latch and retention latch respectively. The operating frequency is 20MHz, and the standby power is 255.8619pW.

Keywords---**VDD, ZigBee protocol**.

1. INTRODUCTION

In recent years, wireless sensor networks (WSNs) have been evolving at an accelerated pace. To build WSNs,the ZigBee protocol, in which medium access control andthe physical layer are defined by IEEE 802.15.4, has been generally used. Because the ZigBee protocol has low datarate and power specifications, its use can prolong battery life.This feature makes the ZigBee protocol preferred over other technologies such as 802.11.× and Bluetooth. In addition,most ZigBee systems-on-chips (SoCs) support a number of power modes including a standby mode that occupies thesystem 99.9% of the time to maximize the battery life.Thus, standby power reduction is extremely important for minimizing the power consumption of ZigBeeSoCs—standby power consumption

becomes more critical as the process technology scales down because the leakage current increases exponentially with the scaling threshold voltage (*Vt)* and thegate oxide thickness. To ensure that ZigBee SoCs can operate properly after returning to the active mode, the logic states containing hardware calibration, hardware configuration, and network routing information should be preserved before entering the standby mode. Data preservation is also required to achieve a smooth power mode transition between the standby mode and the active mode. Thus, retention flip-flops (RFFs) are used in many ZigBee SoCs for storing the logic states, and several types of RFFs have been widely researched. The remainder of this paper is organized as follows. The power management schemes to support the standby mode are explained in Section II. The SRAM-based and proposed RFFsare described in Section III. In Section IV, the SRAM-based RFF is compared with the proposed RFF, and the experimental results are presented in Section V. Finally, we conclude with a summary in Section VI.

i)RETENTION FLIPFLOP

In flip-flops data is stored in cross-coupled inverters. Cross-coupled inverters can hold their states in the power down mode, if their inputs are properly gated. Based on this fact, simple clock and data gating circuitries are employed in flip-flops to retain their data in the power-down mode without using any extra data-preserving latches. The Flipflop used here is known as retention flipflop.

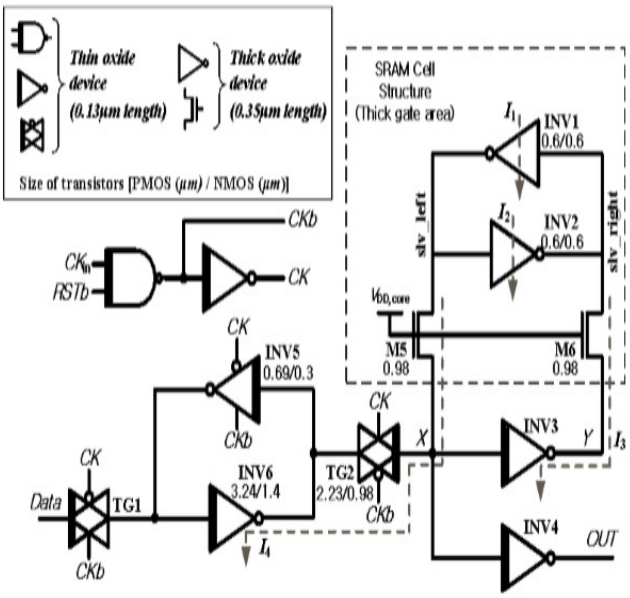

Fig 1: Structure Of the SRAM based RFF

The SRAM-based RFF uses access transistors to convert the voltage level. In the active mode, access transistors are turned on and perform write/read access. During write access, the access transistors provide differential write-access, enabling a conversion in the voltage level from VDD,core to VDD,IO when the clock is asserted high. The logic states at X and Y are the low and high VDD,core levels,

respectively, or vice versa. A low state is completely transferred to the retention latch through M5 (or M6), after which INV4 (or INV3) generates a highVDD,IO level through M2 (or M1). A high VDD,core is transferred as (VDD,core–Vt_thick) (Vt_thick is Vt of the thickoxide transistor) to the retention latch through M6 (or M5), after which the access transistor that transferred the high VDD,core is turned off, avoiding the creation of a dc current path. During read access, the access transistors supply the correct state to the VDD,core domain. In the standby mode, VDD,core is turned off, and the clock is asserted low before the access transistors are turned off; as a result, the retention latch supplied by VDD,IO is isolated by the access transistors and is able to hold data.

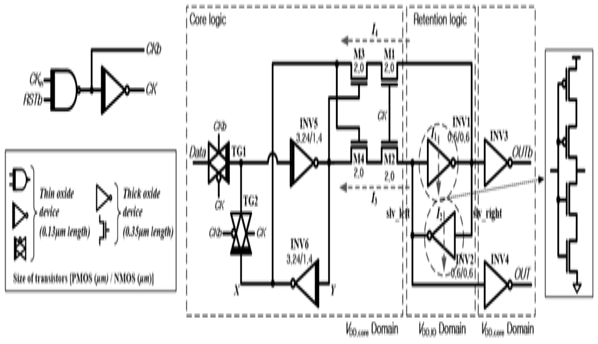

Fig 2. Structure of proposed RFF

The proposed level-converting RFF is shown in Fig. 3. The master latch is also based on a cross-coupled-inverter latch as the DFF, and an additional data transmission path (M3 and M1) is embedded. Both thin- and thick-oxide transistors are used, and the core logic and retention logic are supplied by *V*DD,core and *V*DD,IO, respectively. Level-up conversion from the *V*DD,core domain in the master latch to the *V*DD,IO domain in the slave latch is achieved through an nMOS pass-transistor level-conversion scheme similar to that developed in [18]. The proposed RFF operates as follows (Fig. 4). When nodes *X* and *Y* (or *Y* and *X)* in the master latch are high and low, respectively, an access transistor M4 (or M3) is turned on, and another access transistor M3 (or M4) is turned off. Then, the ON-state access transistor M4 (M3) forms a transmission path between the master latch and the slave latch, and node *Y(X)* becomes an input of the transmission path. In other words, only the transmission path from the master latch to the slave latch is determined on the basis of the state of data in the master latch, and the voltage level can be converted in the slave latch without generating a dc-current path because only a low signal is transmitted at all times.

ii)STAND BY POWER

Standby power is the power consumed by an appliance or device when the device is not in use but is ready to be rapidly put into

use. Standby power is also called vampire draw, vampire power, phantom load or leaking electricity.

iii)LSSR TECHNIQUE

A novel leakage power reduction technique is proposed in this work i.e LSSR [LECTOR]. Control TransistOR (LECTOR)) Stacked State Retention] The LECTOR method [2] inserts two extra Leakage Control Transistors (a P-type and an N-type) within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other.This technique have very good low leak operation but there is no provision of sleep mode of operation,to over come this problem.extra retention transistors are connected to the output so that during sleep mode the logic state is main- tained.Hence we combine the advantages of LECTOR method and the Forced Stack Technique to reduce the overall power dissipation without compromise with the loss of state.

II. SIMULATION

1.The BSIM4 MOS Model

A family of models has been developed at the University of Berkeley for the accurate simulation of submicron technology. The Berkeley Short-channel IGFET Model (BSIM) exist in several version (BSIM1, BSIM2, BSIM3). The BSIM3v3 version, promoted by the Electronic Industries Alliance (EIA) is an industry standard for deep-submicron device simulation. A new MOS model, called BSIM4, has been introduced in 2000. A simplified version of this model is supported by Microwind2, and recommended for ultra-deep submicron technology simulation. BSIM4 still considers the operating regions described in MOS level 3 (linear for low Vds, saturated for high Vds, subthreshold for Vgs<Vt), but provides a perfect continuity between these regions. BSIM4 introduces a new region where the impact ionization effect is dominant. The number of parameters specified in the official release of BSIM4 is as high as 300. A significant portion of these parameters is unused in our implementation. We concentrate on the most significant parameters, for educational purpose. The set of parameters is reduced to around 20. where VTHO is the long channel threshold voltage at Vbs=0 (Around 0.5V), K1 is the first order body bias coefficient (0.5 V1/2), Fs is the surface potential, Vbs is the bulk-source voltage, K2 is the second order body bias coefficient, DVtSCE is the short channel effect on Vt, DVtNULD is the non-uniform lateral doping effect, and DVtDIBL is the drain-induced barrier lowering effect of short channel on Vt. Concerning the

formulations for mobility of channel carriers, he generic parameter is U0, the mobility of electrons and holes. The effective mobility meff is reduced due to several effects: the bulk polarization, and the gate voltage. The equation implemented in Microwind2 is the most recent mobility model proposed in BSIM4.

Temperature effects on the MOS

The MOS device is sensitive to temperature. Two main parameters are concerned: the threshold voltage VTO and the transconductance coefficient KP that decrease with temperature increase. The physical background is the degradation of mobility of electrons and holes when the temperature increase, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers.

III. SIMULATION RESULTS

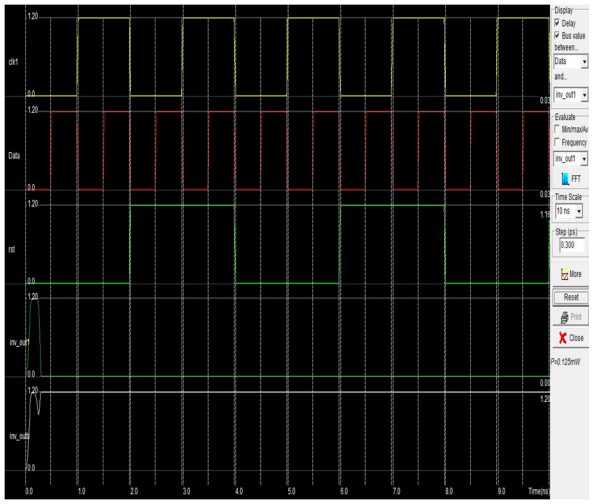

Fig:-3 Simulation output

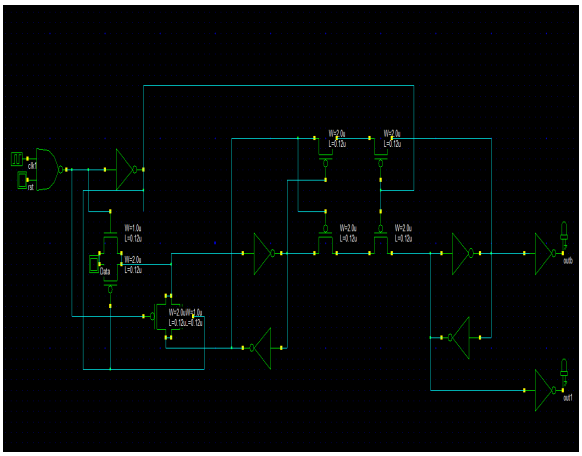

Fig:-4 Schematic Diagram

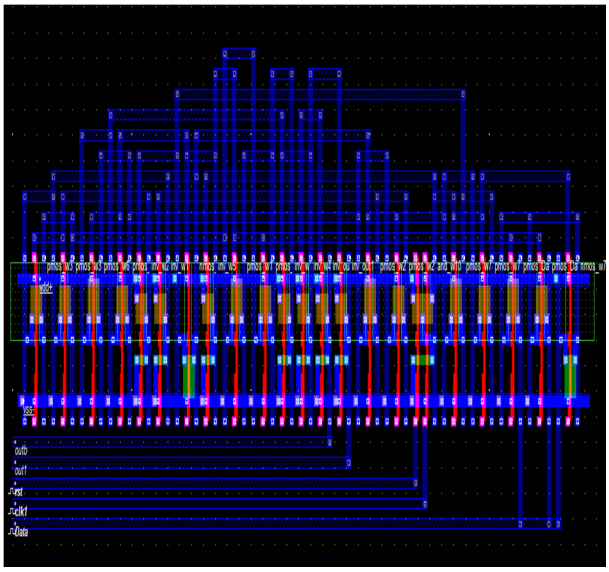

Fig:-5 Layout

IV.CONCLUSION

An RFF that retains data using VDD,IO and performs level conversion using an embedded nMOS pass-transistor level-conversion scheme employing a low-only signal- transmitting technique was proposed in this paper. The proposed RFF achieves ultralow-standby power by adopting a power management scheme to use VDD,IO for data retention and to turn off the voltage

regulator in the standby mode. The embedded level conversion scheme eliminates the need for an additional level-up converter in the proposed RFF. In addition, the retention latch in the proposed RFF is composed of a stacked structure with thick-oxide transistors to reduce the standby leakage current. As validated in the simulations and experiments, the proposed RFF is highly suitable for deployment in low-activity sensor networks using the ZigBee protocol.

V. REFERENCES

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