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Design of Full Adder in 180nm Technology Using TG and Adiabatic Logic

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Abstract:

The main goal of this paper to produce new low power solutions for very large scale integration(VLSI).The main focus of this research on the power consumption, which is showing an ever-increasing growth with scaling down of the technologies. The full adder is the most important component of any digital system applications. To limit the power dissipation, this full adder is designed with adiabatic technique PFAL and it compare with partial adiabatic technique ECRL. These analysis have done on TANNER simulator V 7 technology. The power is reduced up to 70-80% as compared to other methods.

Keywords -**ECRL, TG, PFAL, Full Adder. Adiabatic Circuit**

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1. INTRODUCTION

The demand for low power circuits has encouraged the designers to explore the new methods to design the VLSI circuits. Then, designers move towards the energy recovery techniques such as adiabatic techniques. The main sources of power dissipation are static power consumption, dynamic power consumption and short circuit power consumption. Majority of power is dissipated in pull up network of conventional CMOS network and remaining power is stored on node capacitor [1].This stored charge is wasted in ground. But, it can be recycled back and used as power clock again. It is mention in thermodynamic process which is a reversible logic. The adiabatic logic is worked on this thermodynamic phenomenon and it can recover the partial or whole power from the load. In this paper, authors have designed the full adder using partial adiabatic logic methods. One is ECRL (Efficient Charge Recovery Logic) and other is PFAL(Positive FeedbackAdiabaticLogic).Both methodologies have own significance and authors have also compare their results with each other and

PFAL has better calculation and results as compared to partial ECRL. It gives better performance in terms of energy consumption, useful frequency range and robustness against technology variation [2].

1.1 Transmission Gate Logic

A transmission gate is constructed by combination of NMOS and PMOS transistors with complementary gate signals. It gives full output swing and its uses can increase the speed in CMOS circuits. There is no isolation between the input and output [3].
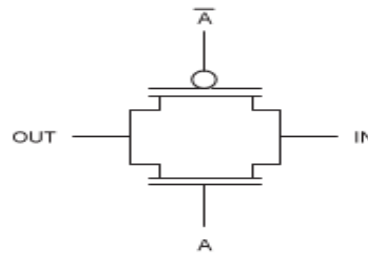

Fig 1: Transmission Gate Logic [3]

1.2 Adiabatic Principle

The word ADIABATIC emanates from a Greek word that is utilized to describe

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thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In authentic-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by decelerating the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as ENERGY RECOVERY CMOS. In the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems. Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits). Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp [4]. Assume, the capacitor voltage V_c is zero initially.

The voltage across switch= IR   1.1

P (t) in the switch = $I^2 R$ 1.2

Energy during charge = $(I^2 R)T$ 1.3

$E = I^2 R = (CV/T)^2 RT = \dfrac{c^2 v^2}{RT}$ 1.4

$E = E\,diss = \dfrac{RC}{T}\,CV^2 = \dfrac{2RC}{T}\,\dfrac{1}{2}CV^2$ 1.5

where, the various terms of Equation (1.3) are described as follows:

E ― energy dissipated during charging,
Q ― charge being transferred to the load,
C ― value of the load capacitance,
R ― resistance of the MOS switch turned on,
V ― final value of the voltage at the load,
 T- time [5].
 Now, a number of observations can be made based on Equation (1.3) as follows:
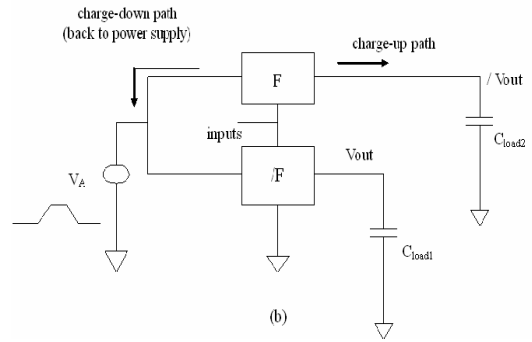

Fig 2: Adiabatic Logic [6]

(i) The dissipated energy is smaller than for the conventional case, if the charging time T is larger than 2RC. That is, the dissipated energy can be made arbitrarily small by increasing the charging time,

(ii) Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation [7].

1.2.1. Types Of Adiabatic Logic:

1.2.1.1 Partially adiabatic logic. They are classified as:
i) Efficient charge recovery logic (ECRL)
ii) Quasi Adiabatic Logic (QAL)
iii) Positive feedback adiabatic logic (PFAL)
iv) 2N-2N2P Logic
v) True single phase adiabatic logic (TSAL)
1.2.1.2 Fully adiabatic logic. They are classified as
i) Pass transistor adiabatic logic
ii) 2 Phase adiabatic Static CMOS logic (2PASCL)
iii) Split rail charge recovery logic (SCRL) [8].

1.2.2. ECRL Logic

ECRL logic is that in which precharge and recovery phases are simultaneously worked and by this implementation, the power consumption is minimize up to greater extent. This method does not use the precharge diode and generates less energy dissipation. As

compared to other methods of energy recovery, it uses least number of PMOSFETS.It uses only two PMOSFETS for precharge and recovery phases. Due to this cross coupled PMOSFETS, the output is stored and it also charge and discharge the load capacitor according to the transition of the constant supply [9].
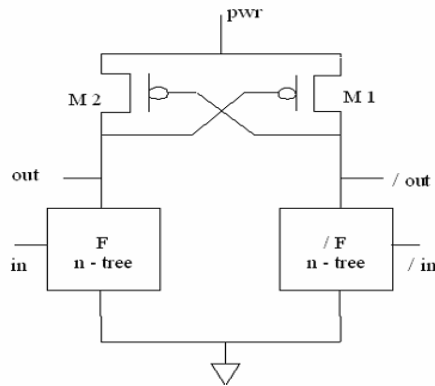

Fig 3: ECRL Logic Circuit [9]

The fig.3 shows two cross coupled PMOS transistors M1 and M 2 and two NMOS transistors logical blocks. In NMOS functional tree, one side is pull up network and other is pull down network. Both are the complement of each other. An AC ramp power supply is used in adiabatic as compared to DC power supply because it has good performance during energy precharge and recovery phases. The outputs out and out/ are drive the constant energy from power supply that is independent of input signal.ECRL always provides the full swing output. For instance, when the voltage approaches to threshold voltage then the PMOS transistors gets turned off automatically [10].

1.2.3. PFAL Logic
PFAL is partial energy recovery circuit and its core of all adiabatic circuit is made by adiabatic amplifier, a latch made up of 2 PMOSFETS M1- M2 and 2 NMOSFETS M3-

M4.Due to these MOS transistors ,the logic level degradation on the outputs nodes can be avoided.
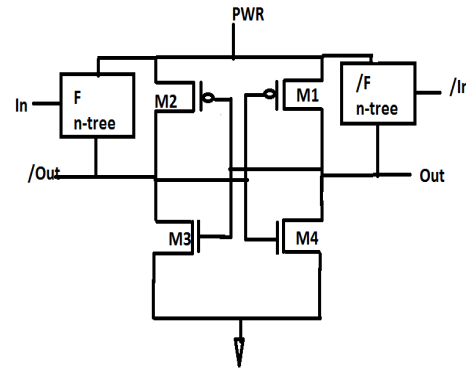

Fig 4: PFAL Logic Circuit [11]

The functional blocks of PFAL are in parallel with the PMOSFETS of adiabatic amplifier and create a transmission gate process. The two F trees realize the logic functions. It is also generates the positive and negative outputs swing [11].

2. LOGIC DESIGN STYLES

2.1 Full Adder circuit using TG
A basic full adder circuit consists of three inputs A, B, C and two outputs sum and carry. Transmission gate logic based full adder is designed with PMOS and NMOS combination and they placed opposite to each other. It is the simplest and easiest method but it dissipated more heat during transition. [12].
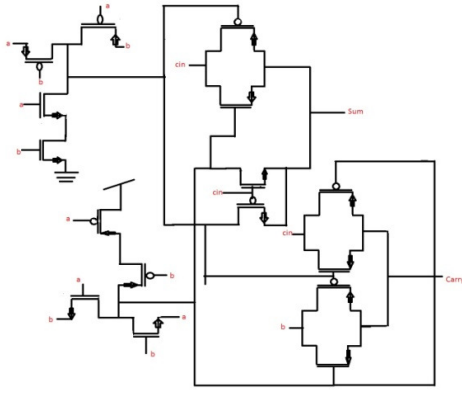
Fig 5: Full Adder circuit using TG [12]

Fig 6: ECRL Sum Circuit

2.2 Full Adder Circuit Using ECRL Logic

ECRL stands for efficient charge recovery logic. It is also known as cascade voltage switch logic with differential logic. The logic in the functional block can be realized with NMOSFETS only. The NMOSFET section is fabricated in pull down function. During precharge phase, the pull up network does work and pull down network does not conduct. Outputs hold the valid logic levels and this condition is maintained during hold phase. When the discharge or recovery phase conducts then the sum/ returns its whole power to the supply voltage. In other words, clock is work as power clock and power supply [13].The sum and carry equations are given below.
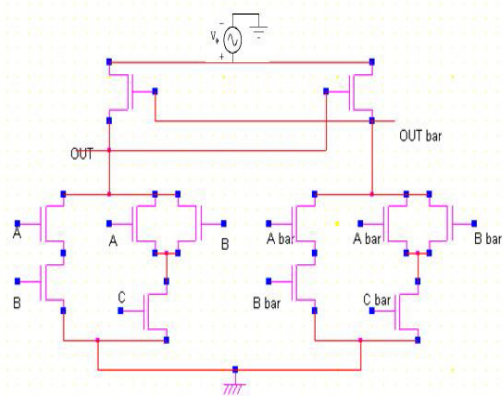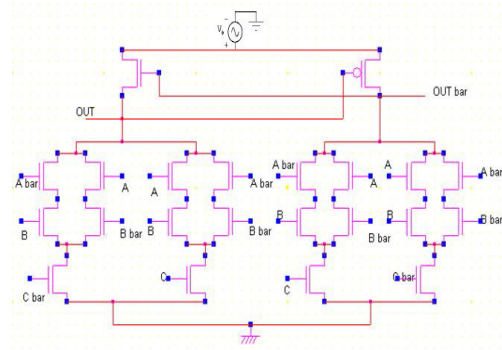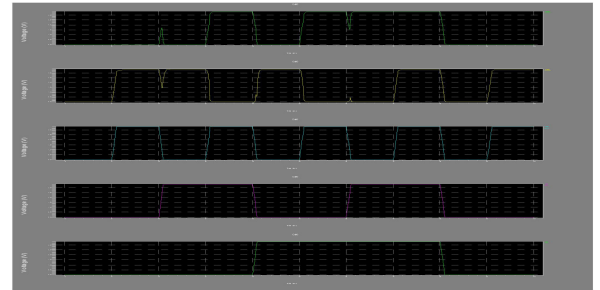

Fig 7: ECRL Carry Circuit

2.3 Full Adder Circuit Using PFAL Logic

PFAL is same as transmission gate logic. But, the major difference between them is that the PFAL latch can minimize the coupling effects and in construction, its latch is made up of two NMOSFETS and two PMOSFETS.The sum and carry equations are implemented on this basis and it produces two outputs separately.Sum,Sum bar, Carry and Carry bar are the four outputs of this circuit[13].
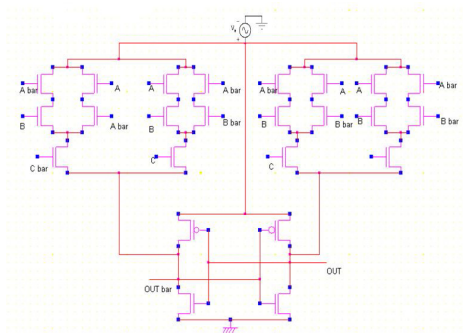
$$S = \overline{A}\,\overline{B}\,C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + ABC$$
$$C = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

Fig 8: PFAL Sum Circuit

Fig 9: PFAL Carry Circuit

Fig 12: Simulation results Of Full Adder Carry Using ECRL Logic
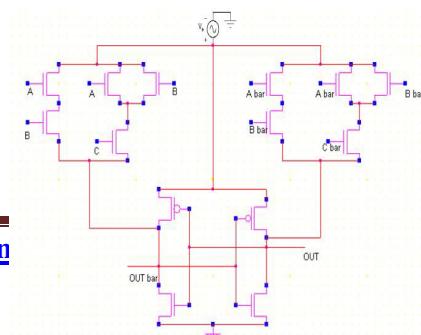
3. SIMULATED WAVEFORMS

In this paper, different methodologies are used to design the full adder using transmission gate logic and adiabatic logics. The full adder is designed on the s-edit of PSPICE software of tanner version 7.The simulation results of both the logics are presented in this section.

Figure 12 indicates that the simulated waveforms of full adder carry using ECRL.The bottom two lines indicate output signal and top sevens are inputs.

Fig 10: Simulation results Of Full Adder Using TG Logic

Figure 10 indicates that the simulated waveforms of full adder using TG.The bottom line indicate output signal and top four are inputs.

Fig 12: Simulation results Of Full Adder Sum Using PFAL Logic

Figure 12 indicates that the simulated waveforms of full adder sum using PFAL.The

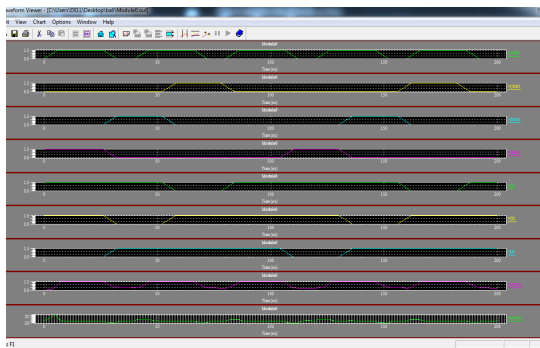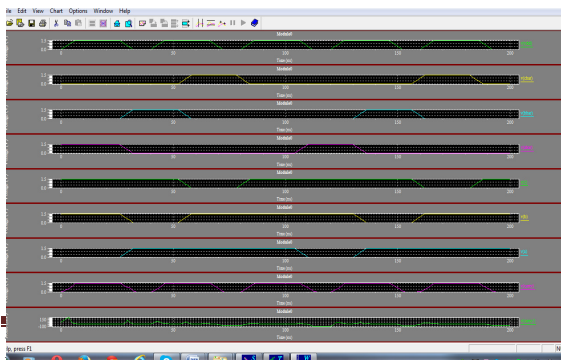bottom two lines indicate output signal and top sevens are inputs.

Fig 11: Simulation results Of Full Adder Sum Using ECRL Logic

Figure 11 indicates that the simulated waveforms of full adder sum using ECRL.The bottom two lines indicate output signal and top sevens are inputs.
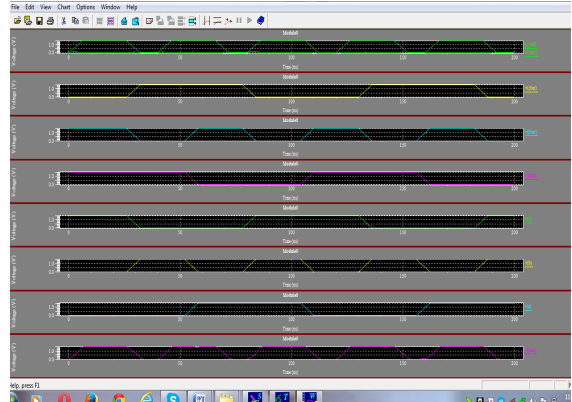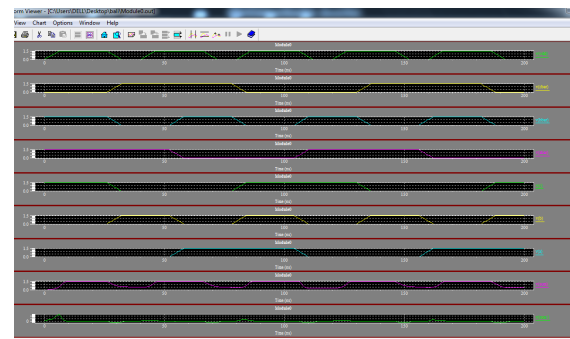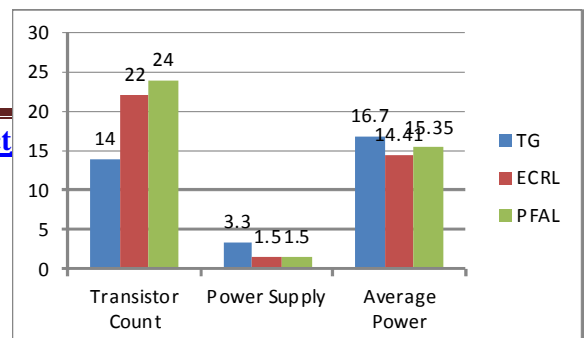
Fig 13: Simulation results Of Full Adder Carry Using PFAL Logic

Figure 13 indicates that the simulated waveforms of full adder sum using PFAL.The bottom two lines indicate output signal and top sevens are inputs.

4. RESULTS & COMPARISON

This section demonstrates the comparison results of conventional CMOS and adiabatic

Frequency	Full Adder (ECRL)	Full Adder (PFAL)
16MHz	15µw	14.72µw
20MHz	14.95µw	15.26µw
25MHz	14.41µw	15.35µw

logic in terms of average power consumption, delay and frequency. The two graphs shows the comparison of frequency with delay and power consumption and the
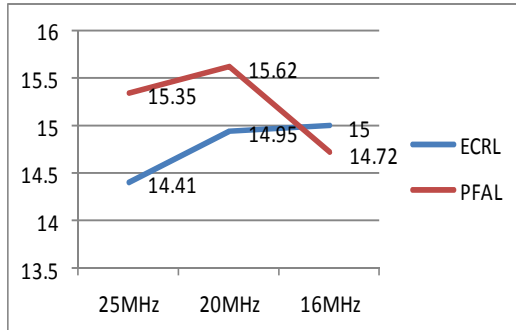
other shows the results of maximum frequency and transistor count.

Fig 14: Graph For Transistor Count, Power Supply and Average

Power for Full Adder between TG and Adiabatic logic
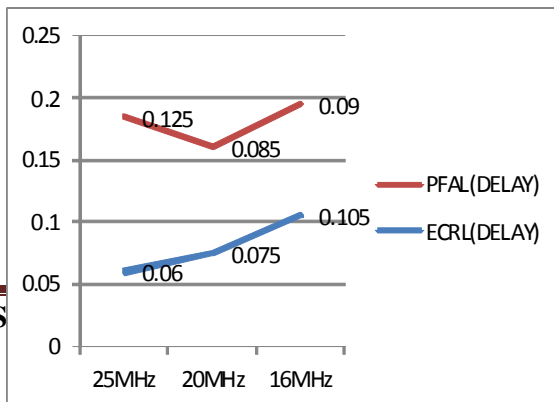
Fig 15:Avg. power verses Frequency For Full Adder

Fig 16: Delay verses Frequency For Full Adder

"Table1: Power dissipation results for full adder with frequency"

"Table1" shows the power consumption analysis of adiabatic circuit ECRL and PFAL.The final results demonstrate that the energy dissipation of energy recovery logic ECRL is less as compared to PFAL logic.

"Table2: Average power dissipated, Power Supply and transistor count of full adder circuit using ECRL family and PFAL family"

"Table 2"shows the comparison analysis of various parameters such as transistor count, power supply and average power dissipated of full adder.

Parameters	Full Adder (TG)	Full Adder (ECRL)	Full Adder (PFAL)
Transistor Count	14	22	24
Power Supply	3.3V	1.5V	1.5V
Average power	16.7µw	14.41µw	15.35 µw

"Table3: Delay verses frequency analysis for full adder"

"Table 3" shows the delay of the full adder with the different frequencies.

Frequency	Full Adder (ECRL)	Full Adder (PFAL)
16MHz	0.105s	0.125s
20MHz	0.075s	0.085s
25MHz	0.06s	0.09s

5. Conclusion

Authors have designed the full adder circuit with efficient charge recovery logic and conventional CMOS.A power consumption is reduced up to 14.41µw as compared to transmission gate with 16.7µw and PFAL with 15.35µw power consumption. All the parameters are simulated with tannerV7 on s-edit at 180nm technology. The adiabatic logic operated with pulsed power supplies of 1.5V which is very less as compared to 3.3V used in TG.All results are verified at different frequencies and temperature. Due to these performance parameters, this adiabatic approach is more convenient for energy efficient digital applications.

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