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IMPLEMENTATION OF ADVANCED UART CONTROLLER

JYOTI APPASHEB LOKHANDE

PG Scholar, E & TC Department, G. H. Raisoni College of Engineering & Management,

Chas, Ahmednagar, Maharashtra, India

ABSTRACT

This paper presents advanced UART controller with configurable baud rate. UART a kind of serial communication circuit is used widely. In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback of parallel communication and emerges effectively in many applications for long distance communication as it reduces the signal distortion because of its simple structure. Architecture of UART implemented on the Spartan 6 Series FPGA using Verilog description language based on FIFO technique to achieve reliable serial data communication. An Asynchronous FIFO is designed with read and writes pointers. The design of Controller is used to implement communication when transmitter Device and receiver Device are set at different Baud rates. The baud rates are synchronized using switches at the input side of FPGA & at the Output side of FPGA. It reduces the synchronization error between subsystems in system with other subsystem. This Paper presents the structure of UART controller as scalable and reconfigurable design. This design can effectively use for communication between two devices with different baud rates. The overall design is simulated on Xilinx ISE simulator.

KEYWORDS: UART (Universal Asynchronous Receiver Transmitter), FIFO (First in First Out)

INTRODUCTION

In Serial communication data is transmitted through serial port. A serial port is one of the most universal parts of a computer. It is a connector where serial line is attached and connected to peripheral devices, In contrast to parallel communication, these peripheral devices communicate using a serial bit stream protocol (where data is sent one bit at a time). The serial port is usually connected to UART, an integrated circuit which handles the conversion between serial and parallel data.

This paper presents UART design consisting mainly Transmitter, Receiver, Baud Rate Generator and Asynchronous FIFO. Since the system clock is much faster than the baud rate generator clock (approximately 16 times faster).

The main objective of design is to achieve reconfigurable baud rate. In this select switches are used to select different baud rates with set of conditions. When UART transmits data i.e. in specified format with one start bit, one stop bit and 8 bit data. This data is received in FIFO as 10 bit and again transmit as converted 8 bit to receiver.

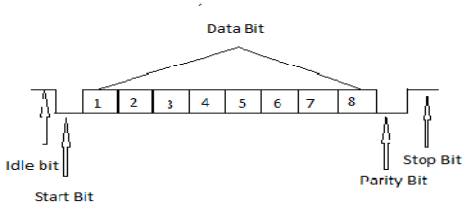


Figure 1: UART Frame Format

This Paper describes the architecture of UART and Implemented on the FPGA using Verilog description language to achieve reliable serial data communication. The design has great flexibility i.e. it is compatible with different baud rate (Configurable baud rate).

This design can effectively play a vital role in SOC technology. The design of UART which includes three modules which are the baud rate generator, receiver and transmitter. It supports configurable baud rate generator with data length of 8 bits per frame.

1. Implementation of UART

UART design is divided in three main parts transmitter module, receiver module and FIFO.

Baud rate of transmitter and receiver are selected based on frequency divider rule. In this mainly one system clock is used and according that baud rate factor are generated.

1.1. Transmitter Module

Data is transmitted through transmitter module / Device 1 with different Baud rates as Spartan 6 FPGA is Used for Implementing UART, the system clock is selected as same as the internal clock of FPGA .

Spartan 6 FPGA is having system clock of 100 MHZ frequency. So if data is to be transmitted at 4800 baud rate, the baud rate count is generated according to frequency divider rule.

Divide Factor=System clock frequency/16*Baud rate.

Assume the system clock is set to 9600 then The System clock i.e. 100 MHZ is divided by 9600 then the count is generated 10416.since the data is to be transmitted at positive edge of Clock the count is divided by 2 i.e 5208. At every rising edge of a clock 8 bit data is transmitted. During the transmission 8 bit data is only send at rising edge with factor increased by 5208. The number of clock cycles required for data transmission depends on Count which is depends on Baud rate selected.

1.2. Receiver

Data is transmitted through Spartan 6 FPGA is received by Device 2. By using the Baud rate selector switches the baud rate is selected accordingly data transmitted between FPGA (The Data which is Transmitted by Device 1 & Stored in FPGA using FIFO algorithm). Spartan 6 FPGA is having system clock of 100 MHZ frequency. So if data is to be transmitted at 19200 baud rate, the baud rate count is generated according to frequency divider rule.

Divide Factor=System clock frequency/16*Baud rate.

The System clock i.e. 100 MHZ is divided by 19200 then the count is generated 5208 .since the data is to be transmitted at positive edge of Clock the count is divided by 2 i.e. 2604. At every rising edge of a clock 8 bit data is transmitted. During the transmission 8 bit data is only send at rising edge with factor increased by 5208. The number of clock cycles required for data transmission depends on Count which is depends on Baud rate selected.

1.3. Baud Rate Generator

Baud Rate Generator is generally a frequency divider. Baud rate frequency factor can be obtained with the help of system clock frequency and the required baud rate and that factor is used as a divider. In this design we apply synchronized clock to both receiver and transmitter.

Divide Factor=System clock frequency/16*Baud rate

In this design, we have designed UART with configurable baud rate generator which can selected by using two switch combination , first two switches used for Device 1 & FPGA to select the Baud rate of the Transmitter Device. The Second two Switch combinations are used for FPGA & device 2 for Selection of baud rate of Receiver device. With this we achieve that both the transmitter & receiver devices will communicates at same Baud rate or at different baud rates depending upon switch position. The selection of baud rate is as shown.

Sr. No	S1	S0	Baud Rate(BPS)
1	0	0	9600
2	0	1	9600
3	1	0	4800
4	1	1	19200

Hence, different baud rate has different frequency coefficient (M) i.e. count value of the baud rate generator.

For 9600 Hz, M =100MHz / 9600 Hz= 10416

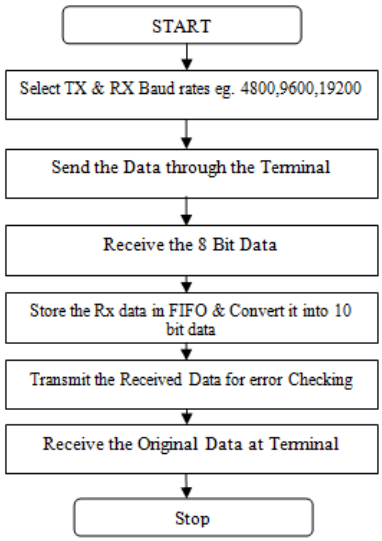
For 4800Hz, M =100MHz/ 4800 Hz=20833

For 19200Hz, M =100MHz/19200Hz= 5208

Features of Spartan 6

- FPGA: Spartan-6 XC6SLX9 in TQG144 package
- Flash memory: 16 Mb SPI flash memory (M25P16)
- 100MHz CMOS oscillator.
- USB 2.0 interface for On-board flash programming FPGA configuration via JTAG and USB
- 8 LEDs and four switches for user defined purposes
- 70 IOs for user defined purposes
- On-board voltage regulators for single power rail operation

Flow Chart of System



RESULTS

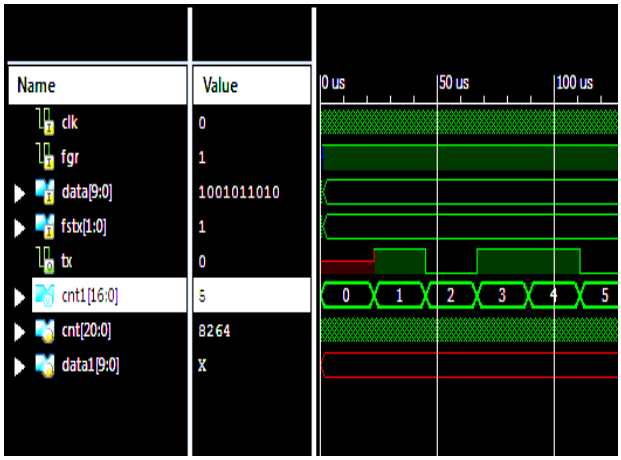


Figure 2: UART Transmitter Output

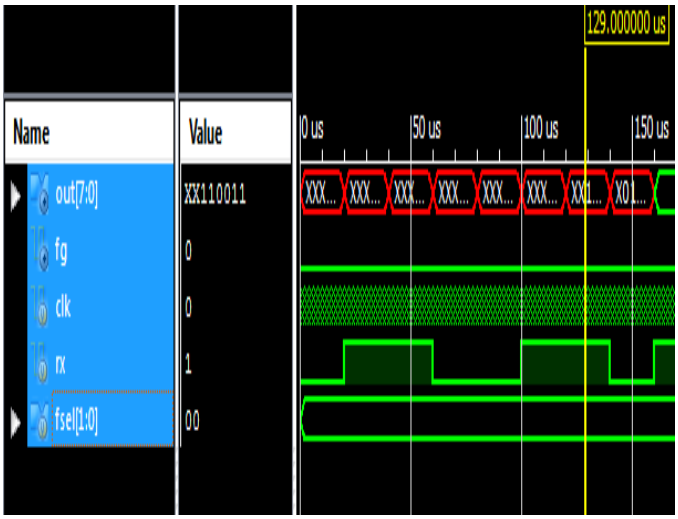


Figure 3: UART Receiver Output

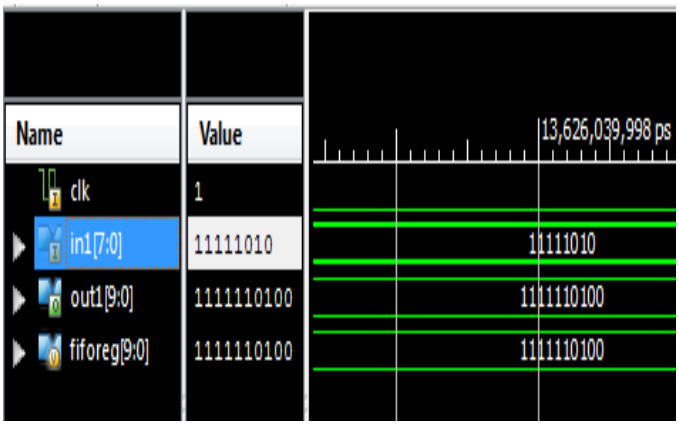


Figure 4: FIFO Input & Output Details

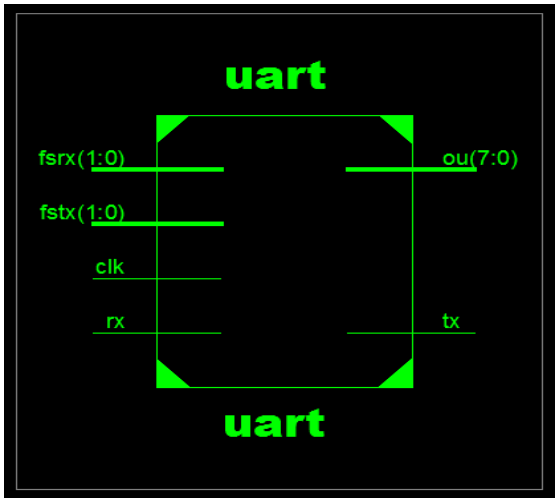


Figure 5: Technology Schematic View

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	69	11,440	1%
Number used as Flip Flops	69		
Number used as Latches	0		
Number used as Latch-thrus	0		
Number used as AND/OR logics	0		
Number of Slice LUTs	462	5,720	8%
Number used as logic	461	5,720	8%
Number using O6 output only	301		
Number using O5 output only	45		
Number using O5 and O6	115		
Number used as ROM	0		
Number used as Memory	0	1,440	0%
Number used exclusively as route-thrus	1		
Number with same-slice register load	0		
Number with same-slice carry load	1		
Number with other load	0		
Number of occupied Slices	159	1,430	11%
Number of MUXCYs used	224	2,860	7%
Number of LUT Flip Flop pairs used	467		

Figure 6: Device Utilization Report

CONCLUSIONS

In this design, we have designed UART with configurable baud rate generator which can selected by using two switch combination , first two switches used for Device 1 & FPGA to select the Baud rate of the Transmitter Device. The Second two Switch combinations are used for FPGA & device 2 for Selection of baud rate of Receiver device. With this we achieve that both the transmitter & receiver devices will communicates at same Baud rate or at different baud rates depending upon switch position.

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