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A Low Power High Speed CMOS Based Optical Receiver for Communication Network Based Applications

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Abstract: The advancement of communication based technology and the growth of the internet traffic have continuously driven the fast evolution of the intelligent networks based applications. As compared to the traditional optoelectronic switch based devices, all the optical transreceiver provides high throughput, rich routing functionalities, and excellent flexibility for rapid signal exchange in optical networking based systems. Among various optical switches, the thermal actuated ring switching devices provides the advantages of high accuracy, easy actuation, and reasonable switching speed for better data communication. However, when this device is used in the system scale up, it may encounter certain issues related to fabrication error, non accurate wavelength. A low-power multi-band RF receiver including a multi-band low-noise amplifier (LNA) based on the IEEE 802.15.4 standard for sensor node applications response, and large terminal numbers in the control circuit. A 12-channel parallel optical receiver front-end amplifier array design and realization in a low cost 0.18 μm CMOS technology. The integrated circuit system has been designed, simulated and demonstrated with a decent performance having free spectral range (FSR) equal to 1.5 nm at 1534 nm and very accurate wavelength modulation to 0.3 nm within 0.01 nm fluctuations for thermal actuated ring type optical switch.

KEYWORDS: Optical receiver, CMOS, Fiber-optic receiver, Low-cost front-end CMOS preamplifier, Trans-impedance amplifier, optical switch, thermal optic, frequency modulation.

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1. Introduction

The optical and wireless communication systems have been applied in many transmission interfaces recently. The frequency synthesizer is a major and most critical component of the optical based wireless transceiver. At high speeds and high pore densities, the power dissipation of optical transceivers becomes a critical element as it determines the type and size of package module. The complementary metal oxide semiconductor (CMOS) technology has the advantages of low cost and thus, it is widely used to implement these devices which are used in intelligent networks. At the GHz frequency range, it is proven to be the best substitute for the low power operation based systems. One of the most important modules of the frequency synthesizer which is employed in the feedback is the pre-scaler, which simply takes a periodic signal and in turn generates a periodic output signal, whose frequency is a fraction of the input frequency. But there is a limitation with the use of the pre-scaler module since it operates at the highest frequency of the signal and consumes quite large power. Thus, the design of high speed pre-scalers module is the dire need of the technology so that a highly efficient networking based application can be designed and implemented [1, 5].

The basic requirement of an optical communication system is to carry large volumes of data across a long distance with the help of the most optimized transreceivers. The block diagram of a complete optical communication system is shown in figure 1. The data provided to the transmitter is in the form of low speed parallel data which are generated by multiple users. The task of parallel-to-serial conversion is performed by a multiplexer (MUX) which requires a number of clock frequencies with precise edge alignment. These clocks required can be quite easily generated by using a PLL. The laser driver of receiver delivers large currents to the laser, and the trans-impedance amplifier (TIA) amplifies the output of photodiode with low noise and sufficient bandwidth, and converts it into to a voltage. Since the received data may exhibit substantial noise, decision circuit, de-multiplexer (DMUX) and clock and data recovery (CDR) are interposed to reproduce the original parallel channels [6, 8].

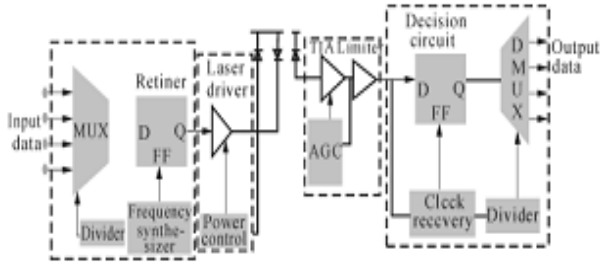

Figure 1: Complete Optical Communication System [9]

The drastically increasing demands for large data capacity require high-speed interconnections with ever increasing data transmission rate. the multimode parallel optic-fiber links appear to be the most promising favored solution. Figure 2 shows the simplified block diagram of such a parallel link. Incase of the opto-electronic based systems with high operation speed upto/beyond 10 Gb/s, the design for low cost, low power consumption and high integration level becomes a real challenge. The frontend amplifier is the most critical element in an optical receiver affecting the whole system performance such as speed, sensitivity, and signal-to-noise ratio. Hence, the design mandates careful optimization of a number of tradeoffs among bandwidth, gain, and noise. The receiver front-end circuits operating at such high data rates are mainly dominated by SiGe, GaAs, and InP technologies. However, the submicron CMOS technologies have recently become very attractive due to their low cost and high integration level characteristics can be easily designed and fabricated in a standard 0.18μm CMOS technology [10, 15].

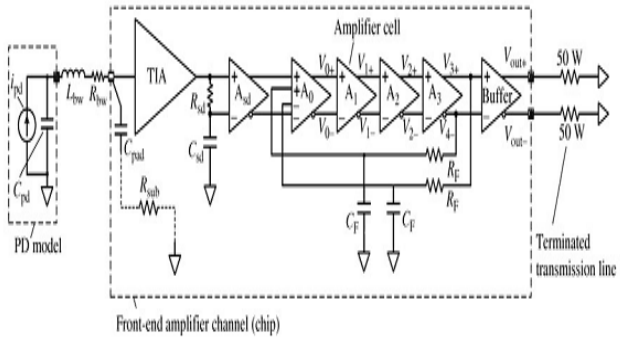

Figure 2: Optical receiver front-end amplifier architecture [16]

The most conventional multi-band receiver architectures are implemented by using multiple individual receiving paths, which increase the cost, power dissipation, and complexity. To overcome these disadvantages, a con-current receiver architecture which can simultaneous receives signals in a multi-band, has been developed. However, this architecture experiences a linearity problem since the spurs in one band can corrupt signals in the other band.

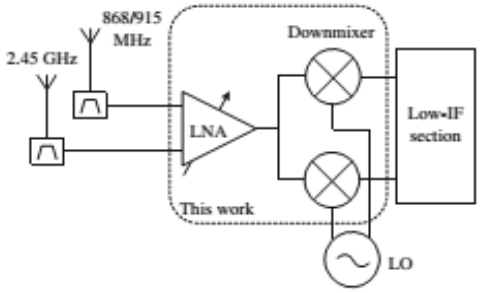

Figure 3: Multi-band receiver architecture [17]

The relevant receiver specifications are sensitivity, selectivity, and dynamic range. Receiver sensitivity can be represented as a noise figure (NF). Therefore, the required NF of the receiver should be less than 24 and 25 dB in 868/915 MHz band and 2.45 GHz band, respectively. Selectivity can be represented as third-order, second-order inter-modulation products as well as a filter requirement. The gain control range presents for receiver dynamic range [18, 20].

2. Basic Discussions of Optical Receiver:

In order to design and implement an effective networking based module for the optical communication systems we have to chart out a table with the desired parameters value that can be used to find out the behavior of the device. This task has been achieved with the desired information in the form of a table 1 as shown below.

Parameters	Target specifications	
	868/915 MHz band	2.45 GHz band
Sensitivity [dBm]	−100	−90
NF [dB]	11	15
Total gain [dB]	103	93
IIP_3 [dBm]		
@ high gain mode	−35	−32
@ low gain mode	−10	−10
IIP_2 [dBm]	12.5	10.5
Gain control range [dB]	80	70
Filter requirement	+) 10 dB rejection @ 2 MHz offset	+) 10 dB rejection @ 5 MHz offset
	+) 40 dB rejection @ 4 MHz offset	+) 40 dB rejection @ 10 MHz offset

Table 1: Summary of desired receiver specification [21]

The receiver must be able to receive signals up to-20 dBm at both band as specified in IEEE 802.15.4. Considering the minimum input signals of -110 and-100 dBm, the dynamic range of the receiver should be 90 and 80 dB for 868/915 MHz and 2.45 GHz bands, respectively, to avoid the saturation of the ADC. Other radio specifications of the multi-band RF receiver are listed in Table 1. The next step is assigning the specifications for each block. Here, the receiver is divided into two sections: RF section including LNA and down conversion mixer, and IF section including band pass filter and variable gain amplifier. This division helps a design process more convenience because the signal level at the LNA input is represented in power while it is represented in

voltage level at the mixer output. Normally, to determine the NF specification of individual block in the cascade system, Friis's equation is applied [22], we have

$$NF_{total} = NF_{RF,R_S} + \frac{NF_{IF,R_{out,RF}} - 1}{A_{P,RF}} \quad (1)$$

where $NF_{RF,Rs}$ and $A_{P,RF}$ are noise figure and available power gain of the RF section with respect to the source impedance, respectively. $NF_{IF;Rout,RF}$ is noise figure of the IF section with respect to the output impedance of RF section. The available power gain of the RF section is given by

$$A_{P,RF} = \left(\frac{R_{in,RF}}{R_S + R_{in,RF}}\right)^2 A_{v,RF}^2 \frac{R_S}{R_{out,RF}} \quad (2)$$

where Rs is the source impedance, $R_{in,RF,}$ $R_{out,RF}$, and $A_{v,RF}$ are the input impedance, output impedance and voltage gain of RF section, respectively. To calculate IIP3, the following expression is used.

$$\frac{1}{A_{IIP_3,total}^2} \approx \frac{1}{A_{IIP_3,RF}^2} + \frac{A_{v,RF}^2}{A_{IIP_3,IF}^2} \quad (3)$$

As can be seen from equations 1–3, there are a so many possible combinations of the section specification that meet the requirements. A set of specifications is specified based on our experience and the experimental results of the previous designs. Then during the design process, some of the values are revised based on the design experimental results. Therefore, authors believe that the given specifications have reached a certain optimal point for low power consumption receiver implementation. The optimization of the receiver implementation is shown in figure 4 where the requirements for each block in receiver chain are described. In 868/915 MHz band, the LNA with 2 dB NF and 28 dB maximum voltage gains are specified. Although higher gain would relax the NF requirements of the following stages, high current would be required to achieve the needed gain and linearity. 13 dB gain variable is also assigned to make sure LNA and mixer are not saturated at high RF input signal under low power consumption design. The final specifications of the individual sections are listed in Table 2 assuming the IF section will be reused for both bands [23, 25].

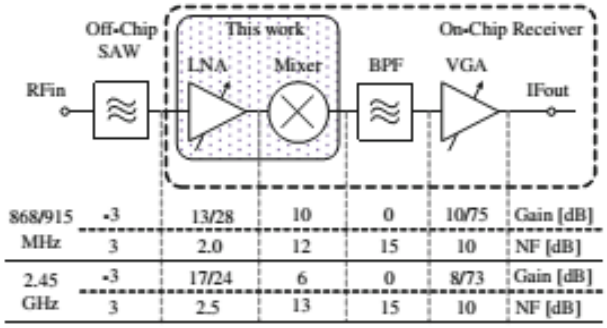

Figure 4: Receiver Architecture Methodology [26]

Parameters	868/915 MHz band		2.45 GHz Band	
	RF section	IF section	RF section	IF section
Max. voltage gain [dB]	38	75	30	73
Min. voltage gain [dB]	23	10	25	8
NF [dB]	7	20	11	20
IIP_3 [dBm]				
@ high gain mode	−15	−30	−15	−30
@ low gain mode	−8	10	−8	10
IIP_2 [dBm]	>20	>20	>20	>20
Gain control range [dB]	15	65	5	65

Table 2: Summary of RF and IF sections specifications [27]

3. CMOS Based Optical Receiver

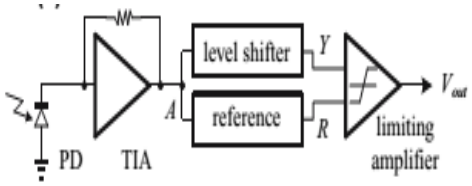

Figure 5: Block Diagram of the Optical Receiver

A CMOS based optical receiver which has been designed for the optimized operation that in turn reduce the PWD and circuit complexity for high-definition digital audio interfaces. Figure 5 shows the logical circuit of the system, consisting of a photo detector (PD), a trans-impedance amplifier (TIA), a level shifter, a replica bias circuit (reference) and a limiting amplifier. The PD and the TIA generate current and voltage signals with various logic thresholds due to the optical wave length and the sender power. However, the direct application of a fixed reference may result in PWD, especially at high speed. In order to overcome this problem, a level shifter is introduced at the receiver, which aligns different thresholds of input signals [28, 35].

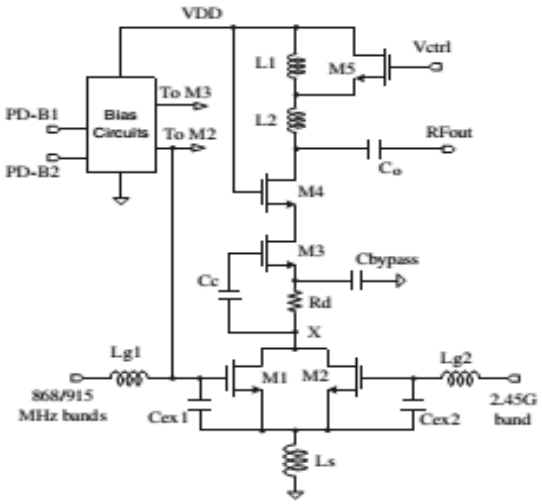

Figure 6: Schematic Arrangement of a Low Noise Amplifier Circuit

The figure 6 is a simplified schematic of the multi-band low noise amplifier (MB-LNA) that uses two-stage cascade configuration with a current reused technique. This device is highly desired in the design of the highly efficient optical transreceiver. The first stage uses a common-source topology with loading resistor R_d and the second stage adopts a cascode topology. The supply voltage of 1.8 V allows stacking three transistors since the threshold voltage, V_{th} of RF NMOS transistor in 0.18 micron CMOS technology is about 0.5 V. Two stages are ac coupled by on-chip MIM capacitor C_c. Transistors M_1 and M_2 are the LNA inputs where M_1 is for the 868/915 MHz band and M_2 is for the 2.45 GHz band. When the LNA is working in 868/915 MHz band, the PD-B1 (power down of the first band) and PD-B2 (power down of the second band) are turned ON and OFF, simultaneously, and vice verse. The advantage of this configuration is that the input matching of each band can be optimized independently. This is an important aspect since the LNA input matching network quality factor is key factor in determining the gain, noise, linearity, and sensitivity to component variations [36, 39].

4. Experimental Analysis and Result Discussions

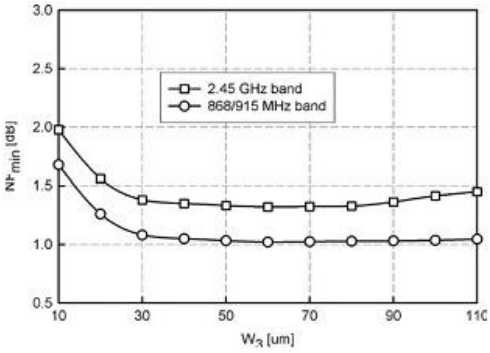

Figure 7: Simulated NF_{min} of LNA

The above figure 7 shows the an optimized plot between the noise figure and the operation of the effective CMOS device.

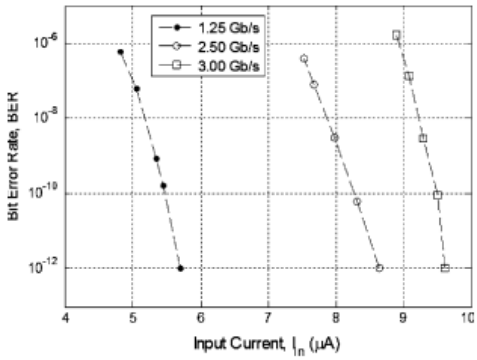

Figure 8: BER as a function of the input current and bit rate

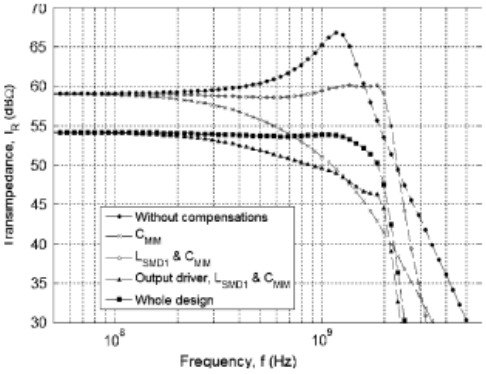

Figure 9: Frequency response obtained when frequency compensation is employed

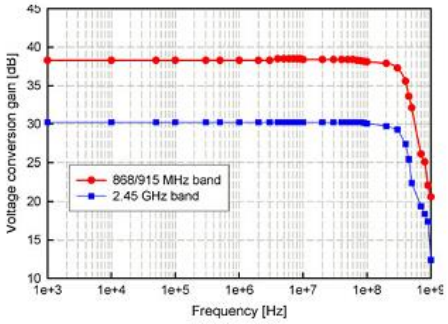

Figure10: Measured voltage conversion gain of the multi-band RF receiver

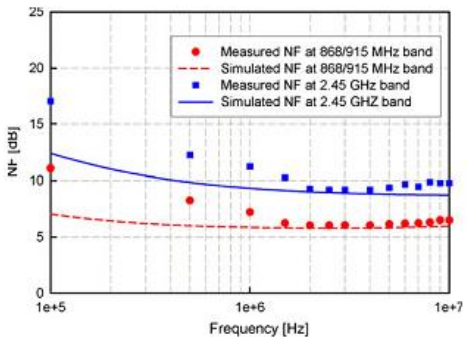

Figure 11: Measured NF of the multi-band RF receiver

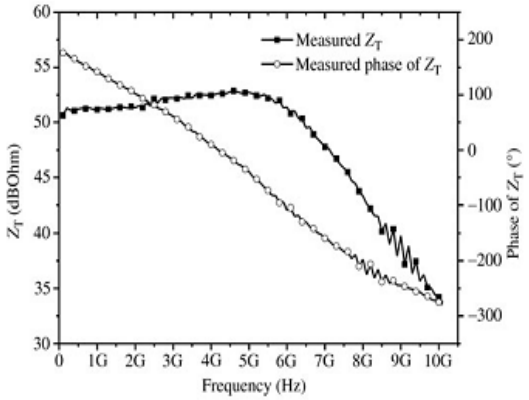

Figure 12: Measured trans-impedance gain.

The above shown figures 7-12 has been simulated and then analyzed experimentally with the desired technology. The behavior of all the required and most dominant parameters have been studied and then plotted against their relevant factors of the device such as noise figure, data bit rate, frequency response of the system, trans-impedance etc.

5. Conclusions

The integrated circuit system has been designed, simulated and demonstrated with a decent performance having free spectral range (FSR) equal to 1.5 nm at 1534 nm and very accurate wavelength modulation to 0.3 nm within 0.01 nm fluctuations for thermal actuated ring type optical switch. This desired parameters with their optimized performance has been discussed, designed and implemented with the use of CMOS 0.18 micron technology. Low power multi-band receiver implementations present significant challenges to CMOS realization.

The implemented multi-band RF receiver having 1.590.8 mm 2 die size consumes 3.0 mA under a supply voltage of 1.8 V at all bands. The single-ended input double balance down-conversion mixer is applied such that the different LNA or single-ended to differential circuitry is avoided. A good trade-off between gain, noise, bandwidth and power consumption has been achieved leading to a high performance design. More concretely, the preamplifier is based on a resistive shunt-feedback topology and employs two different frequency compensation techniques, phantom zeros and shunt peaking.

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References

[1] IEEE 802.15.4, Wireless medium access controls (MAC) and physical layer (PHY) specifications for low-rate wireless personal area networks (WPANs) 2006.

[2] Zargari, M., et al. (2004). A single-chip dual-band tri-mode cmos transceiver for IEEE 802.11a/b/g WLAN.IEEE Journal of Solid State Circuits, 39(12), 2239–2249.

[3] Zang, P., & Razavi, B. (2005). A single-chip dual-band direct conversion IEEE 802.11a/b/g WLAN transceiver in 0.18lm CMOS.IEEE Journal of Solid-State Circuits, 40(9), 1932–1939

[4] Hashemi, H., & Hajimiri, A. (2001). Concurrent dual-band CMOS low noise amplifiers and receiver architectures in Proceedings of VLSI Circuits Symp. Dig. Of Tech. Papers (pp. 247–250).

[5] Li, Z., Quintal, R., & O, K. K. (2004). A dual-band CMOS frontend with two gain modes for wireless LAN applications. IEEE Journal of Solid-State Circuits, 39(11), 2069–2073.

[6] Oh, Nam-Jin, et al. (2005). A CMOS 868/915 MHz direct conversion ZigBee single-chip radio. IEEE Communications Magazine, 43(12), 100–108.

[7] Oh, Nam-Jin, & Lee, Sang-Gug. (2005). Building a 2.4-GHz radio transceiver using IEEE 802.15.4. IEEE Circuits and Devices Magazine, 21(6), 43–51.

[8] Razavi, B. (1998). RF micro-electronics(1st ed.). New York: Prentice Hall.

[9] Nguyen, T.-K., et al. (2004). CMOS low noise amplifier design optimization techniques. IEEE Transactions on Microwave Theory and Techniques, 52(5), 1433–1442.

[10] Lee, S.-G., & Choi, J.-K. (2000). Current-reused bleeding mixer. Electronics Letters, 36(8), 696–697.

[11] Choi, J.-K., & Lee, S.-G. (2004). A 2.45 GHz CMOS up-conversion mixer design utilizing the current-reuse bleeding technique. International Journal of Electronics, 91(9), 537–550.

[12] Zolfaghari, A. (2002).Low power CMOS design for wireless transceivers (1st ed.). London: Kluwer Academic Publishers

[13] C.A. Brackett, A.S. Acampora, J. Sweitzer, G. Tangonan, M.T. Smith, W. Lennon, K.C. Wang, and R.H. Hobbs, "A scalable multi−wavelength multihop optical network: A proposal for research on all−optical networks", J. Lightwave Technol.11, 736–753 (1993).

[14] K. Okamoto, K. Takiguchi, and Y. Ohmori, "16−channel optical add/drop multiplexer using silica−based arrayed waveguide gratings", Electron. Lett.31, 723–724 (1995).

[15] H. Li, C. Lee, W. Lin, L.S. Didde, Y.J. Chen, and D. Stone, "8 wavelength photonics integrated 2×2 WDM cross−connect switch using 2×N phased−array waveguide grating (PAWG) multi/de-multiplexers", Electron. Lett.33, 592–594 (1997).

[16] C.R. Doerr, L.W. Stulz, M. Cappuzzo, E. Laskowski, A. Paunescu, L. Gomez, J.V. Gates, S. Shunk, and A.E. White, "40−wavelength add−drop filter", IEEE Photonic. Techn. L. 11, 1437–1439 (1999).

[17] M. Okuno, A. Sugita, T. Matsunaga, M. Kawachi, Y. Ohmori, and K. Katoh, "8×8 optical matrix switch using silica−based planar lightwave circuits", IEICE T. Electron. E76−C, 1215–1223 (1993).

[18] M. Okuno, K. Kato, Y. Ohmori, M. Kawachi, and T. Matsunaga, "Improved 8×8 integrated optical matrix switch using silica−based planar lightwave circuits", J. Lightwave Technol.12, 1597–1606 (1994).

[19] T. Goh, A. Himeno, M. Okuno, H. Takahashi, and K. Hattori, "High extinction ratio and low−loss silica−based 8×8 thermo-optic matrix switch", IEEE Photonic. Tech. L. 10, 358–360 (1998).

[20] T. Goh, M. Yasu, K. Hattori, A. Himeno, M. Okuno, and Y. Ohmori, "Low−loss and high−extinction−ratio silica−based strictly non blocking 16×16 thermo-optic matrix switch", IEEE Photonic. Tech. L.10, 810–812 (1998).

[21] J.C. Liou and F.G. Tseng "Three−dimensional architecture of multiplexing data registration integrated circuit for large array ink jet print head", J. Imaging Sci. Techn.52, 1–7 (2008).

[22] K. Moriwaki, M. Abe, Y. Inoue, M. Okuno, and Y. Ohmori, Tech. DigestOFC95, 211–212, paper WSI (1995).

[23] J.E. Ford, V. Aksyun, D. Bishop, and J. Walker, "Wavelength add−drop switching using tilting mirrors", J. Lightwave Technol.17, 904–911 (1999).

[24] C. Pu, L. Lin, E. Goldstein, and R. Tkach, "Client−configurable eight channel optical add/drop multiplexer using micromachining technology", IEEE Photonic. Tech. L. 12, 1665–1667 (2000).

[25] N.A. Riza and S. Yuan, "Reconfigurable wavelength add drop filtering based on a Banyan network topology and ferroelectric liquid crystal fiber−optic switches", J. Lightwave Technol.17, 1575–1584 (1999).

[26] W. Lin, H. Li, Y.J. Chen, M Dagenais, and D. Stone, "Novel dual−channel−spacing WDM multi/de-multiplexers based on phased−array waveguide grating", Photon. Tech. L.8, 1501(1996).

[27] J.C. Liou and F.G. Tseng "An intelligent multiplexing control thermal actuated optical packet switch", Photonics in Switching(PS), Optical Switches and Routing Device D−06−2, 1–4 (2008).

[28] J.C. Liou and F.G. Tseng "Integrated control circuit for thermally actuated optical packet switching", Proc. IASTED Int. Conf. on Wireless and Optical Communications(WOC), 213–218 (2008).

[29] YU Chang-liang, MAO Lu-hong and XIAO Xin-dong, Journal of OptoelectronicsgLaser20, 432 (2009). (in Chinese)

[30] XIAO Xin-dong, MAO Lu-hong, YU Chang-liang, ZHANG Shi-lin and XIE Sheng, Journal of Opto-electronics g Laser 21, 520 (2010). (in Chinese)

[31] J. Savoj and B. Razavi, A 10-Gb/s CMOS Clock and Data Recovery Circuit, Symp. on VLSL Circuits Dig. of Tech. Papers, 136 (2000).

[32] Pellerano S., Levantino S., Samori C. and Lacaita A. L., IEEE Journal of Solid-State Circuits 39, 37 (2004).

[33] Yan Dan-Lei, Integrated Circuits for Wideband Communication and Wireless Sensor Networks, RFIT, Integrated Circuits for Wideband Communication and Wireless Sensor Networks, Proceedings. IEEE International Workshop, 219 (2005).

[34] S. K. Singh, T. K. Bhattacharyya and A. Dutta, Fully Integrated CMOS Frequency Synthesizer for ZigBee Applications, 18th International Conference 780 (2005).

[35] Krishnapura N. and Kinget P. R., IEEE Journal of SolidState Circuits 35, 1019 (2000).

[36] Shu K. and Sanchez-Sinencio E., IEEE Journal of Solid-State Circuits38, 866 (2003).

[37] Yang C. Y., Dehng C. K., Hsu J. M. and Liu S. I., IEEE Journal of Solid-State Circuits 33, 1568 (1998).

[38] J. N. Soares Jr. and W. A. M. Van Noije, IEEE J. Solid-State Circuits34, 97 (1999).

[39] Tiwari Rajinder, Singh R. K. "A Real Time Based Intelligent System Designed for the Process Automation & Control Applications" European Journal of Academic Essays 1(2): 40-47, 2014 ISSN: 2183-1904, www.euroessays.org

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