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High-Efficiency Switched-Capacitor-Based Resonant Converter Fed Dc Drive

C.Pratheeba*, G.Praveen Santhosh Kumar **& A.Karthikeyani***

Assistant Professor, Department of Electrical and Electronics Engineering, Vivekanandha College of Engineering for Women,
*****Assistant Professor, Department of Electrical and Electronics Engineering, Muthayammal Engineering College,***
******Assistant Professor, Department of Electrical and Electronics Engineering, Vivekanandha College of Engineering for Women,***

ABSTRACT:

This paper presents operating performance of a switched-capacitor-based resonant converter (SCRC) using a phase-shift control method. The proposed phase-shift control realizes zero-voltage switching operation, and thus achieves high conversion efficiency. A theoretical analysis shows that the SCRC can reduce its inductor volume compared with a conventional buck converter when the output voltage range is within 19%–81% of its input voltage. Experimental results verify the operating characteristics of the proposed method and show the improved conversion efficiency of more than 99%.

Index Terms: Inductor volume, switched capacitor converters (SCC), voltage regulation, zero-voltage switching (ZVS).

I. INTRODUCTION:

Various types of dc–dc converters are widely applied to dc power supplies, battery chargers, voltage regulators for photo volics and fuel cells, etc. Most of the dc–dc converters include magnetic components, such as inductors and/or transformers for stepping up/down or smoothing the current/voltage. The magnetic components, however, occupy a large volume and weight in the converter, and also produce non negligible losses.

Switched-capacitor converters (SCC) [1]–[3] have been used as a simple and low-cost dc–dc converter in small power applications. The advantage of the SCC is its small volume because it needs no inductor or transformer. Recently, resonant power converters consisting of an SCC and a small-rated resonant inductor have been proposed to reduce the switching loss and electromagnetic interference (EMI) [4]. The resonant converters have an additional small inductor connected in series with the switched capacitor, leading to soft-switching operation with a low-switching loss. The inductor used in the resonant converters is much smaller than that in a conventional buck converter because the converter mainly stores the electrical energy in the switched capacitor similarly to the SCC. As a consequence, the resonant converter seems to be more suitable for a high-power application than the SCC [5]–[8]. A circuit configuration using synchronous rectification has been proposed to reduce the conduction loss [9] and the mitigation of the conducted EMI is also reported in [10]. The resonant converter has many similarities with SCCs in its circuit topology and operating behaviour.

Therefore, this paper refers to the resonant converter, which consists of an SCC and a small-rated resonant inductor inserted in series with the switched capacitor as “switched-capacitor-based resonant converters (SCRCs).”

A basic SCRC has an output voltage, which is double or half of the input voltage. An expanded SCRC equipped with n capacitors can convert the input voltage Vin to an output voltage vout = Vin/n in a step-down, or vout = nVin in a step-up configuration [6]–[8], [11], [12]. The switching devices are operated by feeding periodic gate signals with a fixed duty cycle and frequency. Then, the conversion ratio (vout/Vin) is almost fixed at a particular value depending on the number of the series connected capacitors. However, this control method has a difficulty in the output voltage regulation. The output voltage error is caused by the input voltage fluctuations, and the voltage drops in the switching devices and the passive components. Some feedback control methods have been proposed to regulate the output voltage by adjusting the blanking time [13], the switching frequency [14], and the duty cycle [15]. These methods make it possible to decrease the output voltage from the particular value. However, these methods may cause increased switching and ON-state losses due to its hard-switching operation and a large peak current, which lead the conversion efficiency to decline.

The authors have proposed a new voltage-regulation method for SCRCs, which adjusts a phase-shift angle. The control method realized a current amplitude control by adjusting the phase difference among gate signals. The method makes the SCRC not only decrease the output voltage, but also increase it continuously, resulting in a more flexible voltage regulation. The SCRC can continue zero-voltage switching (ZVS) even if the output voltage is changed. The basic characteristics have been analyzed under the condition that the SCRC is used as a dc-capacitor voltage-balancing circuit for a five-level diode clamped inverter [16].

This paper presents the output voltage regulation characteristics of an SCRC using the phase-shift control. The principle of the phase-shift control is explained as well as the mechanism of the ZVS operation. The theoretical analysis shows that the inductor volume of the SCRC is smaller than that of the buck converter in an output voltage range from 19% to 81% of the input voltage. Experimental results verify the operation characteristics of the proposed control method and show the improved conversion efficiency of more than 99%.

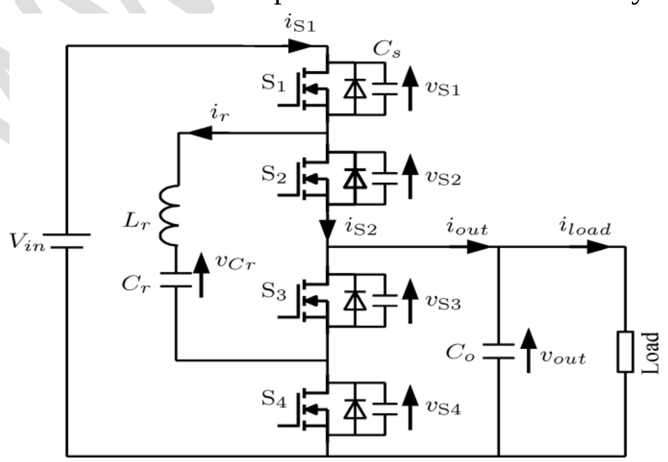

Fig. 1. Switched-capacitor-based resonant converter.

II. SWITCHED-CAPACITOR-BASED RESONANT CONVERTERS

A. Circuit Configuration

Fig. 1 shows a circuit configuration of a SCRC. This circuit acts as a step-down converter and feeds the output voltage vout to a load. The SCRC consists of two half-bridge inverters with four switching devices S1–S4 and a series resonant circuit Lr and Cr. Addition of the small inductor Lr is the difference from a conventional SCC in the circuit configuration, resulting in a great suppression of spike currents, power losses, and EMI issues. The configuration is the same as that in [9] except for addition of four snubber capacitors Cs .

B. Phase-Shift Control

Fig. 2 shows switching modes in the SCRC. Four switching modes exist because the SCRC consists of two half-bridge inverters. Fig. 3 illustrates the switching sequence and waveforms of the phase-shift control. These waveforms are drawn under the condition of a power flow from the voltage source Vin to the load. In addition, the output voltage is assumed to be vout = Vin/2. The switching frequency fSW should be set at a higher frequency than the resonant frequency of the series resonant circuit fr (=ωr /(2π) = 1/(2π √ LrCr)). In this condition, the resonant circuit acts as an inductive impedance, and the amplitude of ir is controllable by the phase difference between the two half-bridge inverters.

The reference signal is a square wave with a period TSW (=1/fSW) and a 50% duty cycle. The gate signals of S1 and S2 lead from the reference signal by TS /2, while S3 and S4 lag by TS /2. Therefore, mode 2 or 4 appears for a short duration of TS between mode 1 and 3. Since the resonant-capacitor voltage vCr is Vin/2 on average, ±Vin/2 is applied across the resonant inductor Lr during mode 2 and 4. As a result, the resonant current ir has a trapezoidal waveform. Since the output current iout is the rectified current of ir , the average value of iout is proportional to the amplitude of ir . When S1 and S2 lag from S3 and S4 (TS < 0), the SCRC regenerates an amount of power from the load to Vin.

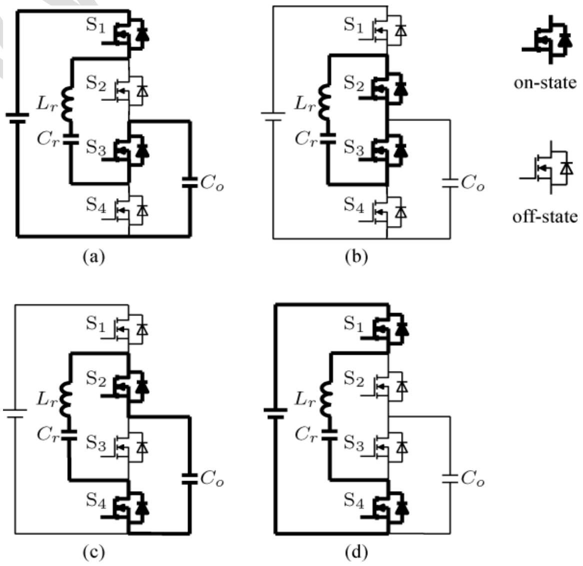

Fig. 2. Four switching modes in the SCRC. (a) Mode 1. (b) Mode 2.(c) Mode 3. (d) Mode 4.

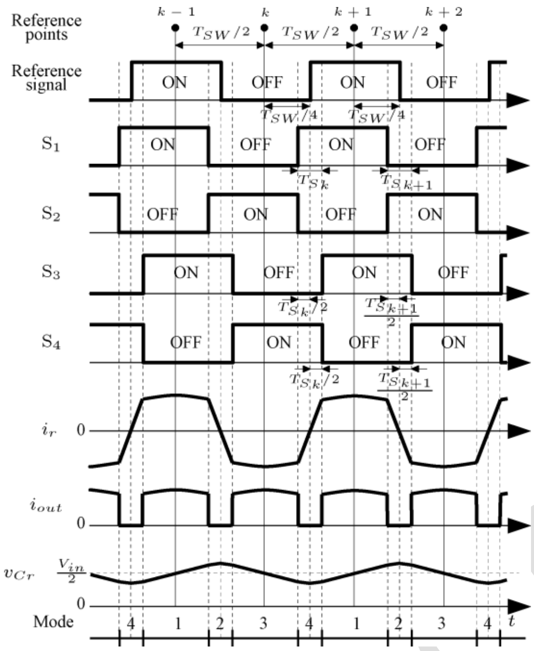

Fig. 3. Switching sequence in the phase-shift control.

The conventional control methods in [13]–[15] cannot regenerate any power when vout < Vin/2, and the direction of the power flow depends only on the relation between the input and output voltages. The phase-shift control enables the SCRC to control iout bidirectionally by adjusting the phase-shift time TS regardless of vout .

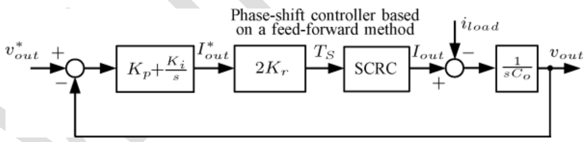

Fig. 4. Block diagram of the output voltage controller.

The average output current Iout can be expressed as follows:

$$I_{out} = \frac{2V_{in}\,\sin\omega_r T_S \,\sin\omega_r T_s}{\omega_r^2 L_r T\,\left(1+\cos\omega_r T_S+\cos\omega_r T_s+\cos(\omega_r T_{SW}/2)\right)} \qquad (1)$$

where Ts = TSW/2 − |TS |. A first-order approximation of (1) around TS = 0 yields

$$I_{out} \approx \frac{V_{in}\tan(\omega_r T_{SW}/4)}{Z_r T_{SW}}\,T_s \qquad (2)$$

where Zr is the characteristic impedance of the resonant circuit, given by Zr =√Lr/Cr .

C. Control Scheme

Fig. 4 shows the block diagram of the output voltage controller for the SCRC. The output voltage vout can be regulated by applying voltage feedback with proportional and integral (PI) gains. The reference of the averaged output current I*out is given as follows:

$$I^*out(S) = \left(Kp + \frac{Ki}{s}\right)\{V^*out(s) - Vout(s)\} \quad (3)$$

where Kp is a proportional gain, Ki is an integral gain, and V *out(s) is a reference of the output voltage. The proposed feedback control realizes an accurate voltage regulation in spite of the input voltage fluctuation and/or voltage drops in devices. According to the relation in (2), TS is calculated from the reference value of the output current I*out as follows:

$$TS = 2KrI^*out \quad (4)$$

where Kr is a control gain depending on circuit parameter, given by

$$Kr = \frac{ZrTSW}{2Vin \tan(\omega rTSW/4)}.$$

This control method simply decides TS to be in proportion to the I*out, and do not need any current sensor.

III. SOFT SWITCHING

A. Soft-Switching Operation

Fig. 5 shows drain-to-source voltages vS1–vS4 and drain currents iS1–iS4 of the MOSFETs in a switching transition from mode 1 to mode 3. The phase-shift control makes the SCRC accomplish ZVS operations by using additional snubber capacitors Cs (Cs _ Cr) or the parasitic output capacitance Coss (Coss _ Cr) of the MOSFET. The .transition is divided into six states from A to F.

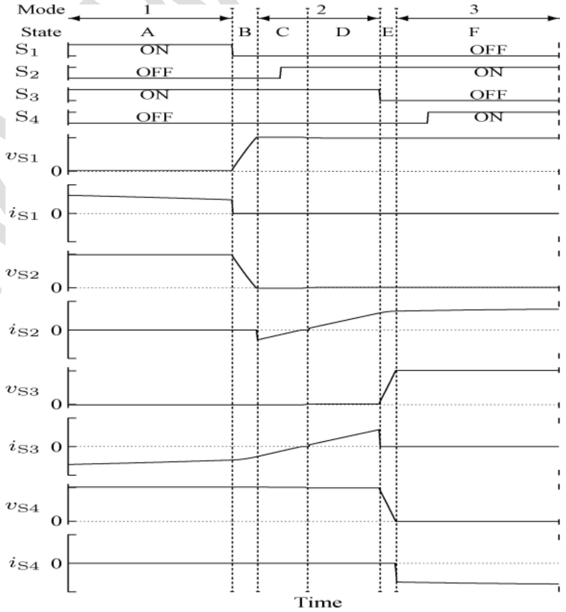

Fig. 5. Voltage and current waveforms of the switching devices in case of a ZVS operation.

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Fig. 6 depicts the six switching states. During state A, forward current flows through S1 and reverse current flows through S3 . The snubber capacitor voltage vS1 equals zero in this state. The state B starts when S1 is turned OFF. The inductor current commutates from S1 to Cs1 and Cs2 , and charges and discharges them. The voltage across S1 gradually increases, and ZVS is achieved in this turn-OFF transition. After Cs2 is fully discharged, the diode in S2 starts to conduct, and the state is changed to C. During the state C, the current ir gradually decreases. The current in S2 and S3 automatically commutates from the diodes to the corresponding MOSFETs when the polarity of ir changes. The forward current increases in S2 and S3 during the state D. The diodes in S2 and S3 turn OFF and the corresponding MOSFETs can be turned ON with zero-voltage zero-current switching (ZVZCS) because the snubber capacitor voltages vS2 and vS3 are zero in this state. The MOSFET in S3 is turned OFF at the beginning of state E. The inductor current commutates from S3 to Cs3 and Cs4, and charges and discharges them. The MOSFET in S3 is turned OFF with ZVS. After Cs4 is fully discharged, the diode in S4 starts to conduct and the state becomes F.

The energy stored in Cs does not cause any power loss when the inductor current ir discharges Cs before the turn-ON transition of the corresponding MOSFETs. The other transition from mode 3 to mode 1 also achieves ZVS due to the symmetric operation. Therefore, all switching devices can be turned OFF with ZVS and turned ONwith ZVZCS in the phase-shift control. This switching operation significantly reduces the switching loss and allows us to use low ON-state resistance MOSFETs with a relatively large output capacitance.

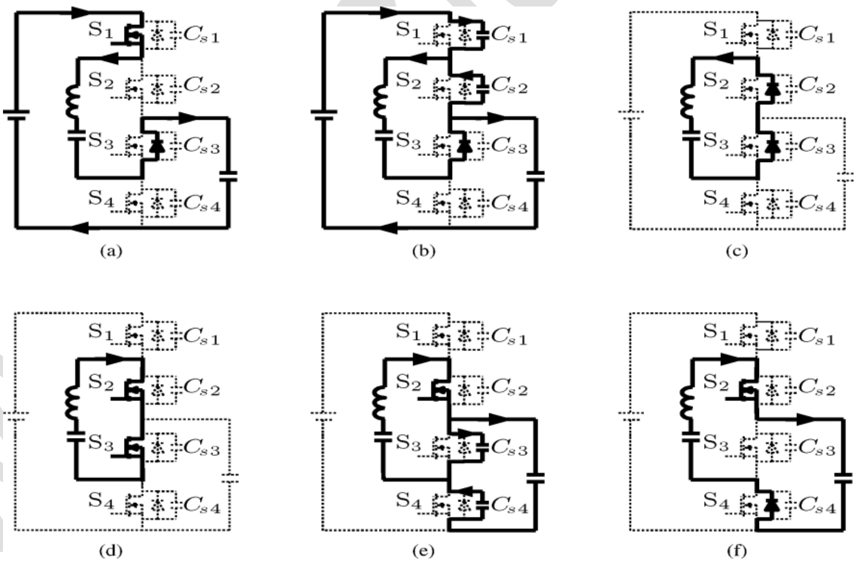

Fig. 6. Transition of the current path fromMode 1 to 3. (a) State A. (b) State B. (c) State C. (d) State D. (e) State E. (f) State F.

.B. Requirement for the ZVS Operation

If the inductor current ir is small during the commutation, the SCRC cannot fully discharge Cs2 before the turn-ON transition of S2 . In this case, the energy remained in Cs2 is consumed in the MOSFET in S2 during the turn-ON process. The snubber capacitor Cs1 is also suddenly charged to Vin/2. Then, a spike current flows through the MOSFET in S2 , and produces a loss.

The snubber capacitor of S2 is discharged by the inductor current ir and its voltage vS2 decreases from Vin/2 during the state B in Fig. 5. Assuming that the capacitance of Cs is much smaller than that of Cr , the resonance between Lr and Cs occurs during the stateB[17], and ir (t) becomes a sinusoidal waveform given by

$$i_r(t) = I_D \cos \omega_s t \qquad (5)$$

where ID is the current at the beginning of the state B, and ωs =1/√2LrCs . The snubber capacitor voltage vS2 is represented by

$$v_{S2}(t) = \frac{V_{in}}{2} - \frac{1}{2C_s}\int i_r(\tau)\,d\tau. \qquad (6)$$

Substituting (5) into (6)

$$v_{S2}(t) = \frac{V_{in}}{2} \;\; I_D\sqrt{L_r/2C_s}\,\sin \omega_s t. \qquad (7)$$

Note that the snubber capacitor voltage vS2 is kept at zero after the capacitor is fully discharged. When ir is too small to discharge it completely, vS2 reaches its minimum value at t = π/(2ωs). The blanking time should be set to TD = π/(2ωs) to minimize the loss caused by short circuits of Cs. From (7), the requirement for ZVS operation is summarized as follows:

$$I_D \geq V_{in}\sqrt{(C_s/2L_r)} \quad . \qquad (8)$$

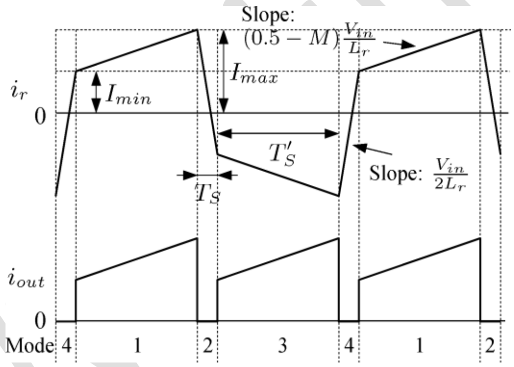

Fig. 7. Current waveforms of the SCRC in case of 0 < M ≤ 0.5.

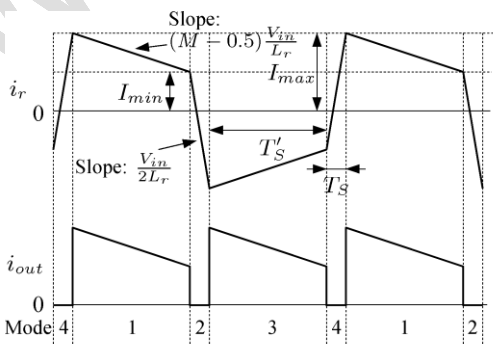

Fig. 8. Current waveforms of the SCRC in case of 0.5 < M ≤ 1.

Figs. 7 and 8 show waveforms of the resonant current ir and the output current iout , when the output voltage vout is lower than Vin/2 and higher than Vin/2, respectively. Here, the voltage conversion ratio is defined asM = vout/Vin . Since the resonant capacitor voltage vCr is equal to Vin/2 on average, Vin/2 is applied to Lr in mode 2 and 4. Therefore, the inductor current is increased or decreased with dir /dt = ±Vin/(2Lr) in mode 2 and 4. In mode 1 and 3, ±(Vin/2 − vout) is applied to Lr , and the slope of ir is dir /dt = ±(0.5 −M)Vin/Lr . Therefore, Lr is a factor to decide these slopes. The decrease of Lr increases the slopes of ir , resulting in the increase of Imax and the decrease of Imin. The requirement for ZVS in (8) can be represented by

Imin ≥ VinCs2Lr. (9)

Lr should be designed to satisfy the requirement in (9) in the main operating range.

IV. ENERGY STORED IN THE INDUCTOR

When 0<M ≤ 0.5, a geometric analysis in Fig. 7 yields
dir/ dt= Vin/2Lr= (Imax + Imin)/TS(in mode 2, 4) (10)

dir/dt=((0.5 −M))/VinLr=(Imax – Imin)/TS(in mode 1, 3). (11)

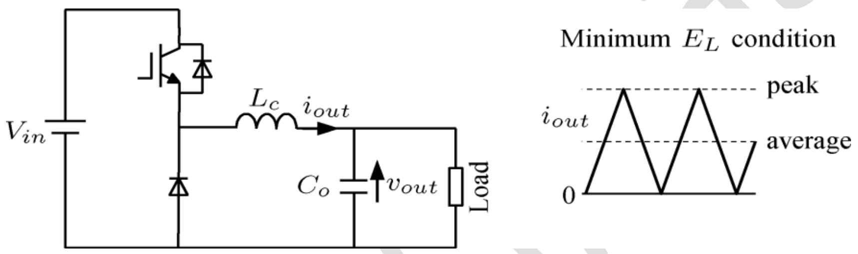

Fig. 9. Buck converter.

The average output current Iout is expressed as follows:

Iout = (Imax + Imin)TS (12)
2(TS + T_S) .

The maximum energy stored in the inductor Lr is given by

EL =(1/2)Lr I2max. (13)

The minimum value of EL and the inductance to minimize EL can be derived from (10)–(13) as follows:

EL min =1 − 2M VinIout (0<M ≤ 0.5) (14)
4• fSW

Lr = 1 1 − 2M VinIout (0<M ≤ 0.5). (15)

32• (1 −M)2• fSW

In general, Vin and fSW are constants decided by the circuit specifications, and M and Iout are also fixed under a rated load condition.

The similar analysis in 0.5<M ≤ 1 gives EL min and Lr as follows:

EL min =−1 + 2M VinIout (0.5<M ≤ 1) (16)
4 fSW

Lr =1 −1 + 2M VinIout (0.5<M ≤ 1). (17)
32• (1 −M)2• fSW

Fig. 9 shows a buck converter. The energy stored in the inductor Lc becomes minimum if Lc is designed to make the peak value of iout equal to twice the average value [18]. In such condition, EL min is given as follows:

EL min = M(1 −M)VinIoutfSW. (18)

The maximum energy stored in the inductor shown in (14), (16), and (18) are plotted in Fig. 10 by the voltage conversion ratio M. The SCRC is smaller in the stored energy than the buck converter in a range of 0.19<M <0.81, and the minimum value of EL min appears at M = 0.5 in the SCRC. Since inductor volume is generally almost proportional to the energy stored in the inductor, the SCRC has advantage in inductor volume around M = 0.5. For example, in case that M is adjusted in a range of 0.45 <M < 0.55, the SCRC is ten times smaller in inductor volume than the conventional buck converter.

V. EXPERIMENTAL RESULTS:

The proposed methods were evaluated using a 2.8-kW experimental circuit. Power MOSFETs (IXYS, HiPerFET, IXFN130N30) were used as the switching devices and they were operated at 20 kHz. External snubber capacitors Cs were not connected because the

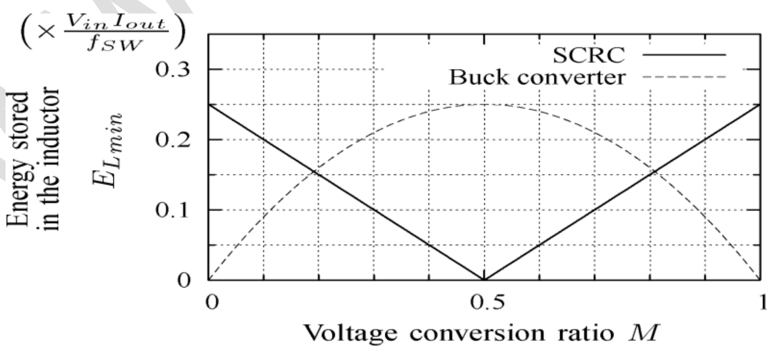

Fig. 10. Relationship between the voltage conversion ratio and the energy stored in the inductor EL min , shown in (14), (16), and (18).

parasitic output capacitance (Coss = 2.7 nF at VDS = 25 V) was large enough to achieve soft switching. The circuit parameters are summarized in Table I. The inductor Lr is designed to realize soft-switching operation in a range of $0.46 \leq M \leq 0.54$ (±8 % in the output voltage). The inductor Lr is twice as large as the theoretical value 12.2 μH given by (15) and (17) to realize the soft-switching

TABLE I PARAMETERS OF THE EXPERIMENTAL CIRCUITS

Input voltage	V_{in}	400 V
Output voltage	V_{out}	184–216 V
Voltage conversion ratio	$M = V_{out}/V_{in}$	0.46–0.54
Output current	I_{out}	14 A
Output capacitor	C_o	2,000 μF
Resonant inductor Rated peak current	L_r	27 μH 22 A
Resonant capacitor Rated voltage/current	C_r	$4.7 \times 2 = 9.4$ μF 630 V, 24 A
Snubber capacitor	C_s	not connected
Switching frequency	f_{SW}	20 kHz

requirement in (9) in the rated operating range. The resonant frequency of the resonant circuit has to be less than 20 kHz because it should operate as an inductive impedance in the phase-shift control. Therefore, Cr has to be set to more than 2.3 μF from the requirement of the resonant frequency. In addition, Cr should also satisfy the requirement of its ripple current rating. In the experiments, two 4.7-μF capacitors (rated ripple current: 12 A) were connected in parallel and Cr was set to 9.4 μF in order to handle the output current of 14 A.

Fig. 11 is the photograph of the resonant circuit used in the following experiments. Film capacitors were used for the resonant capacitor Cr and a ferrite core inductor was used for the resonant inductor Lr . The volume of the capacitors and inductor were 87 cm3 (cylindrical, diameter: 3.5 cm, length: 4.5 cm, and two pieces) and 27 cm3 (3.3 cm × 3.3 cm × 2.5 cm), respectively. The maximum energy stored in the inductor is only 6.5 mJ. On the other hand, a 2.8-kW buck converter has to store the magnetic energy more than 70 mJ in the inductor as presented in (18). Therefore, SCRCs can reduce the volume of the inductor by a factor of ten compared with buck converters.

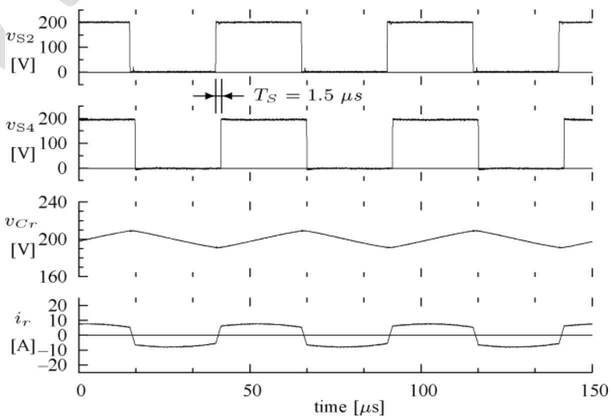

Fig. 11. Components for the resonant circuit.

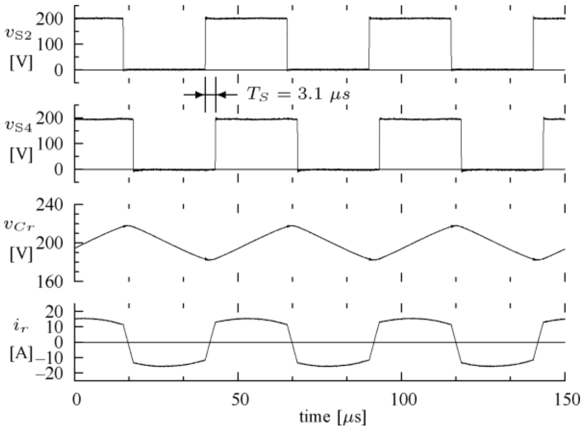

*Fig. 12. Experimental waveforms of a full-load (2.5 kW) condition whenV *out = 200 V and Iload = 12.5 A.*

A. Current Control Characteristics

Fig. 12 shows the experimental waveforms under a full-load (2.5 kW) condition when the voltage reference was set at V*out = 200 V. The control scheme shown in Fig. 4 was applied. The phase of S1 and S2 led to the phase of S3 and S4 by TS =3.0 µs, and the average output current was 12.5 A. The ZVS operation was realized, and switching surge was very small.

Fig. 13 shows the experimental waveforms under a half-load (1.3 kW) condition when V*out = 200 V. The phase-shift time TS decreased to 1.5 µs according to a reduction of the output current to 6.5 A. Therefore, the output current can be controlled by the phase-shift time.

Fig. 14 shows the experimental waveform of the drain-to source voltages and drain currents of S1 and S2 . Each MOSFET has parasitic output capacitance Coss and it operates as a snubber capacitor. Fig. 14(a) shows the soft-switching operation in 2.5 kW conversion. The drain currents iS1 and iS2 show the charging/discharging current of the Coss during the state B, where Coss of S1 was

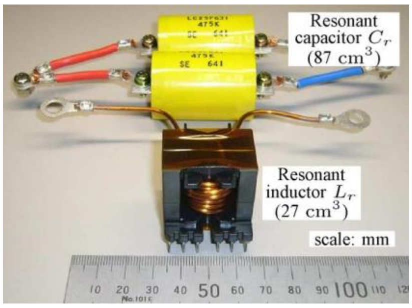

Fig. 13. Experimental waveforms of a half-load (1.3 kW) condition whenV ∗out = 200 V and Iload = 6.5 A.

charged and Coss of S2 was discharged. Total energy related to the charge/discharge of Coss was almost zero. Fig. 14(b) shows the soft-switching limit in 0.5 kW conversion. Coss were charged/discharged slowly during the state B, and the state C disappears. Fig. 14(c) shows the hard switching operation in 0.2kWconversion. The charge/discharge of Coss did not finish during the state B. Then, they are charged/discharged immediately in the state D, resulting in an increase of the switching loss.

B. Voltage Regulation Characteristics

Figs. 15 and 16 are the experimental waveforms of the 2.5 kW conversion. In Fig. 15, the output voltage Vout was regulated at 185 V by the control scheme shown in Fig. 4, and the output current was 13.5 A. In Fig. 16, Vout was regulated at 215 V and the output current was 11.6 A. The voltage vout applies to S3 and S4 , and Vin − vout applies to S1 and S2 . The average of these voltages Vin/2 (=200 V) is the average of the resonant capacitor voltage vCr, which is constant regardless of the output voltage Vout .

Fig. 17 shows the characteristics of the output voltage regulation under different load conditions when the output voltage reference V*out was set to 185, 200, and 215V. The output voltage was well regulated an included almost no error in all operating range. A conventional SCRC without voltage feedback has poor voltage regulating performance for a wide load range. The proposed phase-shift control method can eliminate the steady-state error because it is equipped with the integral gain in the voltage feedback loop.

C. Efficiency and Power Losses

Fig. 18 shows the experimental circuit used for the efficiency measurement [19]. Another SCRC was duplicated with the same devices as the target SCRC and connected to the target SCRC in parallel. The duplicated SCRC operates to regenerate the power from Co to Cin when there is power flowing inside the system. The power consumed in the two converters was fed from the dc power supply Vin . A four-channel power meter (HIOKI 3390) was attached to the system, and measured the input power Pin ,the output power Pout , the regenerated power Preg.

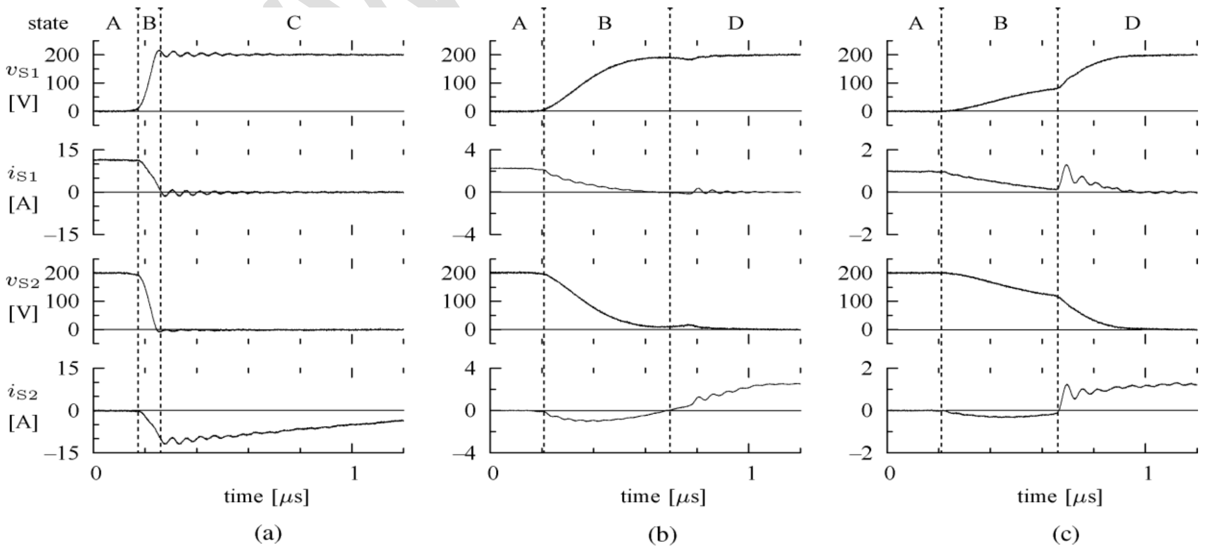

Fig. 14. Drain-to-source voltages and drain currents of S1 and S2 (a) Soft switching (2.5 kW). (b) Soft-switching limit (0.5 kW). (c) Hard switching (0.2 kW).

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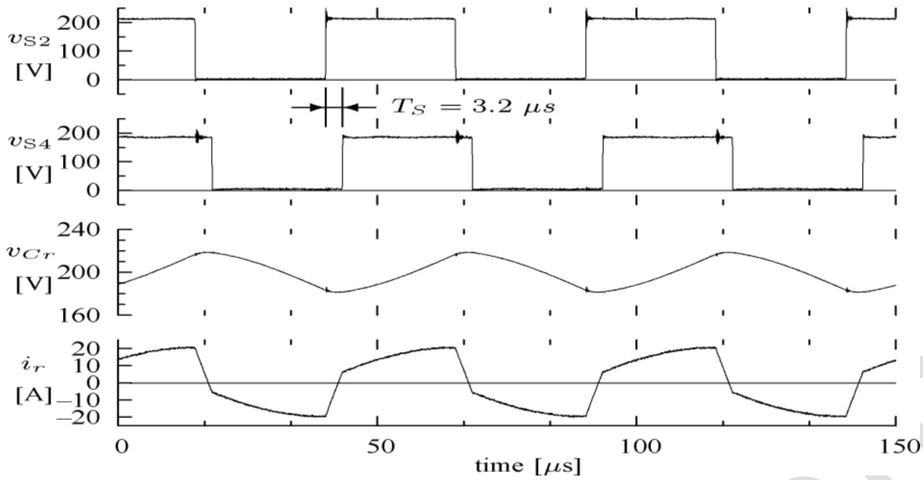

*Fig. 15. Experimental waveforms of 2.5 kW conversion when V*out = 185 V and Iload = 13.5 A.*

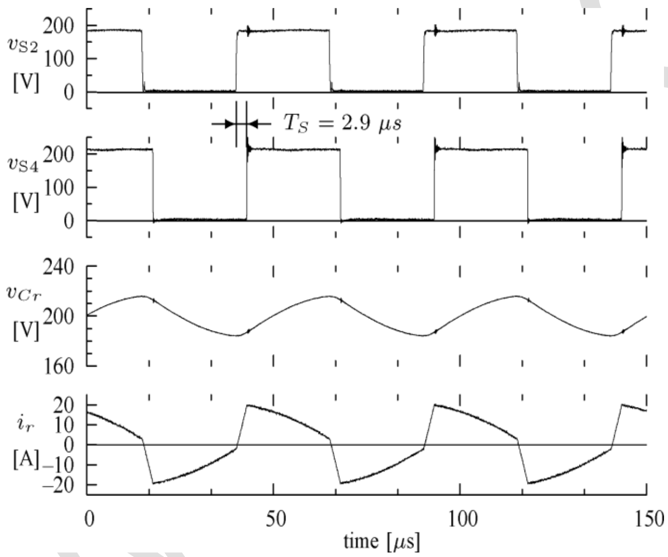

*Fig. 16. Experimental waveforms of 2.5 kWconversion when V *out = 215 V and Iload = 11.6 A.*

out = 215 V and *I*load = 11.6 A.

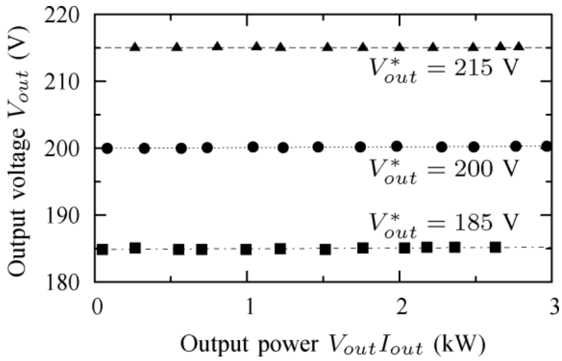

Fig. 17. Output voltage regulation characteristics under different load conditions.

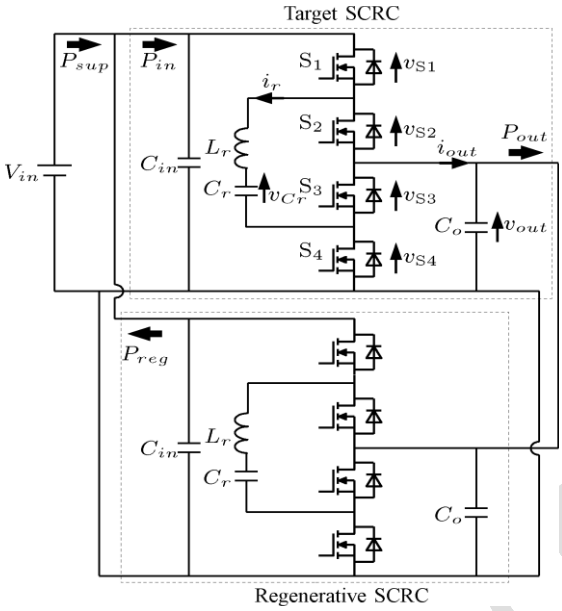

***Fig. 18. Experimental circuit used for the efficiency measurement*.**

Fig. 19 shows the measured power loss. The power loss in the target SCRC can be calculated as Pin − Pout . The total loss in the target SCRC and the regenerative SCRC is Pin − Preg .

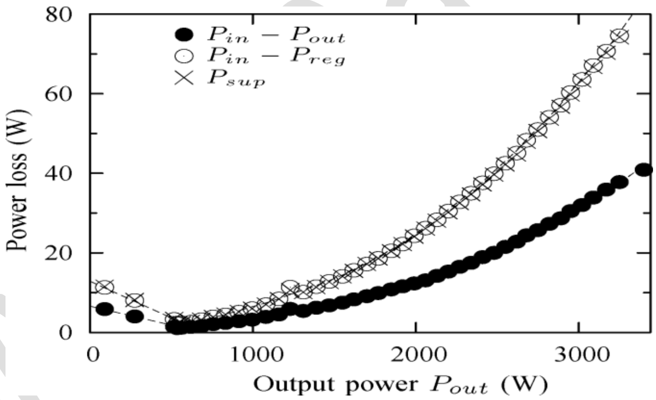

Fig. 19. Power loss in the SCRC.

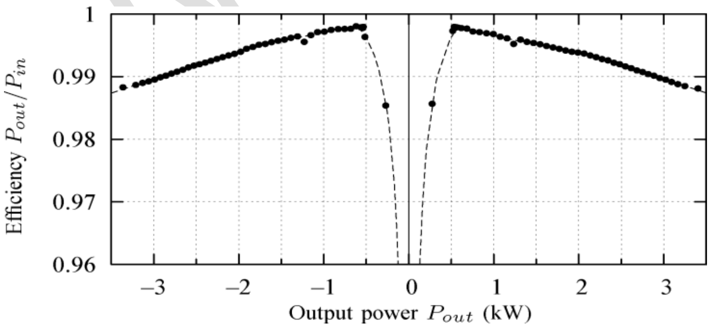

Fig. 20. Conversion efficiency at Vout = 200 V.

Both of them are plotted along with Psup. Difference between Pin − Preg and Psup was less than 0.5 W. Thus, it is expected that the error in the loss measurement is also about 0.5 W.

Fig. 20 shows the conversion efficiency in difference load conditions. The output voltage was regulated as Vout = Vin/2= 200 V, and the output current Iout was adjusted. The negative power means the reverse power flow from the output side to the input side. The efficiency was calculated as Pout/Pin , and it was more than 99% in a range from 10% to the full load. Fig. 21 shows the analytical and measured losses. The MOSFET ON-state loss is calculated based on the ON-state resistance in its data sheet. The loss caused by short circuits of Cs is estimated based on the output capacitance in the MOSFET's data sheet. The ON-state loss and output capacitance loss in the MOSFET are calculated based on the ON-state resistance in its data sheet. The loss in the resonant inductor, resonant capacitor, and wires connecting the components are calculated based on their impedance measured by an LCR meter. When the output power is less than 600W, the resonant current is too small to keep soft-switching operation. Therefore, the output capacitance loss is dominant. The soft switching is achieved when the output power is greater than 600 W, where the output current is Iout = 600W/200 V = 3.0 A. The range of the soft switching can be derived as Imin ≥ 2.8 A from (9), and it almost matches with the experimental result. The ON-state loss of the MOSFET is 40% of the total loss. The inductor loss is only 20% of the total loss because its volume is quite small. The loss in Cr is 0.2Wat 2.8 kW output, and thus, it is negligible. The difference between the measured and calculated losses is assumed to be switching losses.

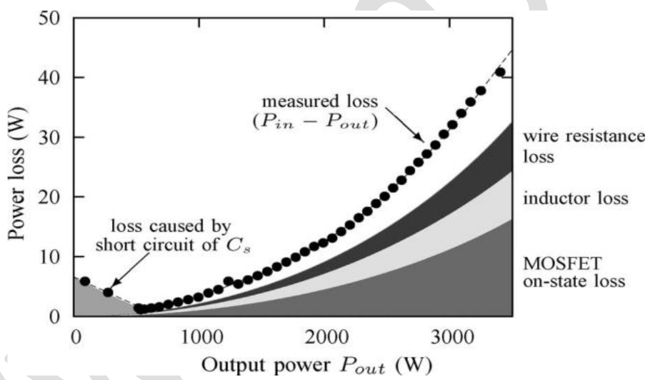

Fig. 21. Classified power losses in the SCRC.

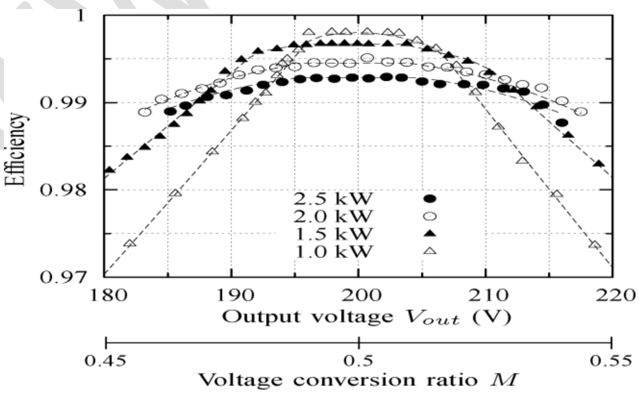

Fig. 22. Conversion efficiency against the output voltage.

Fig. 22 shows the conversion efficiency when the output voltage was changed in a range of 200 ± 16 V (M = 50 ± 4%). The efficiency was maintained to 99% in all range when the conversion power is 2.5 and 2.0 kW. The reduction of the transferred power limits the voltage range available to achieve soft switching. The failure of the soft switching increases power loss. Moreover, the rms value of the current increases when the output voltage deviates from M = 0.5. Therefore, the farther M goes from 0.5 (Vout = 200 V), the lower the efficiency becomes. These effects are shown conspicuously when the conversion power is decreased. The SCRC has advantage in conversion efficiency in case the voltage conversion ratio is near M = 0.5.

VI. CONCLUSION:

This paper discussed the output voltage regulation characteristics, the inductor volume, and the efficiency of the SCRC using a phase-shift control method. A control method and soft switching operation of the SCRC was explained. The analysis of the stored energy in the inductor revealed that the inductor volume of the SCRC is smaller than the buck converter when the converter is operated in a range of 19%–81% in voltage conversion ratio. The analysis also showed that the SCRC has a significant advantage in inductor volume in case the voltage conversion ratio is around 0.5. Experimental setup rated at 2.8 kW confirmed the steady-state and transient-state operation. The conversion efficiency of the experimental setup reached more than 99%.

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