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A Review of Power Consumption Analysis for SRAMs

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ABSTRACT

Battery operated portable devices need low power consumption to increase the battery life. As SRAM is used in the microelectronic applications such as cache memory and occupies 90% of silicon area, various research works being carried out to reduce the power consumption. There are two ways, through which power consumption can be reduced, one is by dropping standby power and another one by reducing dynamic power. This paper had reviewed wide-range discussion and comparison of low power techniques. Various design techniques like 7T SRAM Cell, 9T cell, Charge recycling techniques, drowsy back bias scheme, and P4 SRAM scheme are discussed.

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INTRODUCTION

The increasing importance of portable systems and the need to limit power consumption in modern ULSI chips has led to rapid and innovative developments in low power design during recent years. Due to these developments, the portable devices require low power consumption and high throughput such as communication devices, Personal Digital assistant (PDA), cell phones, laptops and other handheld devices. In most of the cases, the requirement of the low power consumption must be m*et al*ong with demanding goals of high chip density and high throughput (Sung-Mo Kang, 2003). Now a day SRAM is mostly used in high performance circuits and memory occupies nearly 90% of silicon area such as cache memory. If power dissipation is more, it reduces the performance of SRAM. Therefore by using low power SRAM, these problems can be rectified. The power consumption occurs in the form of standby power and dynamic power. The power consumed during the bit stored inside the cell is called standby power. The power consumed during the read and write operation is called dynamic power. Many authors have discussed to reduce power consumption in SRAM by different approaches (Varun Kumar Singhal, 2011). Main power consumption element under dynamic power in CMOS SRAM is the charging and discharging of bit lines. Since in memory there are long running bit lines and for every read and write operation one bit line charges to full swing and another discharges to ground. The power consumed in this cycle is given by equation 1(Yang, 2010),

$$P= f \times (C_{bl} + C_{dl}) \times \Delta V_{bl} \times V_{dd} \quad (1)$$

Where, P = Power
f = Clock frequency
C_{bl} = Capacitance of bit lines
C_{dl} = Capacitance of data lines
ΔV_{bl} = voltage swing on bit lines
V_{dd} = supply voltage

In conventional SRAM,

$$\Delta V_{bl=} V_{dd} \quad (2)$$

Then equation 1 reduces to,

$$P= f \times (C_{bl} + C_{dl}) \times V^2_{dd} \quad (3)$$

With the increase in memory size C_{bl} and C_{dl} will also increase and power consumption varies directly with memory size. To avoid this, banked organization is used (Roy, 2000).

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1. 6T CMOS SRAM Cell:

A 6T CMOS SRAM cell as shown in Figure.1 shows the most well-liked SRAM cell due to its higher energy, low power and low-voltage operation. This SRAM cell must be intended such that it gives a non-destructive read operation and a consistent write operation. A SRAM cell can be in one of the three possible states, it can be in the stable state with the cell holding a value or it can be in the process of carrying out a read or a write. The stable state of the cell occurs with the word line connected to Q5/Q6 being driven low. The cell is efficiently detached in this mode of operation (Roy, 2000). A write to the cell is carried out by driving the bit lines to require state and activating the word line. For example, during write operation when logic low is given to BL and WL is given logic high Q6 transistor is turned ON, the output of Q6 passes to complementary transistor pair Q3 and Q1 which turns Q3 ON. The resulting output from Q5 is high as VDD is ON thus corresponding to BLB. A read operation is initiated by precharging the BL and BLB to precharge voltage and then WL goes high. Either BL or BLB discharges to ground, or a differential voltage is set up across the BL and BLB. This voltage is sensed by sensing amplifier and stored bit value is available at the output of the sense amplifier.

From the above operation, power dissipation of cell occurs in two cases, one is due to transistor switching activity during read and writes operation and another is when the cell is in stable state. Because one of the transistors in the two inverters remains ON continuously which leads to power dissipation due to leakage current.

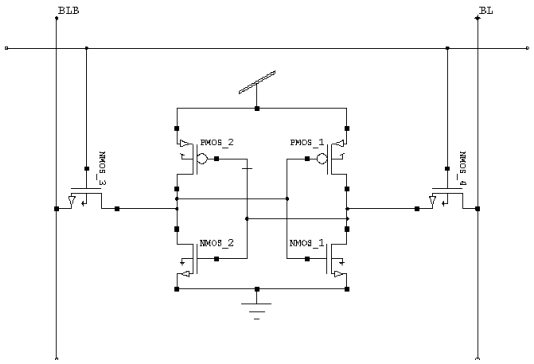

Fig. 1: Conventional 6T SRAM cell.

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2. Power reduction techniques:

This section explains different power reduction techniques in SRAM proposed by different authors.

2.1 Banked organization technique:

In banked organization technique (Roy, 2000) that targets the reducible total switched capacitance to achieve reduced power and improved speed. Banked organization needs a R × C memory where R is number of rows and C is number of columns and an unfortunate outcome of such an organization is that any access to the core causes 'R' cells to be enabled. Generally if cell is the capacitance of the bit line per cell, a total capacitance of $R \times C \times C_{cel}$ is switched. The efficient way to reduce the switching capacitance by splitting the memory into small memories. It is clear that memory blocks are accessed either write or read operation. A complete column or row is activated. If the memory is divided into sub blocks an additional set of decoders is needed to select one of the 'B' bank as shown in Figure.2, where B=4.While an additional delay is gained in selecting the bank and it is compensated by the much lower capacitance that is switched per bank, which is clearly $(R \times C \times C_{cell})/B$ then net capacitance for read write operation which will reduce half for bit lines and address lines.

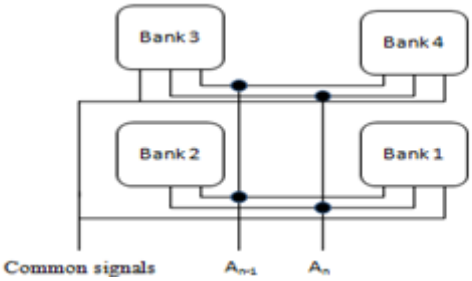

Fig. 2: Banked organization.

2.2 7t Sram cell:

Ramy E. Aly and Magdy A. Bayoumi (Ramy, 2007), proposes 7T SARM cell architecture, in which the power reduction is achieved during the write operation. Figure.3 shows the 7T SRAM circuit diagram. It includes one additional NMOS transistor (N5) which is used to give the feedback link and detachment between two inverters.

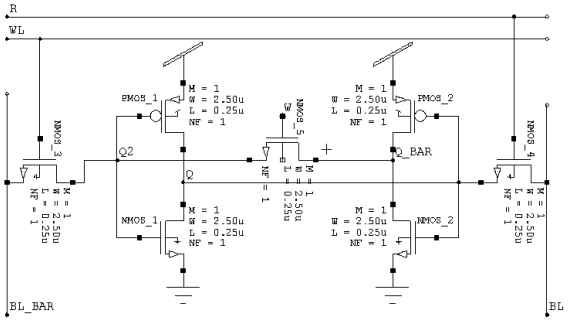

Fig. 3: 7T SRAM cell.

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The write down operation is performed by turning off N5 transistor to cut off the feedback connection. BL _bar take complement of the input data. When N3 transistor is turned on, N4 goes off state as shown in figure 3.

Table 1: Power consumption comparison during write pattern.

Memory Size	Voltage	Technology	Write Pattren	Power(µW)	
				Conventional SRAM	7T SRAM
128×8	1.8v	0.18µm	0 to 0	113.5	7E-2
			0 to 1	116.7	118.4
			1 to 0	116.5	4.7
			1 to 1	113.3	115

The 7T SRAM cell is formed as two cascade inverters, inverter 2 followed by inverter1. Data from BL_bar to Q2 is transferred by transistor N3 which drives inv2, P2, N2 to develop Q, the cell data. Likewise, Q drives inv1, P1 and N1 to develop Q _bar which is equal when data is "0" and slightly higher than Q2 when data is "1." Then, to reconnect the feedback link between the two inverters WL is turned off and N5 is turned on to store the new data. Both BL and BL_ bar are pre charged "high." Using this write scheme, BL _bar is made high" to write "0" with insignificant power utilization and vigilant transistor sizing is necessary to assurance a stable write "0" BL_bar is discharged to "0" with comparable reduced power consumption to the conventional 6T cell to store "1" in cell. To store a "0" in the cell, discharging of BL_bar is not necessary and therefore, the discharging BL_bar activity factor is less than 1 and depends on the percentage of writing "1." For read operation WL and R signals are kept on, while N5 is kept off. When there is Q=0, the read path consists of N2 and N4 which works like a conventional 6T cell. When there is Q=1, the read path consists of N1, N5 and N3, which represents a critical read path. Driving capability of cell is reduced when transistors are connected in series. Due to reducible activity factor of switching BL_bar the max power is saved which is shown in figure.12. From Table 1, 0 to 0 write pattern consumes less power due to only on one of the two bit lines performs a write operation.

2.3 9t Sram cell:

C.M.R. Prabhu (Prabhu, 2009) proposed 9T SRAM cell in which the power consumption is reduced by using an asymmetric inverter pair. This circuit, least power is attained throughout writes and read operations match up to to 6T conventional circuit. Figure.4 shows 9T SRAM cell which is similar to ZA cell (Chang, 2004) with slight difference. The difference is gate of the N7 transistor is connected to BL instead of WS signal as in case of ZA cell (Chang, 2004). An extra N6 transistor connected between two inverters so that during the read operation, cell is working as conventional 6T SRAM cell. While write operation, RWL is set to low and consequently N6 is turned off .Now 9T SRAM cell is same as ZA cell. The write 0 operation of the 9T SRAM is similar to zero aware cell (Chang, 2004). During write 1 operation node B is setting as BL= high, and now the circuit is behaves as conventional SRAM, Since the power consumption is minimized during write 0 operation. The 9T SRAM cell is simulated by tanner tool 0.025µm feature size and average power is reduced by 14% than the conventional SRAM, during write '0',throughout write '1'operation cell act as 6T SRAM which is shown in

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figure.13.from table 2, 9T cell consumes 0.0025mW during reading 0 and reading 1 mode it consumes 0.819mW.

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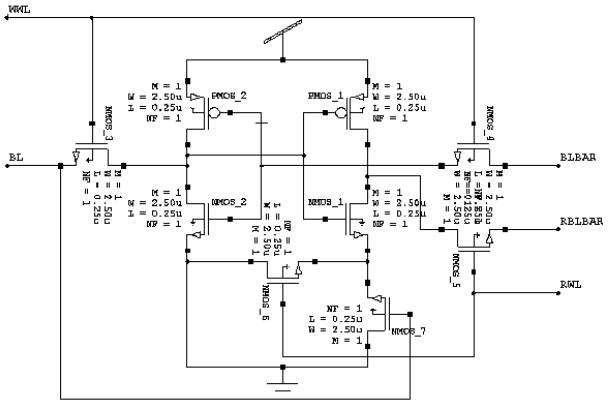

Fig. 4: 9T SRAM cell.

Table 2: Comparison of read power for '0' and '1' in 9T.

Memory Size	Voltage	Technology	Read power '0'	Read power '1'
6T	3v	0.25µm	0.581mW	0.581mW
9T	3v	0.25µm	0.0025mW	0.891mW

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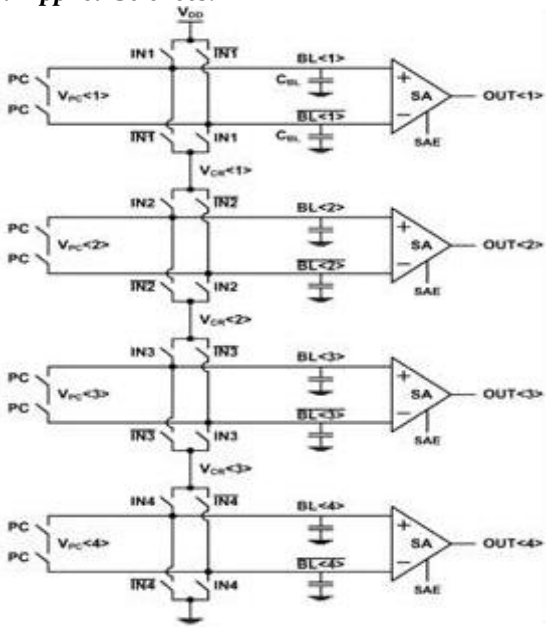

Fig. 5: Concept of bit-line charge recycling (n=4).

2.4 Charge recycling technique:

Power consumption is due to charging and discharging of bit lines. B.yung- Do Yang (Yang, 2010) proposes a novel writing scheme using CR technique in which low voltage swing is developed by reusing of previous charged bit line. This reduces read and write power by reusing the charge in bit lines. The charge is recycled by N bit lines, therefore 1/N times reduced the swing voltage and $1/N^2$ times reduced the bit line power. Hierarchical bit line architecture is utilized for charge recycling technique. This scheme, number of pairs are represented by N. Figure.5 showing the charge recycling SRAM for N=4 ie., 4 bit line pairs are paired .In precharge mode, precharge signal switch (PC) connects the two bit lines in each bit line pair and all evaluation switches (IN(1 : 4) and INb(1 : 4)) are disconnected. Two bit-lines in bit line pair share their charges being different voltages thus become average voltage of them. In evaluation mode, precharge switches are disconnected and evaluation switches (IN(1 : 4) and INb(1 : 4)) are connected. According to input data, whether

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a bit line is connected to adjacent bit line with higher or lower voltage, is determined by the evaluation switches. The adjacent bit line is connected with higher voltage to bit line when the input data is 1. The bit line receives charge from adjacent bit line and its voltage is increased and opposite bit line is connected to the adjacent bit line with lesser voltage. The charge in the bit line pair is recycled to the next bit line pair. In precharged mode, the (BL (1) and BLb (1) has the charge Q1. In evaluation mode, Q1 charge is transferred to second bit line pair (BL (2) and BLb (2)). Now Q1 charge is recycled in the second bit line join up in the subsequently clock cycle. Thus charge Q1 is used N times throughout N-bit line pairs during N clock cycles (N=4) in figure.5. The experimental results are shown in Table 3.The charge recycling SRAM reduce the read,write powers by recycling the charges through 'N' BLs and waveforms illustrating the concept of the bit line Charge recycling technique as shown in figure.14.

Table 3: Read power and write power comparison table for CR-SRAM.

Parameters		CV –SRAM	CR-SRAM
Memory Size		256×128	256×128
Voltage	Read	1.2v	0.15
	Write	0.15	0.15
Frequency		100MHz	100MHz
Power	Read	0.39	0.32
	write	2.12	0.34

2.5. Dual v_t voltage:

To reduce the leakage power of SRAM, Behnam Amelifard, Forzan Fallah, Massound pedram proposed a novel scheme, which is based on dual voltage assignment to reduce the leakage power of SRAM. In this scheme, different voltages are assigned to all or some of the transistor cells are increased. As shown in table. 4. there are eight different configurations for assigning the low and high threshold voltage (V_t) to the transistor within a cell. The threshold voltage (V_t) of each transistor is independently adjusted without affecting each other threshold voltage (V_t) by changing the channel doping because the channels of transistors are not too close to each other. This method is designed and simulated in Cadence platform with supply voltage of 1.8V at 180 nm technology (Behnam Amelifard). Figure.15 shows the leakage current savings of different configurations versus high threshold voltage. Table 5**,** shows the leakage power savings percentage is highest at $0.42V_t$. in which it can be seen that configuration C0, C1,& C2 for low value of $V_{t,high}$,C0,C4,&C6 for high value of $V_{t,high}$ is used.

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Table 4: Possible Configurations for High Threshold Voltage Assignment

Configuration	High Threshold Transistors
C0	None
C1	M1,M2,M3,M4,M5,M6
C2	M3,M4,M5,M6
C3	M1,M2,M5,M6
C4	M1,M2,M3,M4
C5	M5,M6
C6	M3,M4
C7	M1,M2

Table 5: Power reduction and utilisation of each configuration in the low leakage SRAM.

Vt,High	Leakage reduction (%)	Utilization of each configuration (%)							
		C0	C1	C2	C3	C4	C5	C6	C7
0.38	14.64	13.5	76.2	3.1	0.8	2.1	1.2	3.1	0
0.39	25.00	13.7	65.4	7.6	0	6.4	0	6.8	0
0.40	31.84	13.7	52.9	10.0	0	16.0	0	7.4	0
0.41	36.48	13.7	46.9	8.2	0	18.6	0	12.7	0
0.42	38.77	14.1	33.6	15.0	0	24.0	0	13.3	0
0.43	36.55	14.1	8.0	33.8	0	25.4	0	18.8	0
0.44	34.74	14.1	0.6	22.1	0.2	38.1	0	25.0	0
0.45	35.06	14.1	0	9.4	0.2	51.0	0	25.4	0
0.46	34.66	14.1	0	2.5	0	52.5	0	30.9	0
0.47	35.30	14.1	0	0	0	53.9	0	32.0	0
0.48	35.14	14.1	0	0	0	49.0	0	36.9	0
0.49	34.54	14.1	0	0	0	43.0	0	43.0	0
0.50	33.61	15.8	0	0	0	38.7	0	45.5	0
0.51	33.36	16.2	0	0	0	36.1	0	47.7	0

2.6 Drowsy back bias scheme:

Drowsy back bias is a technique proposed by Rabiul Islam, Adam brand, Dave Lippincott as shown in the fig.6. In which PMOS and NMOS reverse bias techniques are used to leakage reduction. This technique is utilized in 2MB SRAM test chip. In PMOS the P channel N well is raised above vcc_mem through reverse bias

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and nMOS is reverse biased when Vss of array is raised to N channel sources and keeping substrate voltage is 0v. Thus the voltage regulators maintain the bias levels. This drowsy mode is called as static mode. In this mode no read or writes operations are allowed. Thus control sequences are necessary to move the array inside and outside of drowsy. This SRAM module separate power supply domain V_{cc}_mem is used and fabricated at 90 nm technology. To attain this high performance, the devices were optimized V_t and low Cgate at the voltage of 0.8v are employed (Rabiul Islam). Fig 6 shows cell leakage measurement during drowsy and idle mode. Fig 16**.**shows the Measurement of Vccmin during write and read operation of drowsy back bias scheme.

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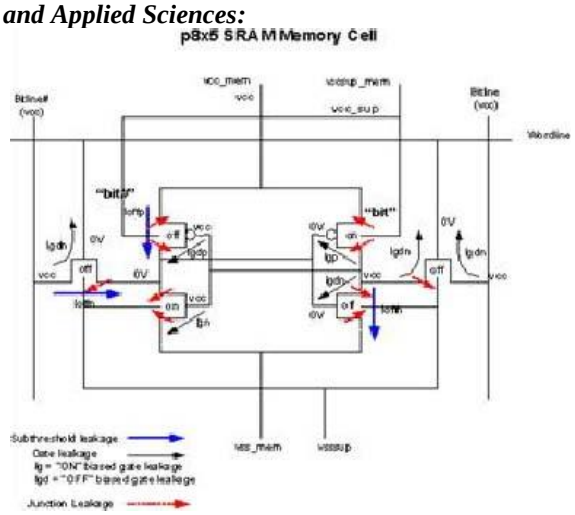

Fig. 6: Cell leakage components and leakage paths during drowsy back-bias.

2.7 P4 sram bit cell:

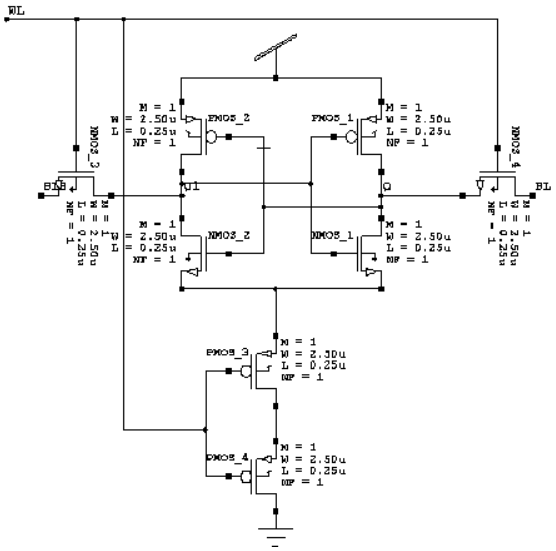

Fig.7: P4 –SRAM Bit cell structure.

Neeraj, R.K. Singh, Manisha Pattanaik proposes a novel P4 SRAM bit cell as shown in figure.7 In which, the barrier height of holes is made larger than that of electrons which is 4.5 eV. When PMOS transistors are in OFF state, gate leakage current is reduced. In standby mode full supply substrate body bias reduces sub threshold leakage current. The SRAM bit cell utilizes stacking of transistors in self reverse biasing of series connected transistors. When WL=0, cell is in active state and ready to read/write data, thus the bit cell behaves as 6T conventional cell. When there is WL=1, the two access transistors PMOS are turned OFF. Stacking transistors are ON in order to sink current. So these transistors are made larger, this reduces read time owing to increase in cost area. In PMOS transistor a forward full supply body biasing is used to reduce active power consumption. (Neeraj, 2011).

In this work the bit cell active power is reduced up to 89% for write data 0 and write data 1, Table.6 shows standby mode power consumption of conventional SRAM and P4 SRAM. This type of SRAM mostly used in

multimedia & Mobile applications. figure.17 and 18, Shows comparison chart for reduced dynamic power upto 89% while writing the data '0' and '1'.

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Table 6: Active power consumption in standby mode of operation.

Memory size	V_{DD}	Technology	CV-SRAM		P4-SRAM	
			Active power			
6T	0.7v	45nm	Writing '1'	Writing '0'	Writing '1'	Writing '0'
			4.011µw	3.815µw	418.65nw	418.52nw

2.8 Source biasing technique:

In this leakage current reduction technique, the line voltage is increased in sleep mode operation to reduce the bit line leakage and generate the negative V_{gs} in the access transistor as shown in Figure.8. The sub threshold leakage is reduced in the transistor by reducing the bit line leakage, signal rail and body effect and when the source voltage is reduced the gate leakage is also reduced (Agarawal, 2002; Yamauchi 1996; Bhavnagarwala, 2000; Osada, 2003).

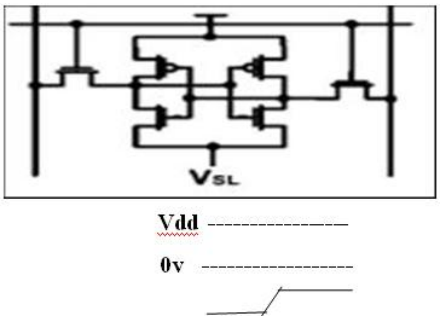

Fig. 8: Source biasing technique

2.9 Dynamic voltage supply:

In this scheme, supply voltage is reduced to lower the leakage power, however, In which the bit line leakage cannot be reduced, and the bias condition in the access transistor does not change which is shown in Figure 9.

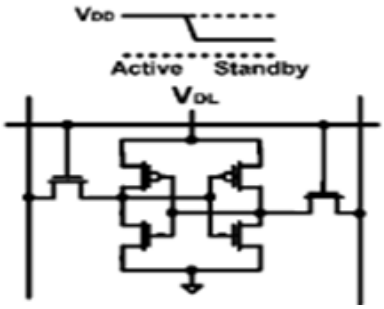

Fig. 9: Dynamic Voltage Supply.

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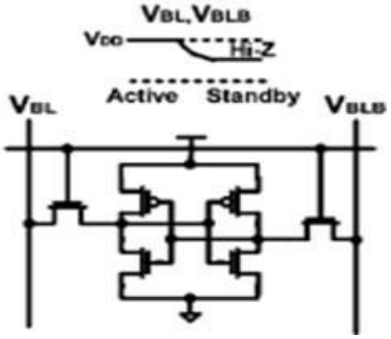

Fig. 10: Floating Bit Line.

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2.10 Floating Bit Line:

In This technique the bit lines are floating in the standby mode and reduce the leakage in bit lines by way of DIBL. Figure.10 shows this technique, it is only applied to different cache lines not a individual cache line. Generally, the bit lines are pre charged during access the word line. If new array is accessed an extra pre charge cycle is required.

2.11 Leakage current reduction:

Srinivasa Rao, Raghavendra Sirigiri, V.Malleswara Rao Proposed a new scheme, In which leakage current can be controlled by leakage controlled transistor in the SRAM cell. The technique behind this approach for reduction of leakage power is efficient stacking of transistor path from VDD to ground. Based on the above approach two leakage control transistor in each inverter pair, in this, one of the transistors in near its cut-off region of its operation as shown in figure 11.

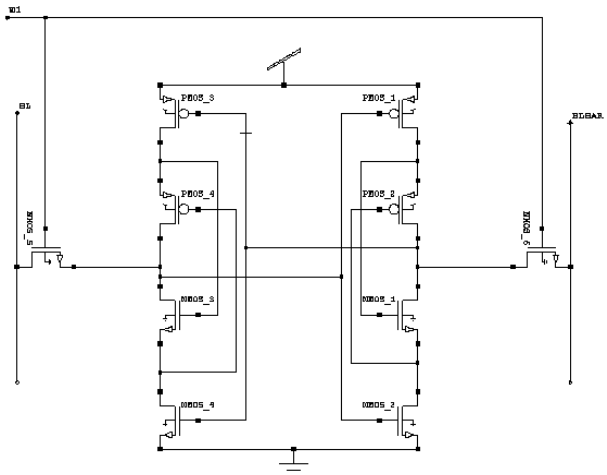

Fig. 11: Leakage current reduction.

The two leakage power control transistor NMOS and PMOS are positioned between the nodes & pull-up, pull-down logic of the inverter. The switching transition of two transistors are controlled by the voltage potential at nodes. As stated earlier one of the leakage manage transistors is always near its cut-off region irrespective of the input. Therefore the resistance of the transistor in not as high as its ”off” state resistance ground path resistance increases, due to this leakage current can be controlled hence leakage power reduction achieved. Due to leakage control transistor increases the resistance of the supply voltage to ground will less than OFF state resistance, and allowing condition enabled, though the resistance of the current is reduced around 25% and different threshold voltages are assigned in dual V_t transistor which diminish leakage power more than 35%. Gate leakage as well as bit leakage is reduced in source biasing scheme. In dynamic voltage supply scheme supply voltage is used to reduce power whereas in floating bit line scheme bit lines reduce power leakage (Srinivasa Rao, 2011). Figure 19 shows the graph between power and V_{DD}. The total power reduced upto 48%.and table 7 shows power dissipation of proposed SRAM with various temperature.

Table 7: Power dissipation of 6T cell with respect to temperature.

S.No.	Vdd(V)	Temperature	Power dissipation in 6T SRAM(w)	Power dissipation in proposed SRAM(w)
1	1.32	27°C	3.010×10-4	1.593×10-4
2	1.2		2.225×10-4	1.086×10-4
3	1.08		1.569×10-4	0.672×10-4
4	1.32	4°C	3.103×10-4	1.599×10-4
5	1.2		2.287×10-4	1.075×10-4
6	1.08		1.610×10-4	0.650×10-4
7	1.32	60°C	2.884×10-4	1.581×10-4
8	1.2		2.143×10-4	1.097×10-4
9	1.08		1.517×10-4	0.699×10-4

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3. Conclusion:

In this paper various existing power reduction techniques are discussed and compared. Banked organisation technique provides low power consumption by simply dividing the capacitance of bit line and word line into sub blocks. Activity factor is reduces the power consumption in 7T SRAM cell by selecting only on one of the two bit lines. In 9T SRAM cell an asymmetric inverter pair is used for reduction of average power consumption during read and write mode. The bit line charge is recycling in the SRAM which reduces the 17% read power and 84% write power in charge recycling technique. Using different V_t assignment for SRAM the low leakage power is achieved. The standby power is reduced upto 16× by applying the reverse bias technique .In P4 SRAM cell the-V_{DD} gated-V_{DD} technique is used to reduce standby, active and dynamic power. The reduced bit line leakage, signal, body effect and lowering the supply voltage is reduces the Sub threshold leakage in source biasing technique and dynamic voltage supply.

The floating bit line technique reduces the bit line leakage when the bit lines are floating during the standby mode. The efficient stacking of transistor between V_{DD} and ground the leakage power is consumed 48% less than conventional SRAM. The references and analysis of this paper is helpful in new design phases of low power SRAM.

4. Simulation results:

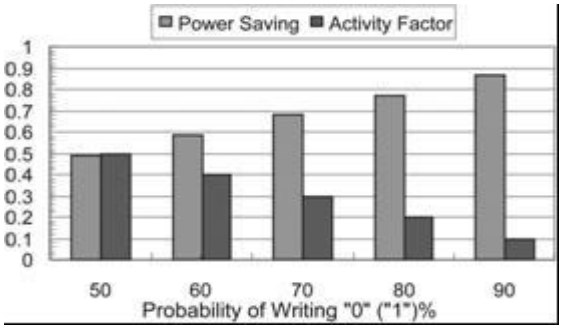

Fig. 12: Power saving and activity factor at different writing "0" probabilities using the.

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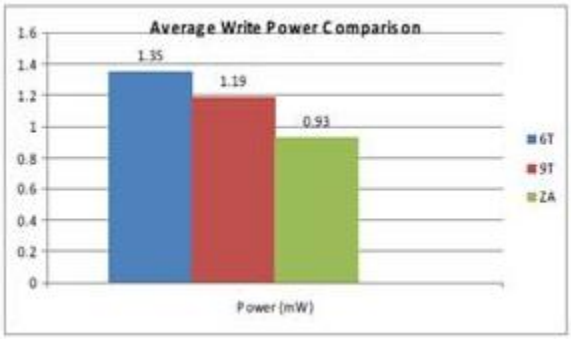

Fig. 13: Average Write Power: A comparison of the 9T cell.

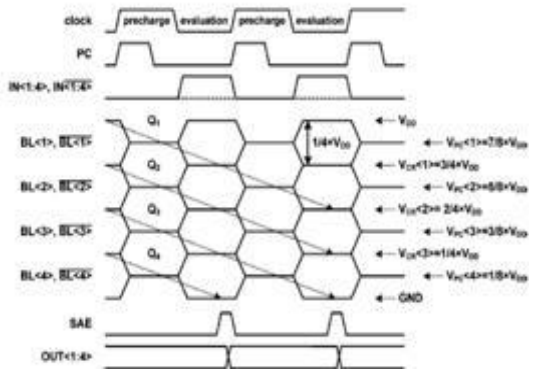

Fig. 14: Waveforms illustrating the concept of the bit-line charge-recycling (N=4).

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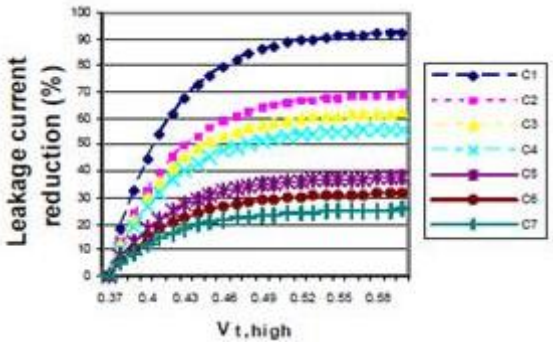

Fig. (15,16): Measured cell leakage during idle and drowsy back bias state Figure 15. Leakage current reduction for each configuration using dual Vt transistors.

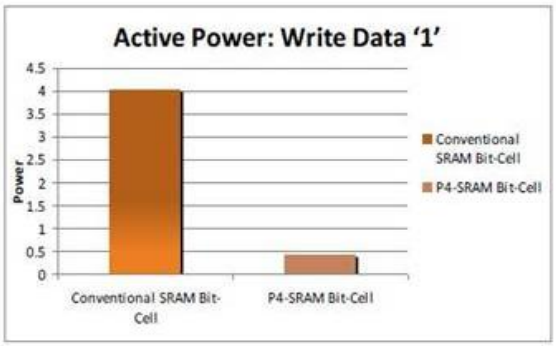

Fig. 17: Active powers for write data"1" using P4SRAM cell.

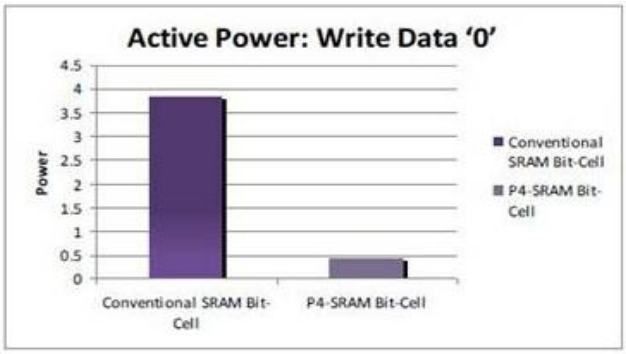

Fig. 18: Active power for write data "0" using p4 SRAM cell.

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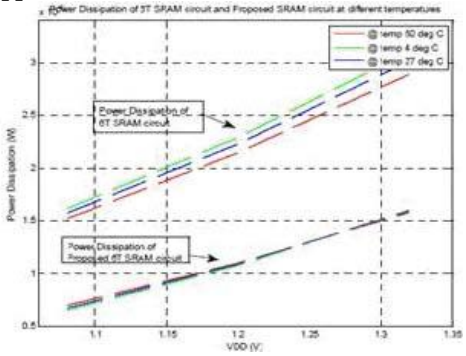

Fig. 19: Power dissipation of SRAM at different temperatures.

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