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Technique For A Higher PSRR In The Regulator Low-Dropout Voltage in 90 nm CMOS Technology

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ABSTRACT

This paper presents a low-dropout regulator (LDO) for portable applications that use a increase gain technique. As a result, the error amplifier gain increases enough to maintain accurate output voltage and block the low frequency supply noise and finally obtain a high power-supply rejection ratio (PSRR). The objective of this research is to develop novel LDO regulators that can achieve good high frequency PSRR performance. Moreover, an tri-state buffer for driving the pass device. The LDO is implemented in 90 nm CMOS technology and achieves a power-supply rejection ratio better than -70 dB up to 100 KHz for load currents up to 100 mA. The voltage regulator provides maximum 110 mA current, moreover with a 1.2V supply voltage, this LDO regulator providing an output of 1 V with a 200mV drop-out voltage.

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INTRODUCTION

Today and in parallel to the electronic revolution, the importance of systems power management has increased significantly in the electronics industry in recent years. This involves increasing demand regulators for electronic devices such as portable batteries as tablets, laptops, and cell phones. Especially, there is lot of articles which are interested for the increasing of the gain, So far, there are few papers published about the design of in increasing of the gain of the regulators, only all studies of the increasing of the gain in the articles are limited about the 2nd stage by using buffer circuit or other technical of the load current (Young-Sub Yuk, 2012; Gianluca Giustolisi, 2012; Ka Nang Leung, 2003; Chaitanya, K., 2004 Pui Ying Or, Ka Nang Leung, 2010).

Therefore, a small gain produces a large steady state error at DC condition, as well as among the proposed solutions which are found in the studies conducted the uses of local positive feedback with negative feedback to increase the gain.

In this article, one PSRR improvement method is presented. this method proposes a novel topology a control drain of transistor that overcomes the problem that obtain a high gain DC without changing the W / L ratios in a node of the circuit design. This improves the gain of the environment without modifying the function of each transistor circuit scheme to improve the PSRR of an LDO. The proposed power supply scheme is designed by using adaptive quiescent current, thereby not degrading the others performances. This circuit have been designed in 90 nm technology.

1. Design Of Increase Gain Circuit And Tri-State Buffer:

2.1 Design Requirement Of Increase Gain Circuit:

A technique of the increase of the DC gain of the proposed symbol Ad regulator in this work increases Ad without changing W / L ratios of each transistor circuit proposed. This improves the operation of the transistors in the same environment without interfering area saturation transistors.

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When the CMOS technique of increase gain has taken place in the circuit, automatically the gain of the voltage regulator has increased this should take some other factors into consideration, such as: power efficient and power-supply rejection ratio (PSRR), moreover it uses a few devices and low cost, in addition the amplifier's gain refutes the supply noise, the PSRR worsen if the frequency increases beyond the regulator's -3dB bandwidth because of the decrease of loop gain (Ka Nang Leung, 2003; Quan Zhou, 2012; Amit, P., 2010).

2.2 Design Principle Of The CMOS Technique Of Increase Gain Circuit Proposed:

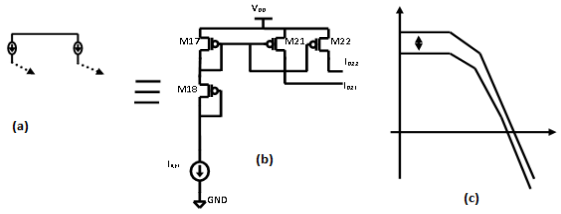


Fig. A.1: (a) block diagram of the circuit proposed of increase gain, (b) active implementation of theproposed circuit, and (c) frequency response of the proposed circuit.

2.2.0. Without the Proposed Circuit:

The differential pair (M1, M2) loaded by the transistors M3 and M4 are diode connected.

$$A_{d0\_DC}=\frac{-g_{m1,2}}{g_{m3,4}}=-\sqrt{\frac{\left(\frac{KW}{L}\right)_1\frac{I_{D5}}{2}}{\left(\frac{KW}{L}\right)_{3,4}\frac{I_{D5}}{2}}}=-\sqrt{\frac{\left(\frac{KW}{L}\right)_1}{\left(\frac{KW}{L}\right)_{3,4}}} \qquad \text{(Eq. (A.1))}$$

2.2.1. With the Proposed Circuit:

The schematic of the PROP_C is in shown in Fig. A.1. If the current source M22 (successively .M21) provides 90% of the current ID2 .that is to say ID21 = ID22 = 0.9 ID5 / 2 and ID3 = ID4 = 0.1 ID5 / 2 this can be done for the right choice of ID17.

$$I_{D17}=I_{D21}=\tfrac{1}{2}(\mathrm{KW}/L)_{17}(V_{DD}-V_{G17}-V_{th17})^2=\frac{0.9I_{D5}}{2} \qquad \text{(Eq. (A.2))}$$

$$A_{d1\_DC}=-g_{m1,2}r_{out}=-(g_{m1,2}r_{ds1,2})//(\tfrac{1}{g_{m3,4}})//(r_{ds21,22}) \qquad \text{(Eq. (A.3))}$$

$$=-\frac{g_{m1,2}}{g_{m3,4}}=\sqrt{\frac{\left(\frac{KW}{L}\right)_1\frac{I_{D5}}{2}}{\left(\frac{KW}{L}\right)_{3,4}0.1\frac{I_{D5}}{2}}}=-\sqrt{10}\sqrt{\frac{\left(\frac{KW}{L}\right)_{1,2}}{\left(\frac{KW}{L}\right)_{3,4}}}$$

generally the current of M17 equal the current of M21 equal the current of M22 equal (0.9 - 0.i) of the current of M5 divided 2. And Ad1_DC equal (√ (10/i)) of Ad0_DC provided i greater than zero (i>0).

$$I_{D17}=I_{D21}=I_{D22}=(0.9-0.\mathrm{i})\frac{I_{D5}}{2}\Rightarrow I_{D3}=I_{D4}=0.i\frac{I_{D5}}{2} \qquad \text{(Eq. (A.4))}$$

$$Ad1\_DC=\frac{\sqrt{10}}{\sqrt{i}}Ad0\_DC \qquad (\ i>0\ ) \qquad \text{(Eq. (A.5))}$$

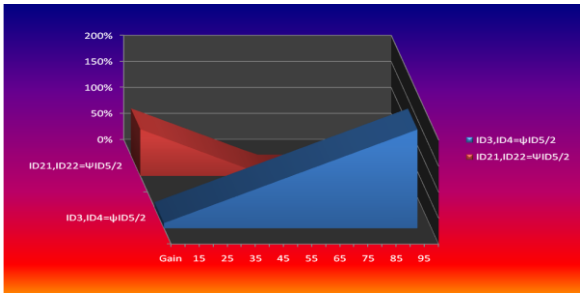


Fig. A.2: Increase gain at different values of the current $I_{D21,22}$ and also changes $I_{D3,4}$ with a increase gain proposed circuit.

2.3. Design requirement of tri-state buffer:

The schematic buffer design contains a tri-state which are transistors: M23_M24, M25_M26_M27_M28 and M29_M30_M31_M32 form respectively the inverter, NOR and the NAND is shown in Fig. A.3. The function of the buffer as following if the output of the error amplifier is low, then the output will be high impedance state. And If the output of the error amplifier is high, then the output will have the same logic value as the drain junction of the transistor M6. In this case, with the existence of the NOR gate improves the speed output. Thus a low propagation delay can be used in the design LDO regulator, that is to say, which we choose the existence of the NOR gate. In addition, the Tri-state buffer that has propagation delay under 5ns, as shown in Fig. A.4.

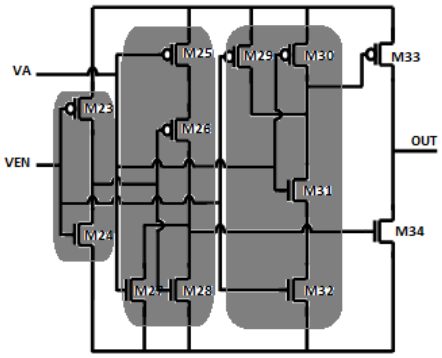


Fig. A.3: The full schematic of the Tri-state buffer.

The total input capacitance can be written as follows
Cin = 3/2(Cox,n + Cox,p + Cox,n + Cox,p) = 100fF We know that Cox =0.0625fF.
So, 100 fF > 3 (Cox (Wn Ln + Wp Lp)).

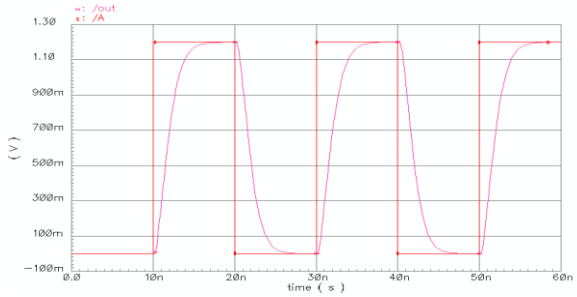


Fig. A.4: The tri-state buffer propagation delay.

Fig. A.5 shows the circuit of the voltage regulator LDO proposed, using five-stages. The principle stage is the error amplifier was implemented using five transistors M1, M2, M3, M4, M5 in the first stage and M6, M8, M9, M10 in the second stage. M1_M2 are the transconductance of the first stage. The function of the transistors M1, M2 is to connect the shunt feedback and the reference voltage (VREF) respectively and show a qualitative comparison of the output voltage and the reference voltage. The effect of the PROP_C to transistors M1, M2, M3, M4, M5. This is one of the excellence and the preference in the circuit design of the voltage regulator.

The output stage the following form, the feedback is provided by a resistive network including R1 and R2 and a common-source amplifier realized with the huge pass transistor MP.

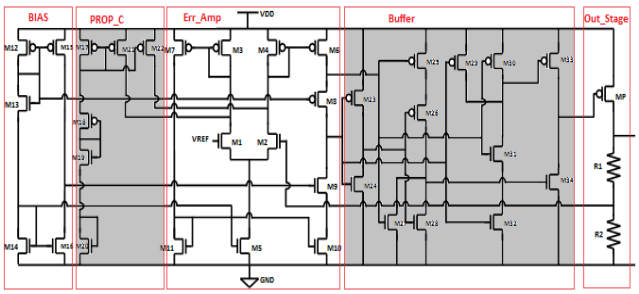


Fig. A.5: The full Schematic of the LDO regulator using a P-MESFET pass transistor.

The closed loop with the negative reaction against, yes looped back then the output into the input the negative in the regulator circuit must operate in linear regime.

Since we compensate a frequency of the regulator circuit, then the added external components was adjustable. The compensation with a very small capacitor Cc of a few worth of the Pico-Farad (pF) or with a series capacitor Cc with a resistance R in the circuit of the regulator voltage. That is why we could actually even moving the pole gain curve Ad, ie to increase the phase margin (Mph) closed loop or to increase the stability of the regulator LDO and even can be increase the bandwidth (BP) circuit without reducing the Ad gain.

In Eq. (A.j), gmk and rdsk are the transconductance and output independence of transistor Mk, respectively. R0 , R02 and C0 , C02 are the output independence and capacitor of the 1st and 2nd stage of the amplifier, respectively. The Boost Factor power-supply rejection ratio FB(PSRR) will be increased from Ad0_DC to Ad1_DC, causing an increase in the gain and hence an improvement of the PSRR. Equation (A.6) shows that the six equations from which Vout, VDD, VFB, VgMP, V1 and V2 can be obtained in matrix form, it's completely determined from the equivalent small signal model of the proposed LDO shown in Fig. A.6.

In Eq .A.8, P1, P2 and P3 are the dominant pole, the second pole, and the third pole of the LDO. Z1, Z2 and Z3 are the zeros, and FB(PSRR) is the boost factor power-supply rejection ratio.

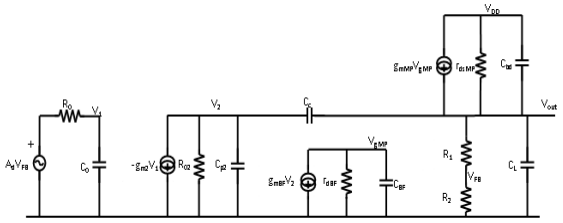


Fig. A.6: Equivalent small signal model of the proposed LDO.

$$\begin{pmatrix} -(g_{dsMp}+C_{bdMP}S)-(\frac{1}{R_1+R_2}-C_LS)-C_cS & g_{mMP}+(g_{dsMP}+C_{bdMP}S) & 0 & -g_{mMP} & 0 & C_cS \\ 0 & 0 & 0 & g_{dsBF}-C_{BF}S & 0 & g_{mBF} \\ C_cS & 0 & 0 & 0 & g_{m2} & -(g_{ds2}+C_{p2}S)-C_cS \\ 0 & 0 & \frac{A_d}{R_0} & 0 & \frac{1}{R_0}-C_0S & 0 \\ \frac{-R_2}{R_1+R_2} & 0 & 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{out} \\ V_{DD} \\ V_{FB} \\ V_{gMP} \\ V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \quad \text{(Eq. (A.6))}$$

$$PSRR = \frac{-(R_1+R_2)g_{dsBF}\left(1+\frac{C_{bdMP}}{(g_{mMP}+g_{dsMP})}S\right)\left(1+C_0R_0S\right)\left(1+\frac{C_{BF}}{g_{dsBF}}S\right)}{A_dg_{m2}g_{mMP}R_2\left[\frac{1}{g_{mMP}}+\left[\frac{(R_1+R_2)\left(g_{dsBF}\left(C_{bdMP}+C_L\right)+g_{mMP}C_c\right)}{A_dg_{m2}g_{mMP}^2R_2}\right]S+\left[\frac{(R_1+R_2)C_cC_{BF}+R_0(R_1+R_2)g_{mMP}C_0C_c-R_0(R_1+R_2)g_{dsBF}C_0C_L}{A_dg_{m2}g_{mMP}^2R_2}\right]S^2+\left[\frac{-R_0(R_1+R_2)(C_{bdMP}+C_L)}{A_dg_{m2}g_{mMP}^2R_2}\right]S^3\right]} \quad \text{(Eq. (A.7))}$$

$$F.B.(PSRR)=\left(\frac{A_dg_{m2}g_{mMP}R_2}{(R_1+R_2)}\right)^{-1}$$

$$\begin{cases} P_1=\dfrac{-1/g_{mMP}}{(R_1+R_2)\left(g_{dsBF}\left(C_{bdMP}+C_L\right)+g_{mMP}C_c\right)} \\ P_2=\dfrac{-(R_1+R_2)\left(g_{dsBF}\left(C_{bdMP}+C_L\right)+g_{mMP}C_c\right)}{(R_1+R_2)C_cC_{BF}+R_0(R_1+R_2)g_{mMP}C_0C_c-R_0(R_1+R_2)g_{dsBF}C_0C_L} \\ P_3=\dfrac{(R_1+R_2)C_cC_{BF}+R_0(R_1+R_2)g_{mMP}C_0C_c-R_0(R_1+R_2)g_{dsBF}C_0C_L}{R_0(R_1+R_2)\left(C_{bdMP}+C_L\right)} \end{cases}$$

$$\begin{cases} Z_1=\dfrac{g_{mMP}+g_{dsMP}}{C_{bdMP}} \\ Z_2=\dfrac{1}{C_0R_0} \\ Z_3=\dfrac{g_{dsBF}}{C_{BF}} \end{cases} \quad \text{(Eq. (A.8))}$$

2. The ldo high psrr discussion and simulation:

Fig. A.7 is the simulation result of output voltage Vout for different power supply voltage Vdd. Vout is among 1V to 1.09V when input voltage Vdd changes from 1.1V to 2.6V. The voltage regulator produced a maximum output current of 110 mA as shown in Fig. A.8. Load transient responses of the designed LDO with a 100 nF output capacitor to the 0-110mA

load transient with rise and fall time of 1n and 1ns is shown in Fig. A.9. It is observed that the LDO can react to fast load current changes and is stable over the entire load current with a maximum output voltage deviation of only 1mV.

Fig. A.10 shows the loop-gain simulation of the proposed LDO with the proposed block diagram of the circuit proposed of increase gain and the proposed voltage buffer shown in Fig. A.3. It shows that the LDO has the best stability at no-load condition and it also has good stability at ILoad = 110 mA (PM=109°).

The simulated of The power supply rejection ratio (PSRR) is equal a -70dB over the entire load current range at a load of 100mA. At a low frequency, from 1KHz to 100 KHz-area, the PSRR was about -70 dB as the worst value is shown in Fig. A.11, and -43 dB at 10 MHz.

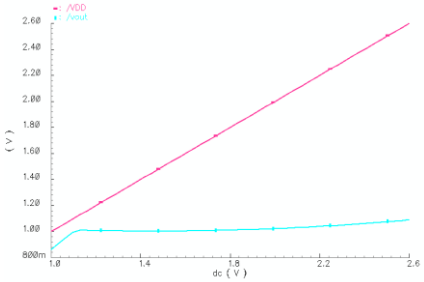


Fig. A.7: Line regulation with different load conditions for a 0-2.6 V input voltage.

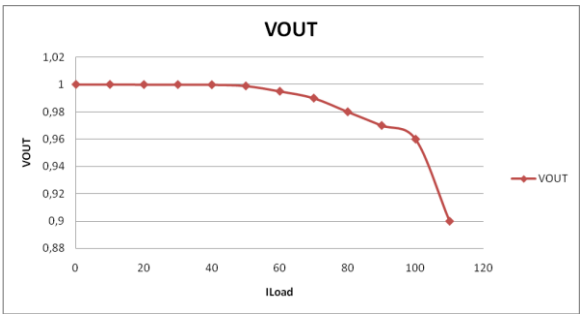
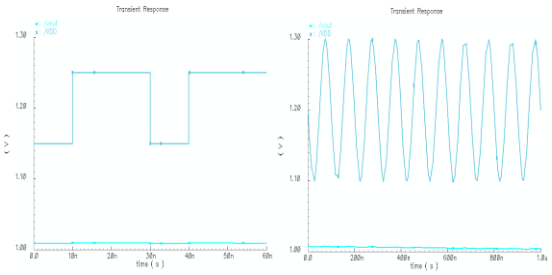


Fig. A.8: Output voltage LDO as function of the load current.



(a).1 (b). 1

Fig. A.9: The transient responses to input voltage steps. (a) 1 pulse signal Vin transition time with C_L = 100 nF. (b) 1 sin signal Vin transition time with C_L=100nF.

The layout of proposed high performance LDO with the circuit technique proposed of increase gain is shown in Fig. A.12. the area size is about 16.175 x 24.165 = 390,868875 μm^2.

Conclusions:

This research paper presents an increase gain technique LDO regulator for we get a high PSRR, although of the increase gain scheme is very simple. Compared to the other dynamic bias approaches, the proposed circuit makes the LDO achieve a high PSRR. We use a Tri-state buffer that has propagation delay under 5ns for render the output in the fast situation. Furthermore, it achieves a very low quiescent current of 26.3 µA as well as an excellent FOM (0.0025 ns). It regulates the output voltage at 1 V from 1.2 V – 2.6 V supply, with a minimum drop-out voltage of 200mV at the maximum output current of 110 mA. Its distinct features, ultra-fast response time of 100ns and very low power consumption.

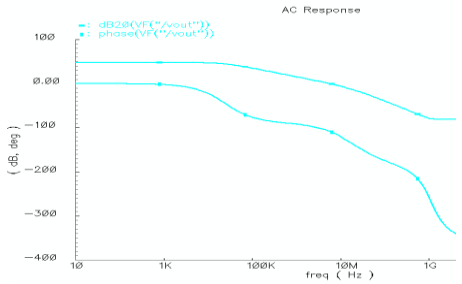


Fig. A.10: The simulated loop gain of the LDO with the proposed buffer at I_L= 110 mA (maximum).

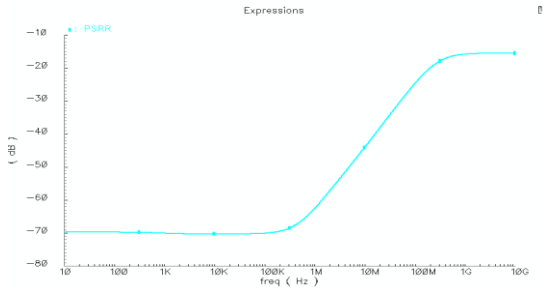


Fig. A.11: The simulated PSRR performance of the proposed LDO.

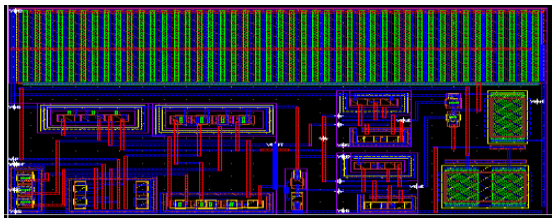


Fig. A.12: The Layout picture of proposed LDO.

Table 1: Performance comparisons of the proposed LDO with some existing works.

	[8]	[4]	[2]	[1]	This work
Year	2010	2011	2012	2012	2014
Technology	0.35µm CMOS	90 nm	0.35µm CMOS	65nm CMOS	90 nm
Vin (V)	1.5-3	1.2	1.2-1.5	1.15-1.3	1.2
Vout (V)		1	1	1	1
Dropout voltage (mV)	300	200	200-500	150-300	200
I_Q (µA)	26	408	45	150-350	26
Imax (mA)	100	100	50	25	110
Load capacitor range for stability (pF)	0.1µF	0–1000 pF	0-1nF	4-4.7 µF	0-100nF
PSRR@100KHz (VOUT = 1 V, IOUT = 110 mA)	*	-36dB (VOUT = 1 V, IOUT = 100 mA)	*	-61 @1MHz	-70 dB (VOUT = 1 V, IOUT = 110 mA)
PSRR@10 MHz (VOUT = 1 V, IOUT = 110mA)	*	-9dB (VOUT = 1 V, IOUT = 100 mA)	*	-47 @10MHz	-45 dB (VOUT = 1 V, IOUT = 110 mA)
FOM (ns)**	*	0.142	0.15	4.88	0.025
Transient load Regulation ΔVout (mV)	44.9 (tr = 0.2µs)	95/17/5 (tr = 0.1 ns/100 ns/1 µs)	70 (tr = 4µs)	8 (tr=100 ns)	12/20 (t_r = 100ns /1 µs)

**The load transient response time (TR) shown in the figure of merit (FOM = t r * IQ / Iload,Max) of the LDO is given by tr = Cout ΔVout / Iload, Max , where ΔVout is the maximum transient output voltage variation.
*Not available

REFERENCES

Young-Sub Yuk, Seungchul Jung, Byunghun Lee, Se-Won Wang, Chul Kim, Gyu-Hyeong Cho, 2012. "This is my paper A CMOS LDO Regulator with High PSR Using Gain Boost-Up and Differential Feed Forward Noise Cancellation in 65nm Process", IEEE 978-1-4673-2213- 3/12/$31.00.

Gianluca Giustolisi, Member, IEEE, Gaetano Palumbo, Fellow, IEEE, Ester Spitale, 2012. "Robust Miller Compensation With Current Amplifiers Applied to LDO Voltage Regulators", IEEE Transactions On Circuits And Systems—I: Regular Papers, 59-9.

Ka Nang Leung, Member, IEEE, Philip K.T. Mok, Senior Member, IEEE , 2003. "A Capacitor- Free CMOS Low-Dropout Regulator With Damping-Factor-Control Frequency Compensation", IEEE Journal Of Solid-State Circuits, 38-10.

Suming Lai, Peng Li, 2012. "A fully on-chip area-efficient CMOS low-dropout regulator with fast Load regulation", Springer Science+Business Media, LLC.

Quan Zhou, Shuxu Guo, Qiang Li, Zhaohan Li, Jingyi Song, Yuchun Chang, 2012. "A Fully on-Chip LDO Regulator with a Novel PSRR Boosting Circuit ", IEEE 978-1-4673-2475-5/12/$31.00.

Chaitanya, K., Chava, Member, IEEE, José Silva-Martínez, Senior Member, IEEE, 2004. "A Frequency Compensation Scheme for LDO Voltage Regulators ", IEEE Transactions On Circuits And Systems—I: Regular Papers, 51-6.

Amit, P., Patel, Gabriel A. Rincón-Mora, 2010. "High Power-Supply-Rejection (PSR) Current-Mode Low-Dropout (LDO) Regulator", IEEE transactions on circuits and systems—II: express briefs, 57-11.

Pui Ying Or, Ka Nang Leung, 2010. "A fast-transient low-dropout regulator with load-tracking impedance adjustment and loop-gain boosting technique ", IEEE Trans. Circuits Syst- II, 57-0.