Sigma Delta Modulation Based Ternary FIR Filter Mapping on FPGA

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ABSTRACT

In this paper single-bit SDM (Sigma Delta Modulation) based TFF (Ternary FIR Filter) with balanced ternary coefficients (i.e. -1/0/+1) has been mapped on small commercially available FPGAs (Field Programmable Gate Arrays). Filter coefficients were obtained using second order sigma delta modulator. The filter structure is based on a hierarchical adder tree that can easily be pipelined for high performance purpose. Filter structure was coded in VHDL (Very High Speed Integrated Circuit Hardware Description Language) and simulated in Quartus-II software. The filter exhibits low I/O (Input Output) and core area usage and high performance-achieving clock speeds close to 200MHz on a low-cost FPGA and over 500MHz on a latest FPGA commercially available device. This single-bit ternary filter is intended to support video and audio processing applications in mobile communication systems.

Key Word: **Sigma Delta Modulation, FPGAs, Ternary FIR Filter, VHDL.**

1. INTRODUCTION

Single-bit SDM has been applied widely for the purpose of audio processing in systems such as mobile phones. Inherent advantages of these systems includes: simplicity of operation, low power consumption, stability and efficient hardware implementation. Recent technological advancement has wide spread the scope of SDM and it has been scaled to operate above 10MHz and to achieve a dynamic range beyond the 70dB. This has made the technique applicable to mobile handset receivers and transmitters [1-3].

Previously, SDM based systems were restricted to the PCM applications i.e. Analog to digital or digital-to-analog conversion, due to its incapability to perform the complicated DSP tasks using single-bit operation. However, a SWL (Short Word Length) SDM system that operates in the range of 1-3 bits, were introduced in last decade that has proved cost effective and efficient solutions to replace the current general purpose DSP applications including LMS adaptive filtering [4-7]. The key advantage of short word-length systems is that they do not require complex integer multiplication hardware, these being replaced by simple multiplexers [4,5,8-7]. Using FPGAs these simple arithmetic DSP systems can take a great advantage of the lower chip-area that reflects the reduced latency and improved throughput [9]. In addition, an FPGA based hardware implementations are easy to reconfigure and flexible to tailor the word length according to the desired application [9]. To take a full advantage of

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the sigma-delta based DSP designs, it is required that input bit-stream and coefficients of the TFF operate with values of +1/0/-1 [7,10]. Due to ternary nature of the coefficients SQNR (Signal to Quantization Noise Ratio) improves with an order of 7-9 dB as reported in [11-12].

Much work has already been reported on the cost-efficient design of FIR filters over the last two decades using distributed arithmetic, systolic distributed arithmetic, and parallel processing etc. Most recently new algorithms has been proposed to overcome an issue of latency in FIR filters and improve the throughput [13-14]. Additionally, area-performance tradeoffs have been reported using conventional multi-bit techniques. Although it has shown some advantage over the old techniques but complexity of the multiplier doesn't change due to its multi-bit nature.

Towards this end, we have introduced the TFF implementation using VHDL in FPGA [3]. Here, we extend that paper and present the revised version with additional information and demonstrate the organization of a novel design of ternary sigma delta modulation based FIR filter simulated using small commercial FPGA devices. This work will culminate with the design of new SWL high performances adaptive filter modules targeting both video and audio applications in the mobile communication domain. Section 2 outlines the general design of TFF with ternary taps, and generation of ternary coefficients in Matlab. In Section 3, introduces the implementation, synthesize and simulation aspects of the TFF. While in Section 4, paper has been summarized with conclusion remarks and future work.

2. Sigma Delta Modulation Based Ternary FIR Filter

In a broad sense, SWL encompasses all the types with low bit counts i.e. DSP systems for which the input, internal processing and output are all in 1, 2 or 3 bit format. Single-bit is a special case of SWL DSP systems where the input and output are in single-bit format i.e. binary (+1/-1). In our work Ternary (and ternary filters) refers to the case where the coefficients and/or data exist in the set {+1/0-1}. Whereas Balanced Ternary FIR Filter has similar structure as conventional FIR filter as shown in the general block diagram of Fig. 1, i.e. a FIR ternary filter comprises a tapped single-bit delay line followed by a coefficient multiplication stage and finally the addition of the partial products. As ternary filter coefficients are generated by SDM (Fig. 4) that operates at high OSR (Over Sampling Ratio) than the Nyquist rate so the design of an efficient single-bit ternary FIR filter typically requires a very large number of coefficient taps (e.g. in excess of 1024). In a SWL ternary filter, the tap coefficients will take the values of +1, 0 and -1, while the input data values, x(k), may either be single-bit (binary) or ternary, depending on the application. As a result, the complex MAC (Multiply and Accumulate) block stages generally and multiplication especially will be restricted to a simple bit-wise AND/OR logic or a small LUT (Look-Up Table). Thus there may be variety of techniques to deal with the partial products addition i.e., serial, parallel, bit-wise serial etc. However, here it has been dealt with parallel processing of large number of partial products that is discussed in the following section.

Mathematically the ternary FIR filter output y(k) is a convolution sum of its ternary coefficients w_j and the input signal u(n). If K is the order of the filter then the output of the filter is:

$$y(n) = \sum_{j=0}^{K} w_j u(n-j) \quad (1)$$

In the implementation described here, the tap values (i.e. order of the filter K) have been generated via SDM of the target impulse response. The process commences with a target low pass filter impulse response (Fig. 2) that may be derived using any suitable design algorithm. We have used the Remez exchange method to derive the filter coefficients then interpolated before encoding to a ternary format (Fig. 3) [7] . Thompson, A.C., et. al. [15], sigma delta modulation based FIR filter performance has been

evaluated at different oversampling (i.e. interpolation) and proposed that FFT is the best technique that offers good SQNR and has been used in this paper.

The digital ΣΔM used to generate the ternary filter taps must have two properties i.e. tri-level quantizer (i.e. +1/0/-1) and second, the ΣΔM should exhibit a flat signal frequency response over the desired bandwidth f_0 of the signal. Second order sigma delta modulation structure used in this paper is shown in Figure 4. This second order sigma delta modulator z-domain transfer function is given as [7]:

$$H(z) = G(z)z^{-1} + N(z)(1-2z^{-1} + z^{-2}) \quad (2)$$

where G(z) and N(z) represents the target impulse response and quantization noise transfer function. In Equation (2), the filtering term, $(1-2z^{-1}+z^{-2})$ embedded with noise N(z), assures the noise shaping affect of the ΣΔM. The frequency response of the above ΣΔM is given by:

$$H_{\Sigma\Delta T}(e^{j\Omega}) = G(e^{j\Omega})e^{-j\Omega} + N(e^{j\Omega})(1-2e^{-j\Omega} + e^{-2j\Omega}) \quad (3)$$

where $\Omega=2\pi f/f_s$ is the normalized radian frequency.

The ternary filter design assumes that the input signal is ΣΔM modulated with values of +1/-1 and that it operates at a specific OSR. As noted above, the input might alternatively be ternary encoded (1,0) but this will not alter the filter operation. The SQNR can be improved by increasing the OSR. For example, in a second order M the

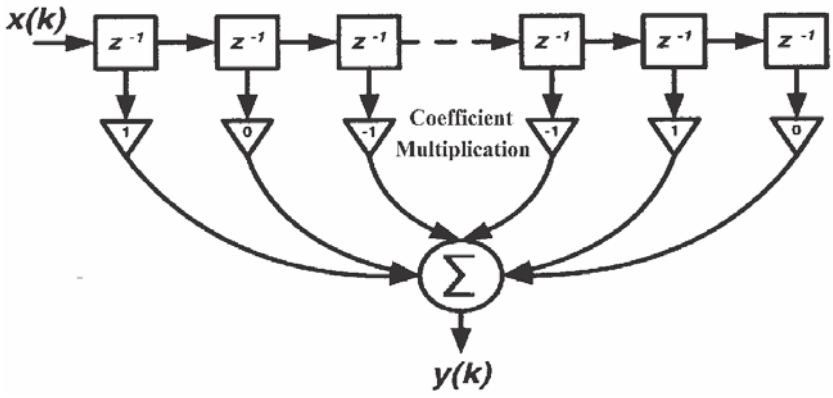

FIG. 1. GENERAL BLOCK DIAGRAM OF A TERNARY FIR FILTER [7]

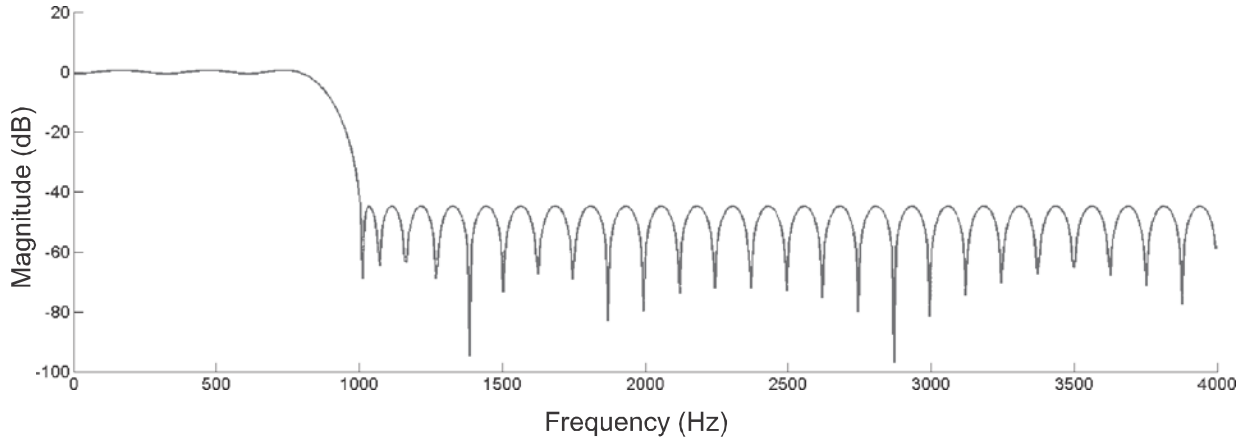

FIG. 2. TARGET IMPULSE RESPONSE OF THE FIR FILTER

SQNR can be improved by 15dB with each doubling of the OSR [16]. For the filter explored here (with 1024 taps) we have used an OSR of 32. Clearly, the upper bound on the Nyquist rate for the filter is related to the OSR and the maximum achievable clock frequency (F_{MAX}) for the implementation. For example, operating on a video signal with a 6MHz bandwidth and an OSR of 32 would mandate an FMAX in excess of 200MHz.

3. VHDL Design of Ternary FIR Filter

As identified in Section 2, the operation of a TFF (Fig. 1) has transversal structure i.e. comprising of input delay line with multiplication of coefficients and followed by the addition of the large number of partial produces e.g. K=2048. Noting that order of the ternary filter (i.e. K) is the multiplication of OSR by multi-bit coefficients number i.e. OSR*M. In transversal structure, coefficients symmetry can have advantage of less chip area and better performance but here is not the case due to oversampling ratio and its ternary nature. Thus we have considered K taps multiply blocks followed by an adder tree with $\log_2 K$ levels to perform the summation. We have already mentioned that input to the SWL DSP systems should be in binary/ternary format that would offer better SQNR [17]. Thus, both the input and coefficients can easily be mapped on FPGA using a two-bit two's-complement representations (+1=01, -1=11, 0=00). Therefore, assuming K=2048, and summing over this number implies 11 levels adder tree and the one final multi-bit result is +K. However, 13 bits are necessary to represent the range of ±2048, due to 2's complement approach that is offset around zeros. As it is evident that two-bit multiplication will reduce the delay path and chip-area that is the key advantage of SWL systems. Multiplication becomes trivial and can

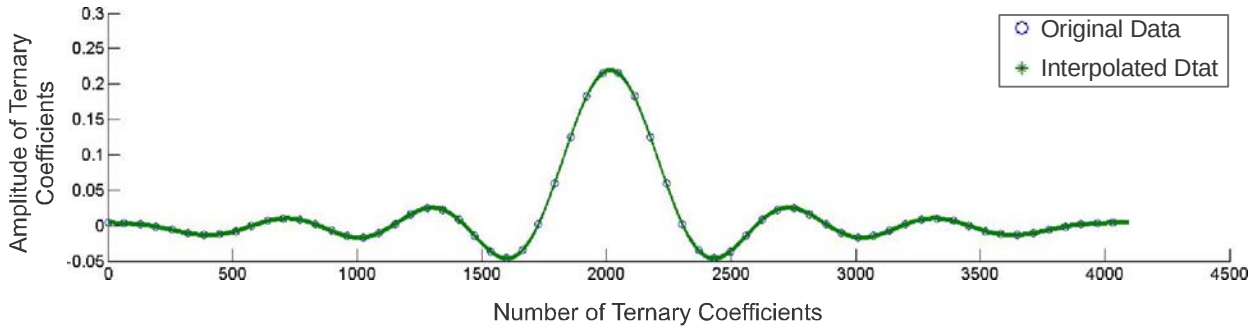

FIG. 3. INTERPOLATED TERNARY FORMAT OF COEFFICIENTS

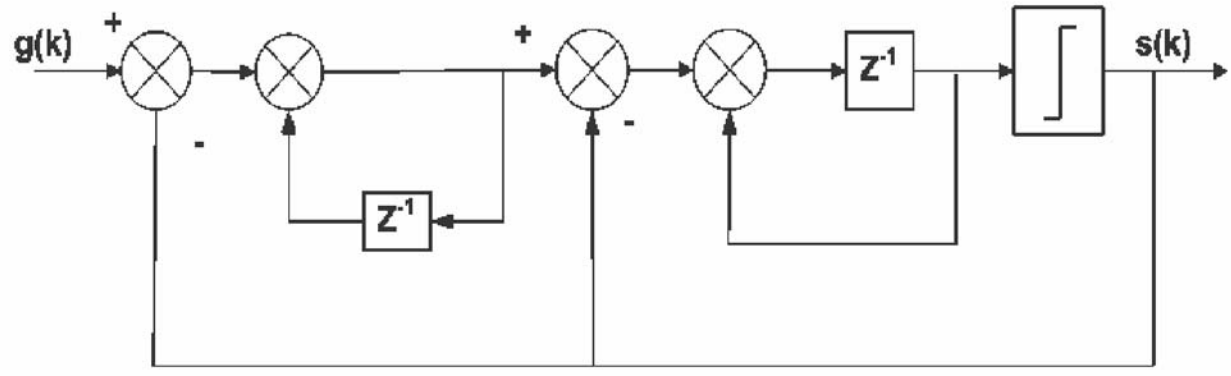

FIG. 4. BLOCK DIAGRAM OF A SECOND-ORDER MODULATOR

easily be implemented using simple gate logic or multiplexers instead of complicated multiplication stages that reduces the performance and increase the delay path. These two-bit multiplications in FPGA means a small LUT can be mapped easily even with the simplest devices available in the market like: cyclone-III.

Chen, D., [18], test bench approach was used to generate the HDL code through Matlab and Wallace adder tree is used for overall sum. In this paper, we have taken more general approach of distributed arithmetic in designing FIR filter with single-bit ternary coefficients [19]. We have defined small adder and multiplier blocks that best suits the application. In this way, design of TFF with simple LUT or AND-OR logic offers efficient solution that can easily be mapped on FPGA organization without requiring complex IP blocks.

The general block diagram of the TFF is shown in Fig. 5. In this block diagram, if we consider K=2048, then it makes the 11 adder stages as discussed above. Thus, at every stage of the adder the number of adder blocks becomes half while their length increases by one bit and finally gives 13 bit output. Small fragment of the adder tree developed for this design is shown in 0. In the available commercial FPGA devices LUT structure has capacity to take a small number of inputs (i.e. 6-8), so the first 3-4 adder stages will be mapped to individual LUT blocks in the FPGA architecture that will operate in concurrent. However, the rest of adder tree stages will comprise small ripple-carry blocks up to thirteen bits long. Here we can use the optimised IP blocks already provided for reconfigurable purpose. Thus, the designed FIR filter has been analysed using more general approach so that our final results can be considered to be worse-case comparable. In any case, for the short adder structures generated by this approach (<12 bits), we have observed little or no performance advantage in choosing complex techniques such carry-look ahead or redundant binary encoding schemes over simple ripple-carry organizations.

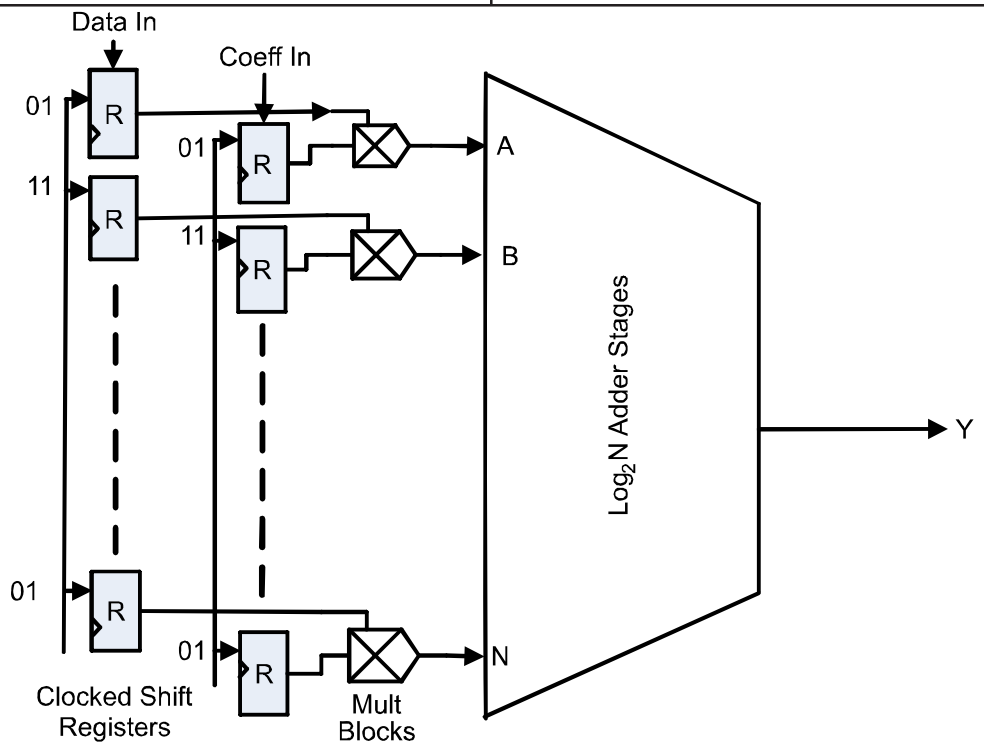

FIG. 5. GENERAL STRUCTURE OF THE TFF THE PIPELINED VERSION PLACES REGISTERS AT THE SITES SHOWN I.E. THE OUTPUT OF THE MULTIPLIER AND BETWEEN EACH STAGE OF THE ADDER TREE

3.1 Simulation of Ternary FIR Filter

The FIR filter design was created using VHDL and synthesized using Quartuss-II 9.1 targeting small commercial small number of Altera Cyclone and Stratix FPGAs-chosen as representative of a range of FPGA components from low-cost to through to high performance.

The design was explored using two different approaches, i.e. pipelined and non-pipelined. The non-pipelined version has a single 12-bit result register at the output of the adder block (considering K=1024) (Fig. 6) so that F_{MAX} is limited by the propagation delay of the 10-level adder blocks. The pipelined version places registers at the output of the multiplier and each stage of the adder tree so the primary limitation is the final 12-bit adder stage. The simulated results of both the designs with various FPGA devices are given in Table 1. Assuming an OSR of 32, it can be seen that we can easily process audio signals with any of the implementations, even the non-pipelined configurations. Processing a 6MHz video signal is also possible with most of pipelined implementations. The high performance Stratix IV device would be capable of supporting OSR values of more than 80, offering greatly improved filter performance in exchange for a significantly higher component cost and the larger power consumption implied by the increased operating frequency.

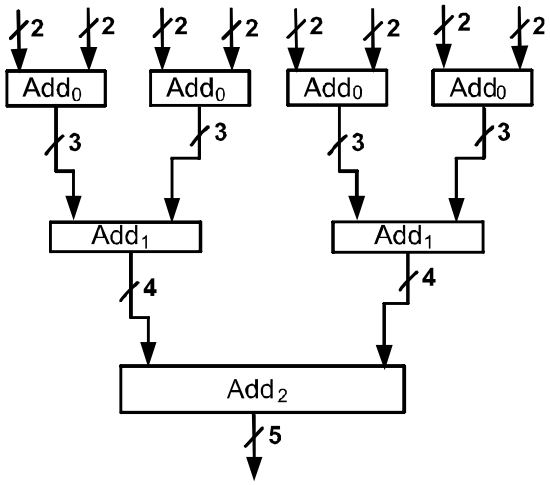

FIG. 6. FRAGMENT OF ADDER TREE USED FOR TERNARY FIR FILTER

TABLE 1. MAPPING RESULTS ON SELECTED ALTERA FPGAs

Device	Configuration	Area (# Elements)		F_{MAX} (MHz)
		Comb.	Registers	
Cyclone-II	Non-Pipelined	7124	3084	62.6
EP2C15	Pipelined	10658	9202	190.3
Cyclone-III	Non-Pipelined	7422	3084	60.1
EP3C10	Pipelined	9972	9202	198.3
Stratix-II	Non-Pipelined	5462	3093	85.3
EP2S15	Pipelined	6810	9204	423.0*
Stratix-III	Non-Pipelined	5473	3089	120.2
EP3SE50	Pipelined	6818	9210	587.5*
Stratix-IV	Non-Pipelined	5392	3092	117.8
EP4SGX230DF	Pipelined	6803	9203	518.4*
*Internal Clock Rate, I/O Pin Limited to Lower Frequency				

4. CONCLUSIONS

In this paper, TFF was designed and simulated using VHDL in Quartus and ModelSim that is suitable for audio and video stream processing in mobile communication. This filter offers speeds around 200MHz when it was operated using the traditional hierarchical pipelined adder tree that offers operating speeds around 200MHz using a low-cost FPGA available in the market. While using a state-of-the art high-tech commercially available FPGA e.g., the 40nm Stratix IV the filter offers the clock speed in excess of the 500MHz, that can easily support video data rates at an OSR of over 64. The filter operates on small 2's complement binary numbers and does not use any built-in specialised DSP blocks such as fast multipliers and thus occupies only a small part of the FPGA-for example, around 2% of the Stratix IV device.

Single-bit SDM based systems (i.e. SWL Systems) offer a high performance and low-area solution to DSP systems with application in mobile communication systems as well as more general DSP disciplines such as bio signal processing, telemedicine, telecommunication, robotics, and others. The current implementation uses a fixed coefficient set derived from the impulse response of the target filter. In future work we will expand this to encompass adaptive SWL systems, where the coefficients are derived from an analysis of the bit stream during operation.

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