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Mitigation of Power Quality Problems with Reduced Switches Using Unified Power Quality Conditioner

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ABSTRACT:

This paper presents a control strategy for a three phase unified power quality (UPQC) for an improvement of different power quality problems. The UPQC is realized by integration of series and shunt compensation system. The shunt and series system is realized using a three phase, three leg voltage source inverter (VSI). A control technique based on unit vector tempulate technique (UTT) is used to get the reference signals for transmission line, while Icosφ algorithm is used for the control of shunt, series transsformer. The performance of the implemented control algorithm is evaluated in terms of voltage sag, swell and voltage dip in a three phase transmission system for different combination of linear and non linear loads. In this control method, the current voltage control is applied over the fundamental supply currents/voltage instead of fast changing current s voltages, thereby reducing the computational delay and the required sensors. MATLAB simulink based simulations results are obtained, which support the functionality of the UPQC.

Index Terms – Cogging Torque, FEM Analysis, Flux Distribution, Saturation**.**

1. INTRODUCTION

The power quality has become one of the most significant issues for power electronics engineers. Mainly, in signal processing, control systems and power electronics, the load characteristics have changed completely, these non linear current degrade electric power quality. The quality degradation leads to low power factor, low efficiency, leads to overheating of transformers. Preferably, voltage and current waveforms are in phase, power factor of the load equals unity, and the reactive power consumption is zero. As represented in fig.1 UPQC is a combination of series and shunt winding.

It compensates reactive current of the load and improves power factor. There are many control strategies reported in the literature to determine the reference value of the voltage and current of the three-phase system, the most common are the p-q-r theory, the modified single phase p-q theory, synchronous reference frame (SRF) theory, symmetrical component transformation and unit tempulate technique etc. Apart from this one cycle control (OCC) (without reference)

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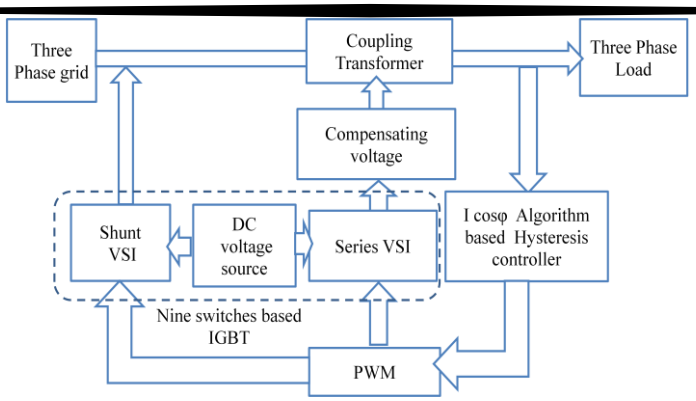

Fig.1. Representation of block diagram

The performance of the above mentioned control schemes was mostly affected under distorted and unbalanced supply voltage, while Icosφ theory has potential of the working under distorted as well as unbalance supply voltage. Therefore the proposed work presents an application of I cosφ theory with an in direct control for the shunt system of three –phase three-wire UPQC, extending the scheme for three-wire transmission system with additional advantages of fast computation and less numbers of current sensors. In this control algorithm the current /voltage control is applied instead of fast changing currents/voltage, thereby reducing the computational delay. In order to mitigate the, voltage sag, swells and voltage dips the UTT theory is used because apart from its simplicity, it gives a flexibility to generate the desire reference signals of require amplitude. The proposed control technique is capable of extracting most of the load current and source voltage distortions successfully. The series winding is controlled voltage regulation against voltage sag, swells and voltage dips while, the shunt winding is controlled to alleviate the reactive power and load balancing.

2. CONTROL SCHEME OF SERIES SYSTEM

The series is controlled in such a way that it injects voltage (Vinja, Vinjb, Vinjc), which cancel outs the distortions presents in the supply voltages (Vsa, Vsb, Vsc), thus making the voltage at PCC (Vla, Vlb and Vlc) perfectly sinusoidal with the desired amplitude. In other words, the sum voltage makes the desired voltage at the load terminals, the control strategy for the series system. Since the voltage is distorted, a phase locked loop (PLL) is used to achieve synchronization with the supply voltage. Three-phase distorted supply voltage are sensed and given to PLL which generates two quadrature unit vectors (sin wt, cos wt).The in-phase sine and cosine outputs from the PLL are used to compute the supply in phase 120·

The displaced three unit vectors (u_a , u_b,u_c) using equation is given by,

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} = \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix}$$

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The computed three phase unit vector multiplied with desired peak value of the PCC phase voltage (V^*_{lm}) which becomes the three- phase reference PCC voltage as,

$$\begin{bmatrix} v^*_{la} \\ v^*_{lb} \\ v^*_{lc} \end{bmatrix} = v^*_{lm} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}$$

The compute reference voltage from equation are then given to the hysteresis controller along with the sensed three phase PCC voltage (v_{la},v_{lb} and v_{lc}). The output of the hysteresis contoller is switching signals to the nine switches of the VSI of the series transformer. The hysteresis controller generates the switching signals such that the voltage at PCC becomes the desired sinusoidal reference

$$I^*_{sp} = \{I_{La}|\cos\phi_a + |I_{Lb}|\cos\phi_b + |I_{Lc}|\cos\phi_c + I_d\}3$$

Where $V_{de(n)} = V_{dcr} - V_{dca(n)}$ denotes the error in V_{dc} calculated over reference value of V_{dc} and average value of V_{dc}. K_{pd} and K_{id} are proportional and integral gains of the bus voltage I cosφ controllers. The three phase component of the source currents can be obtained from this model.

3. WORKING PRINCIPLE

The three phase source voltage is given to non-linear a load which consists of three phase IGBT converter with series and parallel transformer is connected with the non linear load. The system under consideration for the three phase three wire distortion system shown in fig. the UPQC is connected before the load to make the source and load voltage free from any distortions and at the same time, the reactive current drawn from source should be compensated in such a way the current at source side is, would be in phase with utility voltage ,provisions are made to realize voltage harmonics, sag and swell in the source voltage by switching on / off the three phase power module load, R-L ,RC load respectively.

A voltage dip in the load voltage is created by switching on an induction motor on the load side. The UPQC, realized by voltage source converter is shown. one acting as a shunt unit system, while series unit system the implemented control algorithm consists mainly of the computation of three phase reference voltage of load voltage (V*la, V*lb, V*lc) and the reference currents for the source current (i*sa, i*sb, i*sc).The voltage at the source side before UPQC the load voltage at load. The voltage injected by series unit system and the DC voltage between converter are represented by V_s, V_L, V_{inj} and V_{dc} respectively. Whereas the current on the source side, load current and the current injected by shunt unit system are represented by is and is respectively.

The three phase load voltage and load currents are sensed and given to the controller circuit. In order to extract the fundamental component of voltage and current Icosφ algorithm is used. The extracted value is compared with actual value to get the error signal, which is given as input to the Icosφ based hysteresis controller. Icosφ hysteresis controller produces the gating

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signal to the IGBT inverter, which in turn inject the voltage content into phase in direction. Thus the load voltage and load current gets compensated.

4. SYSTEM DESCRIPTION OF NINE SWITCH POWER CONDITIONER

Table 1.Phase-leg voltage of nine-switch converter

Switch state	Voltage
S1=S2=ON and S3=OFF	$V_{AN}=V_{DC}$ and $V_{RN}=V_{DC}$
S1 = S3 =ON and S2 = OFF	$V_{AN}=V_{DC}$ and $V_{RN}=0$
S2= S3 = ON and S1 = OFF	V_{AN} and $V_{RN}=0$
Other combinations are combinations are not permitted	

Figure.2 shows the per-phase representation of the common back-to-back unified power quality conditioner (UPQC), where a shunt converter is connected in parallel at the point-of common-coupling (PCC), and a series converter is connected in series with the distribution feeder through an isolation transformer.

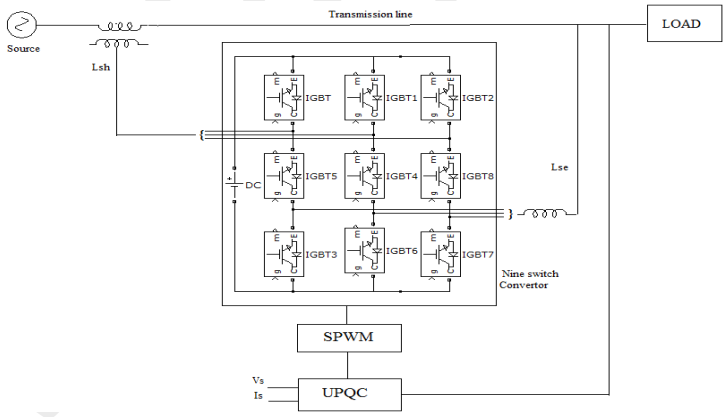

Figure 2 Representations of nine-switch power conditioners

The shunt converter is usually controlled to compensated for load harmonics, reactive power flow, and unbalance, so that a grid, regardless of the extent of load nonlinearity. Complementing, the series converter is controlled. A set of three-phase fundamental voltages always appears cross the load terminals rather than described, the inverse assignment of functionalities with the shunt converter regulating voltage and series converter regulating current is also possible, as demonstrated in. Being so flexible, the UPQC is indeed an excellent "isolator," capable of promptly blocking disturbances from propagating throughout the system. Despite its popularity the block diagram of UPQC is none the less still complex and quite not utilized, although it offers independent control of two decoupled converters.

Its underutilizations largely attributed to the series converter, whose output voltages are frequently small, where only small amount of grid harmonics need to be compensated by it under normal and steady-state conditions and especially for strong grids (_*V*SUPPLY ≈ _*V*LOAD). Some typical numbers for illustration can be found, where it is stated that the converter modulation ratio can be as low as 0.05 × 1.15 with triplen offset included, while the converter is sized to introduce a series voltage of 1.15 p.u. during sag occurrence. Such a low modulation ratio gives rise to computational problems, which fortunately have already been addressed in, but not its topological underutilization aspect. Resolve the topological aspect is, however, not so easy, especially for cases where the dc-link voltage must be shared and no new component can be added. Tradeoffs would certainly surface, meaning that the more reachable goal is to aim for an appreciable reduction in component count, while yet not compromising the overall utilization level by too much.

Offering one possible solution then, this paper presents an integrated power conditioner, implemented using the nine-switch converter documented in, rather than the traditional back-to-back converter. Before the nine-switch converter can be inserted though, its impact should be thoroughly investigated to verify that there would not be any overburdening of system implementation cost and performance. This recommendation is advised as important, since earlier usages of the nine-switch converter for motor drives and rectifier–inverter systems have so far resulted in some serious limitations, which would be brought up for discussion shortly to highlight certain insightful concepts.

5. NINE-SWITCH CONVERTER OPERATING PRINCIPLES AND EXISTING CONSTRAINTS

As illustrated in Figure.2 the nine-switch converter is formed by tying three semiconductor switches per phase, giving a total of nine for all three phases. The nine switches are powered by a common dc link, which can either be a micro source or a capacitor depending on the system requirements under consideration. Like most reduced component topologies, the nine-switch converter faces limitations imposed on its assumable switching states, unlike the fully decoupled back-to-back converter that uses 12 switches. Those allowable switching states can conveniently be found in Table I, from which, it is clear that the nine-switch converter can only connect its two output terminals per phase to either *V*dc or 0V, or its upper terminal to the upper dc rail *P* and lower terminal to the lower dc rail *N*. The last combination of connecting its upper terminal to *N* and lower terminal to *P* is not realizable, hence constituting the first limitation faced by the nine-switch converter. That limitation is nonetheless not practically detrimental, and can be resolved by coordinating the two modulating references per phase, so that the reference for the upper terminal is always placed above that of the lower terminal, as per the two diagrams. Imposing this basic rule of thumb on reference placement then results in those gating signals for the three switches of *S*1, *S*2, and *S*3 per phase. Equations for producing them can also be explicitly stated as

$S_1 = S_1' =$ ON, if upper reference is larger than carrier

OFF, otherwise

$S_3 = S_3' =$ ON, if upper reference is smaller than carrier OFF, otherwise

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$$S_2 = S_1' \oplus S_3' \qquad (1)$$

Where $\oplus$ is the logical XOR operator. Signals obtained from (1), when applied to the nine-switch converter, and then lead to those output voltage transitional diagrams for representing V_{AN} and V_{RN} per phase. Together, these voltage transitions show that the forbidden state of VAN = 0 V and VRN = Vdc is effectively blocked off. The blocking is, how- ever, attained at the incurrence of additional constraints limiting the reference amplitudes and phase shift. These limitations are especially prominent for references having sizable amplitudes and/or different frequencies, as exemplified by the illustrative cases.

In particular, Figure,3 shows two references of common frequency limited in their phase dis-placement, while shows two references of different frequencies limited to a maximum modulation ratio f 0.5each, extendible by 1.15 times if triplen off set is added , in order to avoid cross over.

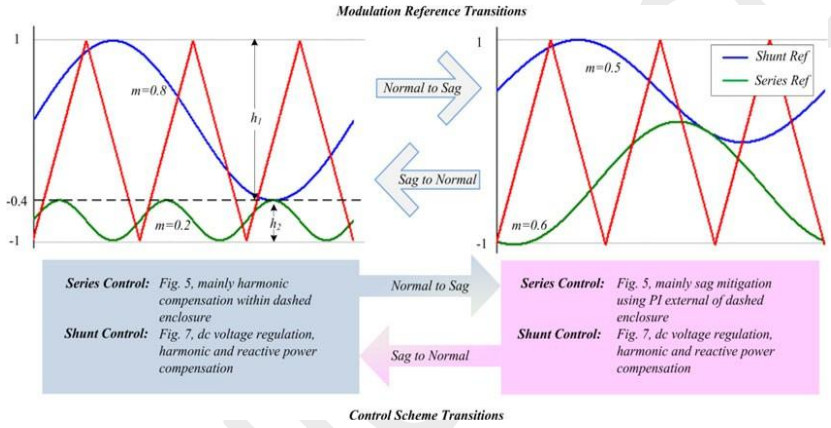

Fig.3 transition of modeling reference and control scheme between normal (left) and sag mitigation (right) mode

The limited phase-shift constraint, associated with references of the same frequency and combined modulation ratio of greater than 1.15 with triplen offset added (=1.2in Figure.3 as an example), has recently been shown to adapt well with online uninterruptible power supplies, which in deed is a neat and intelligent application of the nine-switch converter. This, however, is only a single application, which by itself is not enough to bring forward the full potential of the nine-switch converter.

Considering now these limitation detailed, a help full example for explaining it is the nine-switch dual drive system proposed in, where references used for modulation can have different operating frequencies. These references are for the two output terminal sets of the nine-switch converter, tied to separate motors operating at approximately the same rated voltage but at different frequencies. Such motor operating criteria would force the references to share the common carrier range equally, like that drawn in Fig.3.The maximum Modulation ratio allowed is therefore 0.5×1.15 per reference. Even though technically variable, such sharing of carrier is not practically favorable,

Since to produce the same output voltages, the dc-link voltage maintained, and hence semiconductor stress experienced must at least be doubled. Doubling of voltage is, however ,

not needed for the traditional dual converter, whose topological structure is similar art the back-to-back converter, and hence would also support a maximum modulation ratio of unity quite then , doubling of dc-link voltage is attributed of to the halving of modulation ratio imposed by the nine switch converter, and is there for equally experienced by the AC-DC- AC adjustable speed motor drives recommended in where the nine switch converter is again operating at different principle .Judging from these examples, the general impression formed.

Is that the nine-switch converter is not too attractive, since its semiconductor saving advantage is easily had owed by trade- offs, especially for cases of different terminal frequencies. Such un attractiveness is however not universal, but noted here to link only with those existing applications reported to date, where the nine-switch converter issued to replace two shunt-connected converters.

References demanded by these shunt converters are usually both sizable, inferring that the carrier band must be shared equally between them, and hence giving rise to those tradeoffs identified earlier. Therefore, instead of "shunt–shunt" replacement, it is recommended here that the nine-switch converter should more appropriately be used for replacing series and a shunt converter like those found in a power quality conditioner or any other "series–shunt" topological applications. Explanation for justifying that recommendation is provided in Section II- C with all relevant advantages and residual tradeoffs identified.

5. PROPOSED NINE SWITCH POWER CONDITIONER

Under normal operating conditions, the output voltage amplitude of the shunt converter is comparatively much larger than the voltage drop induced by the series converter along the distribution feeder. That indirectly means the modulating reference needed by the shunt converter is much larger than that associated with the series converter, which mighty simply consist of only the inverse harmonic components for grid voltage compensating purposes. Drawing these details in the carrier range would then result in a much wider vertical range h1 in the left diagram of figure.3 for controlling the upper shunt terminal (h1>>h2).other operating details like logical equations used for generating gate signal for the three switches per phase would remain and unchanged.

For h2, a command rise here is that it can be set zero, if an ideal grid with no distortion and rated sinusoidal voltage is considered. In that case the lowest three switches, labeled else S3 for each phase in Figure 3, should always be kept ON to short out the series coupling transformer and to avoid unnecessary switching losses. The series transformer can also be bypassed the grid side to remove unwanted leakage voltage drop without affecting the compensating ability of the shunt converter.

Referring back to the h1 and h2 carrier band division shown in the illustration of fig 3 it would still need a higher dc link voltage as trade off in the UPQC, but increase is much reduced and indefinitely not anywhere close to doubling. Quoting as an example, where a modulation ratio of the series converter can be as low as 0.05*1.15 with triplen offset included, the increase in dc-link voltage is merely about 5%,before the same maximum shunt voltage amplitude, like in a back-to-back converter, can be produced by the nine-switch converter.

This maximum is however arrived at a reduced maximum modulation ratio of 0.95*1.15 with triplen offset considered. The scenario would somehow be improved slightly, if an ideal grid is considered instead, in which case, h2 is set to zero, as explained in an earlier paragraph. No increase in DC link voltage is then needed and the maximum shunt voltage amplitude can be produced at the ratio of 1.15.

Replacing of series shunt converter by the nine switch converter by the nine switch converter is therefore an acceptable option with it saving of three conductor switches viewed here as more profound since they represent heavily underutilized switches founded in the back to back converter for series compensation purposes. The another issue to address, before the nine switch converter can be confirmed as favorable topology for the series shunt power conditioner, is to study its compensating ability under voltage sag condition. For that purpose the PCC voltage in fig.2 is assumed to dip by some amount, which would then subject the higher shunt terminal of the nine switch converter to a reduced voltage level. In contrast the lower series terminal must respond immediately by injecting a sizable series voltage of the fundamental frequency ($V_{series}=V_{load}-V_{supply}$)where V_{load} is the demanded load voltage references, so as to keep the load voltage close to its perfect value.

Updating this sag operating scenario to the carrier domain then results in the shunt terminal using reduced reference, and the series terminal widening its reference range to include a sizable fundamental component, regardless of whether h2is initially zero for an ideal grid or taking a small value for a distorted grid, since both reference are now predominantly fundamental with sizable amplitudes, their placement can ended up like the example drawn on the right of figure.3 With the same earlier mentioned phase-shift limitation imposed. fortunately, this limitation will not hider the operation of the nine-switch conditioner ,since large injected series voltage with a demanding phase shift is usually accompanied by a severe sag at the PCC and hence a much reduced shunt modeling reference. The compressed shunt reference would then free up more carrier space below from it for series reference to vary within, as easily perceived from the example drawn on the right of fig.3.

In conclusion the proposed nine –switch power conditioner can indeed operate well under both normal and sag operating conditions, owing its auto complementary tuning of shunt and series reference within the single common carrier band. suitability of the nine switch converter for "series-shunt "replacement is therefore established without any stringent practical limitations encountered, unlike those existing "shunt –shunt replacements.

6. PROPOSED NINE-SWITCH UPQC

As shown in figure 3, the proposed nine-switch UPQC operates with its carrier band divided into h1,h2.the latter, being much narrower ,is for blocking small grid harmonics voltages from propagating to the load, which from the example described , is only about 5% of the full carrier band. The minimum dc-link voltage, and hence voltage rating of components, must then be chosen based on $V_{dc\text{-}NS}=1.05V_{dc\text{-}BB,}$ where subscript NS is used to represent "nine switch". Current rating wise, analysis of the nine-switch UPQC is slight different, because of its merging of functionalities to gain a reduction of three switches. Focusing first at he upper S1switch, maximum current flowing through it would be the sum of shunt (-k) and series (1+k) currents per phase when S1 and S2 are turned ON, and hence giving a final value of 1p.u being slight higher, the common maximum current flowing through S2 and S3 is

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(1+k)p.u which flows when S1and S2 are turned ON for the former, and S1and S3 are turned ON latter.

Note, however that these maximum currents are only for sizing the switches, and should not be exclusive used for computing losses. The reason would be clear after considering S1as an example, where it is noted that the maximum current of 1p.u.does not always flow .in fact, then S1and S2 are turned ON, the current flowing through S1 is smaller at kp.u. The duration depends on a number of operating parameters like modulation ratio, phase displacement. Analytical computation of losses is therefore nontrivial, as also mentioned, whose simulation approach is now practiced here for computing the UPQC losses. Obtained results for both normal and sag operating are subsequently summarized in table II for easier referencing.

7. NINE-SWITCH UPQC WITH ONLY COMMON FREQUENCY

Nine-switch UPQC constrained to operate with the same common frequency (CF) at its shunt and series terminals, is not able to compensate for harmonics grid voltages, parameter h2 in figure.3 .is therefore redundant, and can be set to zero, whose effect is a minimum dc-link voltage that is no different from that of that of the back-back UPQC the series transformer, being no longer used, can also be bypass to avoid unnecessary leakage drop, and to divert the large load current away from the UPQC, leaving the three switches per phase to condition only the –k shunt .among the switches, the lowest S3 switched behaves differently in the sense that it is always turned ON, as explained in sectionII-c.and therefore produces only conduction losses, it will only start to commutate when a sag occurs, and the transformer exist its bypassed state. When that happens, the load current again flows through the switches.

8. SIMULATION RESULTS

The waveform of distribution system for unbalanced condition using UPQC is given as,

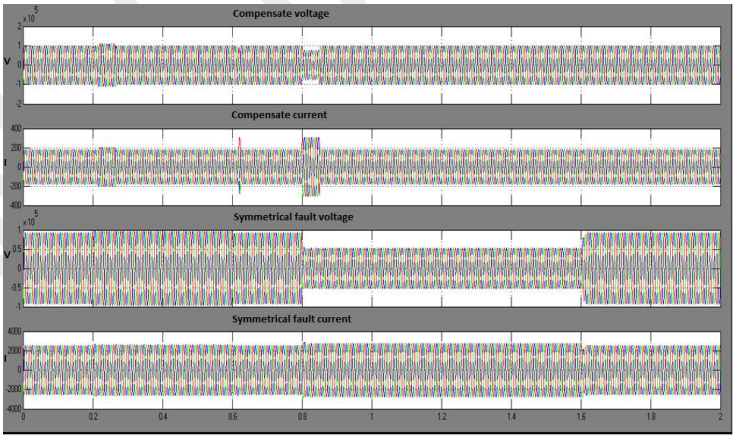

Fig 4. Transmission Line Voltage Waveform with UPQC

From the figure.4 we can observe that the voltage distortion in all phases and conductor current is reduced while fundamental component remains unaffected. The voltage sag and sag has been suppressed to a great value.

9. CONCLUSION

The project has outlined the design of controller for Icosφ. The observed performance has demonstrated the ability of the proposed unit template control technique to compensate the Transmission Line voltage, current and Reactive power compensation at PCC, The scheme has the advantage of simplicity and effectiveness. In this study, a Icosφ controller with fast dynamic response to regulate distorted transmission voltage, load current and reactive power in three-phase system was presented and analyzed. The simulation results show a very good performance of the proposed algorithm and control scheme under arbitrary fault conditions of the utility supply. It has been observed that the system has a fast dynamic response with the proposed control scheme.

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