



## Implementation of Single-Phase DVR-BES Based on Unit Vector Template Generation (UVTG) to Mitigate Voltage Sag Using Arduino Uno and Monitored in Real-Time Through LabVIEW Simulation

Yohanes Artha Setiawan<sup>1</sup> Amirullah Amirullah<sup>1\*</sup>

<sup>1</sup>Electrical Engineering Study Program, Faculty of Engineering,  
 Universitas Bhayangkara Surabaya, Surabaya 60231, Indonesia

\* Corresponding author's Email: amirullah@ubhara.ac.id

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**Abstract:** This paper aims to design and implement a single-phase dynamic voltage restorer (DVR) supplied by battery energy storage (BES) using load voltage controlled by the unit vector template generation (UVTG) method. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used for monitoring the parameter in real-time during 80% voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain total harmonic distortion (THD) of the source current and load current. The single-phase DVR system is connected to load i.e. a 5-watt bulb lamp (linear-load), 5-watt fluorescent (FL) lamp (non-linear load), and 5-watt light-emitting diode (LED) lamp (non-linear load). During voltage sag, the single-phase DVR-BES system is able to maintain load voltage i.e. bulb lamp, FL lamp, and LED lamp of 216 volts, 256 volts, and 185 volts, respectively. The percentage of load sag voltage deviation for each load is 6.4%, 26.13%, and 8.87%, respectively. The measurement of source power-factor with voltage sag results in source true power factor of three loads of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively. On the same system with voltage sag, single phase DVR-BES is able to result in source current THD for three loads of 1.523%, 1.523%, and 1.010% respectively. The proposed study is able to give the best performance because it is able to produce source current THD lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

**Keywords:** Single phase DVR, BES, Arduino uno, LabVIEW, Voltage sag.

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### 1. Introduction

During the last decade, there has been an increase in the number of sensitive and critical loads. On the other hand, the use of these tools also has an impact on deteriorating Power Quality (PQ). Among a number of PQ problems, problems related to voltage mitigation are also of increasing importance from a sensitive load and customer point of view. PQ problems related to voltage i.e. voltage sag, voltage swell, voltage harmonics, fluctuations, interruptions, and imbalance. In accordance with IEEE 1346 [1] and IEEE 1159 [2] standards, the sag voltage is defined as the RMS (root mean square) AC voltage sag with a magnitude of 10% to 90% of the nominal

voltage, at power frequencies with a duration of 0.5 cycles to one minute. The voltage sag is caused by a single-phase short circuit to ground in the power system, starting in large-capacity induction motors, and sudden changes in the system connected to large loads [3]. Viewed from the system, the DVR is divided into two systems, namely one-phase DVR and three-phase DVR. Then three-phase DVR is connected to a 3 phase 3 wire (3P3W) or a 3 phase 4 wire (3P4W) system. Next, this paper will further focus on the design and implementation of single-phase DVRs to mitigate voltage sag at the source side and connect to a number of the linear/non-linear load. The simulation of low voltage single phase DVR based on the multilevel inverter to protect sensitive

loads has been implemented in [4]. The proposed model is able to compensate for the voltage sag and increase the PQ on the load side. A DVR topology using a cascaded multilevel direct pulse with modulation (PWM) ac-ac converter has been proposed in [5]. In this scheme, the unit cell of the multilevel converter consists of a single-phase ac-ac converter PWM using a switching cell (SC) structure that is paired with an inductor. The implementation of the phase shift PWM technique is capable of significantly reducing the size of the output filter inductor. One and three-phase DVR control schemes using PSCAD/EMTDC have been observed in [6]. The proposed system is able to compensate for a number of voltage sag variations and keep the load voltage constant. DVR control scheme with an ac-ac converter, based on voltage drop characterization has been investigated in [7] to reduce voltage drop with phase jumps. The superiority of the proposed control scheme is then validated on an ac-ac interphase converter topology. The vector-based one-phase DVR control using an improved synchronous reference frame (SRF) has been proposed in [8]. The vector analysis used in this control method during the voltage period was able to provide the magnitude and phase of the injection voltage.

The control methods to reduce sag voltages using a fuzzy logic controller (FLC) connected with sensitive loads [9] and distributed generation (DG) [10] have been proposed. The FLC control was used to generate pulses with the Sinusoidal Pulse Width Modulation (SPWM) technique at the output of an active filter circuit. Comparing to proportional-integral (PI) control, FLC control was able to provide better performance during voltage sag because it has more advantages in terms of resistance to parameter variations and system execution. A DVR with DG-connected FLC control also able to enhance voltage profiles, power quality, and reliability. Single-phase and three-phase DVRs use a single-phase ac to ac matrix converter to replace voltage source inverter (VSI), has been investigated by Matlab in [11, 12], and in PSCAD [13], at a number of variations in source voltage (sag, flicker, and unbalance). The single-phase DVR has been simulated in [14] and a special voltage detection method for single-phase DVRs has been introduced in [15]. The simulation results show that the DVR was able to maintain the nominal load voltage, despite interference and other abnormal conditions from the source side. The special detection method using double closed-loops of the proportional-resonant controller was also able to provide superior performance in voltage detection and compensation.

The DVR control scheme for reference voltage generation based on a single-phase Second Order Generalized Integrator-Phase Lock Loop (SOGI-PLL) using a series of active compensator has been observed in [16]. The proposed scheme is capable of dynamically responding, detecting, and rapidly compensating for sag/swell voltages without and with phase jumps. A DVR that uses a multilevel H-bridge inverter with a capacitor as an energy source has been introduced in [17]. This configuration allows the DVR to connect directly to a medium-voltage network, eliminating the need for a series injection transformer and batteries. The DVR model was the same but uses a single H-Bridge inverter and a battery on sag/swell voltage disturbances connected to the non-linear load which has also been observed in [18]. Interline DVR (IDVR) on two same [19] and different voltage distribution lines with voltage source inverter (VSI) and current source inverter (CSI) [20] to restore voltage sag and harmonics has been introduced. When voltage sag and voltage distortion occur on one channel, the DVR on the same channel is able to perform voltage compensation and harmonics elimination, while the other DVR can recharge the energy to the DC-link to maintain the DC-link voltage constant.

In order to efficiently the number of equipment in the DVR circuit configuration, the implementation of a direct ac/ac converter on the DVR has been introduced in [21, 22]. The proposed configuration uses the minimum switches, did not require a dc-link energy storage element, and has a longer compensation time during sag/swell voltage disturbances. The compensation voltage for each phase is taken from each of the three-phase sources so that each converter was able to operate independently and is also able to compensate for single-phase blackouts and unbalance sag/swell voltages. The use of a single-phase transformer-less DVR (TDVR) to mitigate the sag/swell voltage has been observed in [23]. The proposed configuration was capable of reducing system size and losses compared to DVR which using a series transformer. The single-phase interactive channel DVR using the sag voltage detection algorithm has been developed in [24]. The detection algorithm has a hybrid structure consisting of a momentary detection section and a RMS variation detection section. The DVR development could compensate for input voltage sag or interrupt in 2.0-ms delay and can be used effectively for sensitive loads.

The single-phase DVR with synchronous reference frame control under distorted source conditions has been applied in [25]. The proposed control using a moving average filter (MAF) is

capable of extracting positive sequence fundamental components as well as being able to mitigate voltages sag and distorted source voltages. The single-phase DVR using elliptical restoration-based voltage compensation to correct the power factor on the source side has been proposed in [26]. The active and reactive voltage components and centrifugal angles are used to formulate an elliptical compensation path. So that the voltage will be in-phase with the load current using precise control of the DVR injection voltage. The optimization of the voltage injection technique in DVR to protect sensitive loads has been observed in [27]. The recursive least square (RLS) method is used to estimate the magnitude and phase of the voltage in order to minimize the amplitude of the injection voltage. Meanwhile, repetitive control was proposed to track the compensation voltage. Both controls are suitable for sinusoidal reference and are reliable for mitigating harmonics, sags, and swell distortions.

Energy storage in single or three-phase DVR circuits related to the capacity and type of energy storage has become the attention of many researchers. The determination of the two parameters relates to the ability and duration of the energy storage to supply real power to the inverter during a fault. Unbalanced voltage compensation in 3P3W system using DVR using a super capacitor has been investigated in [28]. The proposed DVR configuration uses a control based on the d-q-0 and Proportional Integral (PI) transformation technique and is further coded using a digital signal processor (DSP). DSP control and super capacitor implementation can mitigate unbalanced voltage disturbances. A compressed air energy storage powered dynamic voltage restorer (CAESPDVR) with ANFIS control has been proposed in [29] to compensate for unbalanced sag/swell voltages and harmonics. The single-phase DVR configuration using a hybrid energy storage system (HES) has been developed in [30].

The HES series consists of superconducting magnetic energy storage (SMES) in collaboration with battery energy storage (BES) on a DC type DVR. The proposed HES concept integrated with fast response large power SMES unit and low-cost high capacity BES can further be implemented in large scale DVR development. The DVR uses VSI method with SPWM to compensate for sag voltage has been implemented in [31]. The voltage sag was able to be simulated and monitored by LabVIEW with the NI myRIO-1900 interface using LabVIEW in real-time. The mitigation of sag/swell voltage and harmonics in low voltage distribution networks using DVR-BES-PV using the UVTG control method has been observed in [32]. The proposed model was able to

compensate for sag voltage between 10% to 90% and swell voltage between 110% to 180% with a voltage THD within the IEEE 519 limit.

In this paper, BES is proposed as energy storage and implemented in single-phase DVR using load voltage control with the UVTG method and connected to linear/non-linear loads. The UVTG method on the DVR system is implemented using the Arduino-Uno microcontroller hardware. The LabVIEW based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period i.e. source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power factor measurements are also carried out to obtain the total harmonic value or Total Harmonic Distortion (THD) of the source current and load current.

This paper is arranged as follows. Section 2 presents the proposed method, UVTG method, percentage of voltage sag, true power factor and harmonic, single-phase DVR-BES using LabVIEW, as well as hardware and software implementation, Section 3 presents results and discussion of the source

Table 1. Abbreviation

| Symbol         | Description  |
|----------------|--|
| PQ             | Power Quality  |
| DVR            | Dynamic Voltage Restorer                                       |
| BES            | Battery Energy Storage   |
| PV             | Photovoltaic   |
| UVTG           | Unit Vector Template Generation                                |
| THD            | Total Harmonic Distortion                                      |
| $P_{f_{true}}$ | True Power Factor  |
| FL             | Fluorescent  |
| LED            | Light Emitting Diode   |
| DG             | Distributed Generation   |
| 3P3W           | Three Phase Three Wire   |
| 3P4W           | Three Phase Four Wire  |
| SPWM           | Sinusoidal Pulse Width Modulation                              |
| VSI            | Voltage Source Inverter  |
| CSI            | Current Source Inverter  |
| SOGI-PLL       | Second Order Generalized Integrator-Phase Lock Loop            |
| CAESPDVR       | Compressed Air Energy Storage Powered Dynamic Voltage Restorer |
| ANFIS          | Artificial Intelligent Fuzzy Inference System                  |
| IDVR           | Interline Dynamic Voltage Restorer                             |
| CB             | Circuit Breaker  |
| RMS            | Root Mean Square   |
| GUI            | Graphic User Interface   |
| PC             | Personal Computer  |
| USB            | Universal Serial Bus   |
| PU             | Per Unit   |

voltage, injection voltage, load voltage, DC-link voltage, source current, load current, percentage of

voltage sag, true power-factor, and current THD which analyzed from data measured by Arduino-Uno and monitored by LabVIEW. In this section, the system connected to the linear/non-linear load with and without voltage sag is selected to present the best performance single-phase DVR-BES system connected to three different types of load during voltage sag. Finally, this paper is concluded in Section 4. All manuscripts must be in English. These guidelines include complete descriptions of the fonts, spacing, and related information for producing your proceedings manuscripts. Table 1 shows the abbreviations used in this paper.

## 2. Research method

### 2.1 Proposed method

Fig. 1 shows a single-phase DVR supplied by BES using load voltage control with the UVTG method. The DVR is a tool that functions to compensate for the load voltage in the event of a voltage sag disturbance on the source bus at a level of 0.1 to 0.9 per unit. The UVTG method on the DVR system is implemented using the Arduino-Uno hardware. LabVIEW-based interface simulation is used to monitor electrical quantities in real-time during the voltage sag period.

The observed parameters are source voltage ( $V_S$ ), injection voltage ( $V_{inj}$ ), load voltage ( $V_L$ ), DC-link voltage ( $V_{DC-Link}$ ), source current ( $I_S$ ), and load current ( $I_L$ ). The true power-factor ( $Pf_{true}$ ) measurements are also carried out to obtain the THD value of the source current and load current. There are two cases in this study, the source without voltage sag, and with an 80% voltage sag. In each case, the single-phase DVR

|                      |   |
|----------------------|---|
| $V_S$                | Source Voltage                            |
| $V_{inj}$            | Injection Voltage                         |
| $V_L$                | Load Voltage                              |
| $V_{DC-Link}$        | DC-Link Voltage                           |
| $I_S$                | Source Current                            |
| $I_L$                | Load Current                              |
| $I_L^*$              | Reference Load Voltage                    |
| $V_m$                | Peak Fundamental Input Voltage Magnitude  |
| $K$                  | Gain                                      |
| $S_1, S_2, S_3, S_4$ | Gating Signal 1, 2, 3, and 4              |
| $Sag_{dev}$          | Voltage Sag Deviation                     |
| $V_{pre-sag}$        | Pre-Sag Voltage                           |
| $V_{sag}$            | Sag Voltage                               |
| $Pf_{true}$          | True Power Factor                         |
| $P_{avg}$            | Average Power                             |
| $S$                  | Apparent Power                            |
| $V_{rms}$            | RMS Voltage                               |
| $I_{rms}$            | RMS Current                               |
| $V_{1rms}$           | RMS Fundamental Voltage                   |
| $I_{1rms}$           | RMS Fundamental Current                   |
| $THD_V$              | Voltage THD                               |
| $THD_I$              | Current THD                               |
| $P_{1avg}$           | Fundamental Average Power                 |
| $Pf_{displacement}$  | Displacement Power Factor                 |
| $Pf_{distorted}$     | Distorted Power Factor                    |
| $R_S$                | Line Resistance (0.1 ohm)                 |
| $L_S$                | Line Inductance (0.15 mH)                 |
| $R_C$                | Load Resistance (0.4 ohm)                 |
| $L_C$                | Load Inductance (15 mH)                   |
| $L_{Se}$             | Series Inductance (0.015 mH)              |
| $L_1$                | BES Inductance (6 mH)                     |
| $C_1$                | BES Capacitance (1000 $\mu$ F)            |
| $C_{DC}$             | DC-Link Capacitance (200 $\mu$ F)         |
| $R_L$                | Linear/Non-Linear Resistance (0.6 ohm)    |
| $L_L$                | Non-Linear Load Inductance (0.15 mH)      |
| $C_L$                | Non-Linear Load Capacitance (3.3 $\mu$ F) |
| $C_R$                | Ripple Capacitance (0.2 $\mu$ F)          |

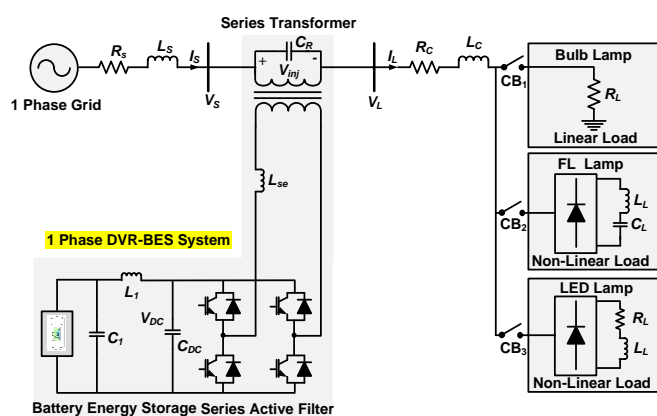


Figure. 1 Proposed single phase DVR-BES connected to linear/non-linear load

Table 2. Notation list and parameters

| Notation | Description |
|----------|-------------|
|----------|-------------|

system is supplied by BES connected to a 5-watt bulb lamp (linear load), 5 watt FL lamp (non-linear load), and 5 watts LED lamp (non-linear load), so the total selected case is six. The CB1, CB2, and CB3 are used to connect and disconnect links to three linear/non-linear loads. The DVR-BES system configuration is then run based on a predetermined case using Arduino-Uno microcontroller interfaced communication and the results are simulated and monitored in real-time by a LabVIEW. Table 2 shows the notation list and parameters of Fig. 1.

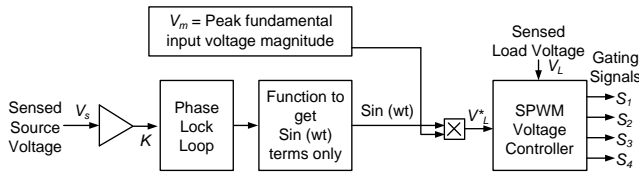


Figure. 2 UVTG control on single phase series active filter

### 2.2 Unit voltage template generation method

The series active filter protect sensitive loads against several voltage disturbances from the source bus. In [31], the control method of source and load voltage in a three-phase series active filter has been discussed. Using the same procedure, the authors propose the same method for single-phase series active filter control as shown in Fig. 2. This method extracts UVTG from the distorted input supply. Then, the template is expected to be an ideal sinusoidal signal with a unity amplitude. The source of the distorted voltage is measured and divided by the peak amplitude fundamental input voltage ( $V_m$ ).

A single-phase locked loop (PLL) is used in order to generate sinusoidal unit vector templates with a phase lagging by the use of the sine equation. The reference signal of the load voltage is calculated by multiplying the unit vector templates with the peak amplitude of the fundamental input voltage ( $V_m$ ). The reference load voltage ( $V_L^*$ ) is then compared to the sensed load voltage ( $V_L$ ) by a SPWM controller used to generate the desired four gating signal on a single-phase series active filter.

### 2.3 Percentage of voltage sag deviation

The recommended standard of practice on monitoring voltage sag/swell as part of electric power quality parameters is IEEE 1159 [2]. This standard presents the definition and table of voltage sag base on categories (instantaneous, momentary, temporary) typical duration, and typical magnitude. The percentage of load voltage sag deviation is formulated in Eq. (1) [31].

$$Sag_{dev}(\%) = \frac{|V_{pre\_sag} - V_{sag}|}{V_{pre\_sag}} \quad (1)$$

### 2.4 True power factor and harmonics

The true power factor at the load is defined as the ratio of average power to apparent power. The true power factor for both sinusoidal and non-sinusoidal situations is presented in Eq. (2) [33].

$$pf_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{rms} I_{rms}} \quad (2)$$

$$V_{rms} = V_{1rms} \sqrt{1 + (THD_V/100)^2} \quad (3)$$

$$I_{rms} = I_{1rms} \sqrt{1 + (THD_I/100)^2} \quad (4)$$

By substituting Eq. (3) and Eq. (4) into Eq. (2), the true power factor ( $Pf_{true}$ ) results in Eq. (5) for both sinusoidal and non-sinusoidal cases [33].

$$pf_{true} = \frac{P_{avg}}{V_{1rms} I_{1rms} \sqrt{1 + (THD_V/100)^2} \sqrt{1 + (THD_I/100)^2}} \quad (5)$$

A useful simplification can be made by expressing Eq. (5) as a product of two components defined in Eq. (6).

$$pf_{true} = \frac{P_{avg}}{V_{1rms} I_{1rms}} \times \dots \dots \frac{1}{\sqrt{1 + (THD_V/100)^2} \sqrt{1 + (THD_I/100)^2}} \quad (6)$$

By making the following two assumptions: (1) In most cases, the contributions of harmonics above the fundamental to average power are very small, so that is  $P_{avg} \approx P_{1avg}$  and (2) Since  $THD_V$  is less than 10%, then from (12) we see that  $V_{rms} \approx V_{1rms}$ . Then, merging both assumptions into Eq. (6) results in the following approximate function for the true power factor ( $Pf_{true}$ ) presented in Eq. (7) [33].

$$pf_{true} = \frac{P_{1avg}}{V_{1rms} I_{1rms}} \times \frac{1}{\sqrt{1 + (THD_I/100)^2}} = Pf_{displacement} \times Pf_{distorted} \quad (7)$$

Because displacement power factor ( $Pf_{disp}$ ) could never be greater than unity, Eq. (7) shows that the true power factor ( $Pf_{true}$ ) in non-sinusoidal cases has the upper limit so finally its function is defined in Eq. (8) [33].

$$pf_{true} \leq Pf_{distorted} = \frac{1}{\sqrt{1 + (THD_I/100)^2}} \quad (8)$$

### 2.5 Single phase DVR-BES using labVIEW

The implementation of the single-phase DVR-BES system consists of several stages. That stage i.e. create a single-phase series active filter, create a gate driver to trigger the MOSFET in the series active filter, create a SPWM program to drive the gate driver as an inverter trigger and create a monitoring program in LabVIEW. Fig. 3 presents a schematic diagram of a single phase DVR-BES system.

Fig. 3 shows that the BES and series active filters play an important role in compensating for the

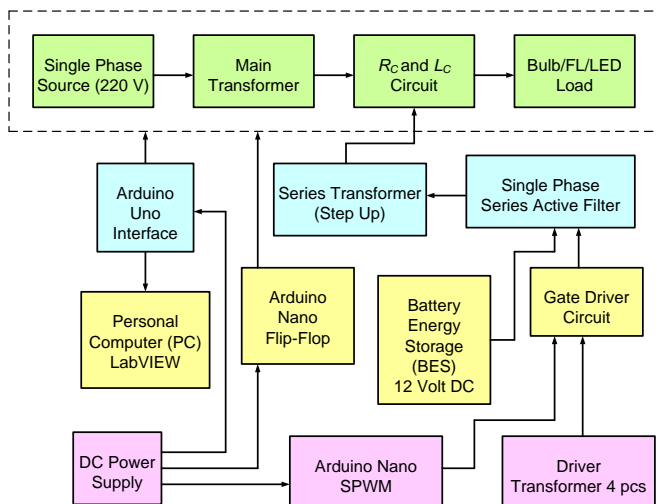


Figure. 3 A schematic diagram of single phase DVR-BES

voltage sag on a single-phase DVR. The step-up transformer that is installed in a series against the load functions to inject the voltage from the series active filter to the load. The main energy source for series active filters uses BES DC voltage 12 V with a capacity of 7.2 Ah. The process of changing the DC to AC voltage begins with the Arduino Nano SPWM microcontroller providing Sinusoidal SPWM pulses to the Gate Driver circuit which has the main component of the TLP 250 Optocoupler IC, then the Gate Driver circuit triggers the IRFP250 MOSFET gate on a series active filter circuit cross-like as an electric current cycle in the circuit bridge diode rectifier. So that it will produce an AC output from a series active filter circuit. The output voltage of the series active filter is an AC voltage of 7 V depending on the battery voltage conditions, which will then be increased to an AC voltage of 220 V using a step-up transformer. The step-up series transformer has a power of 600 VA with a primary AC input voltage of 7.2 V and a secondary AC output voltage of 220 V. The goal is that the series active filter is able to inject enough power to compensate for the sag voltage at a level of 10% to 90%.

The Arduino Nano flip-flop functions as a timer to run system simulations using a single-phase DVR-BES without and with sag voltage. The Arduino nano has been programmed with a flip-flop program with the 1-second case instructing the relay to turn "on" as a representation of the system experiencing sag voltage and 1 second ordering the relay to turn "off" as a representation of the system without experiencing sag voltage. This timer is expected to function when there is a sag voltage and automatically orders a single-phase active filter to inject a voltage compensation into the load so that the load voltage will remain stable.

The Arduino Uno interface functions as a medium for receiving data from voltage sensors and current sensors that are measuring the amount of electricity in the DVR circuit and sending the data to a personal computer (PC) with LabVIEW software. Curves and data displayed in LabVIEW i.e. source voltage, load voltage, injection voltage, DC-link voltage, source current, and load current respectively. The display form implemented in LabVIEW is in the form of graphs and number indicators. With a graphic display, the reader will find it easier to observe the wave condition both voltage and current during the system condition without and with voltage sag. All data displayed in LabVIEW is real-time and continuous data as long as the single-phase DVR-BES system is operated to the system. In addition to using the LabVIEW, data collection is also carried out by the cos-phi meter to determine the value of the true power factor of source and load as a basis for determining the harmonic of source and load currents. The single-phase DVR-BES system connected to three linear/non-linear loads i.e. bulb lamp 5 W (linear), FL lamp 5 W (non-linear), LED lamp 5 W (non-linear) respectively.

### 2.5 Hardware and software implementation

The LabVIEW interface software diagram consists of the main program in the form of a Graphic User Interface (GUI) which functions to run all indicators and controls on the front panel. Fig. 4 shows the model of the single-phase DVR-BES hardware circuit. The nominal parameters of Fig. 4 are presented in Table 3.

Table 3. Nominal of device parameters

| Devices                               | Design Values       |
|---------------------------------------|---------------------|
| Single phase source voltage           | 220 V               |
| Frequency                             | 50 Hz               |
| Series Transformer ( <i>step-up</i> ) | 600 VA<br>7,2/220 V |
| Main Transformer (CT)                 | 3 A                 |
| Current Sensor ACS 712                | 5A                  |
| Relay                                 | 1 device            |
| Arduino Uno (Interface)               | 1 device            |
| Arduino Nano (Flip-Flop)              | 1 device            |
| Arduino Nano (SPWM)                   | 1 device            |
| Load Resistance ( $R_c$ )             | 0.4 ohm             |
| Load Inductance ( $L_c$ )             | 15 mH               |
| Cos-phi-Meter                         | 1 device            |
| Battery Energy Storage (BES)          | 12 V/7.2 Ah         |
| DC-link Capacitance ( $C_{DC}$ )      | 1000 $\mu F$        |
| Bulb Lamp Load                        | 5 W                 |
| FL Lamp Load                          | 5 W                 |
| LED Lamp Load                         | 5 W                 |

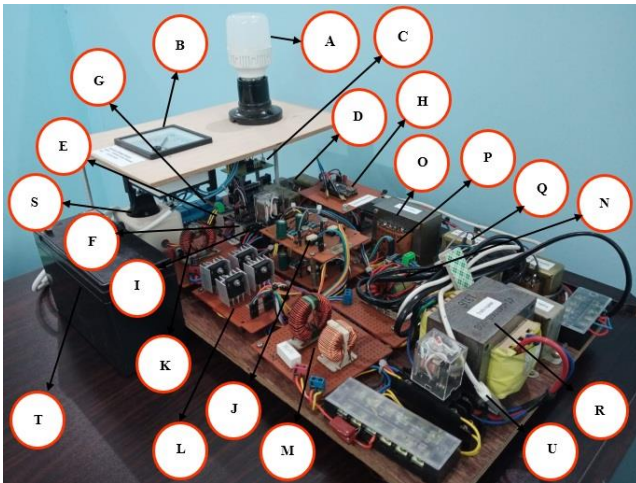


Figure. 4 Single-phase DVR-BES hardware

Where A: Load; B: Cos-phi-meter; C: Arduino Uno; D: Voltage Sensor Transformer; E: Current Sensor; F: Arduino Nano SPWM; G: Relay 1 (4 Channel); H: Arduino Nano Flip-Flop; I: Two Relays (220V-AC); J: Gate Driver Optocoupler; K: DC-link Capacitance and BES filter ( $C_{DC}, L_1, C_1$ ); L: Series Active Filter; M: Load Impedance ( $R_C, L_C$ ); N: Series Inductance ( $L_{Se}$ ); O: Main Transformer; P: Source Current Sensor; Q: Gate Driver Transformer; R: Series Transformer; S: Source Voltage; T: BES and U: Universal Serial Bus (USB) for data communication between hardware PC.

Fig. 5 shows the overall GUI program design and the component parts of the single-phase DVR-BES. In order for the LabVIEW software interface on the PC to communicate with the Arduino Uno, a program is needed to communicate the two devices. The communication program used by Lifa Base. Lifa Base is the driver for Arduino Uno in connecting data communication with PC. Lifa Base is the default program from Arduino when users install LabVIEW.

### 3. Results and discussion

Fig. 1 shows a series of DVR supplied by BES connected to a load of Bulb, FL, and LED respectively. The series transformer connected to the load functions to inject the voltage from the series active filter during voltage sag. The Arduino Nano Flip-Flop is used as a timer to run simulated data collection. The cycle timer applied to the DVR is 1 second on and 1 second off. The data collection period is carried out with a LabVIEW simulation for 3 seconds, with 80% depth of source voltage sag duration between 1 to 2 seconds. Data collection is carried out at 1.5 seconds from the curve of the source voltage ( $V_S$ ), injection voltage ( $V_{inj}$ ), load voltage ( $V_L$ ), DC-link voltage ( $V_{DC-Link}$ ), source current ( $I_S$ ), and load current ( $I_L$ ), curves. The true

power-factor ( $Pf_{true}$ ) data in the source bus and load bus is measured from the cos-phi meter.

Using the same LabVIEW simulation procedure and period, data collection is also carried out without the voltage sag. The percentage of load voltage sag deviation is calculated using Eq. (1) with a pre-sag voltage of 203 V. Base on true power-factor, then harmonics current is measured using Eq. (8). Table 4 presents the performance of voltage, current, and percentage of sag deviation of load voltage ( $V_L$ ) of the single-phase DVR supplied by BES without and with voltage sag disturbance. Table 5 presents the performance of true power factor ( $Pf_{true}$ ) and harmonics value of the single-phase DVR supplied by BES without and with voltage sag disturbance. Fig. 6, Fig. 7, and Fig. 8 show the performance of voltage and current of the single-phase DVR supplied by BES connecting to bulb lamp, FL lamp, and LED lamp load respectively.

Fig. 6 shows the simulation curve of the sag voltage on a single-phase DVR system supplied by a BES connected to a bulb lamp load. The voltage sag disturbance lasts from  $t = 1$  to  $t = 2$  seconds with a total simulation time of 3 seconds. The measurements on all simulation parameters curves are carried out at  $t = 1.5$  seconds. At  $t = 1$  to  $t = 2$  seconds, the source voltage ( $V_S$ ) drops from 230 V to 44.7 V, and the series transformer injects a voltage ( $V_{inj}$ ) of 168 V so that the load voltage ( $V_L$ ) remains constant at 216 V. In this disturbance condition the value of the source current ( $I_S$ ) is 0.228 A and the load current ( $I_L$ ) drops to 0.45 A. To keep the load voltage ( $V_L$ ) maintain constant, BES releases its energy so that the DC link voltage ( $V_{DC-Link}$ ) drops from 13.03 V to 8.20 V.

Fig. 7 shows the simulation curve of sag voltage on a single-phase DVR system supplied by the connected BES to the FL lamp load. At  $t = 1$  to  $t = 2$  seconds, the source voltage ( $V_S$ ) drops from 230 V to 50.3 V and the series transformer injects a voltage ( $V_{inj}$ ) of 200 V so that the load voltage ( $V_L$ ) remains constant at 256 V. During the duration of the sag voltage, the capacitance effect of the capacitor component able to store charge on the FL lamp load, causing the load voltage value to exceed the source voltage. In the disturbance conditions, the value of the source current ( $I_S$ ) is 0.166 A and the load current ( $I_L$ ) drops to 0.208 A. To keep the load voltage ( $V_L$ ) maintain constant, BES releases its energy so that the DC link voltage ( $V_{DC-Link}$ ) drops from 13.03 V to 7.33 V.

Fig. 8 shows a simulation curve voltage sag on a single-phase DVR system supplied by BES connects to the LED lamp load. At  $t = 1$  to  $t = 2$  seconds, the

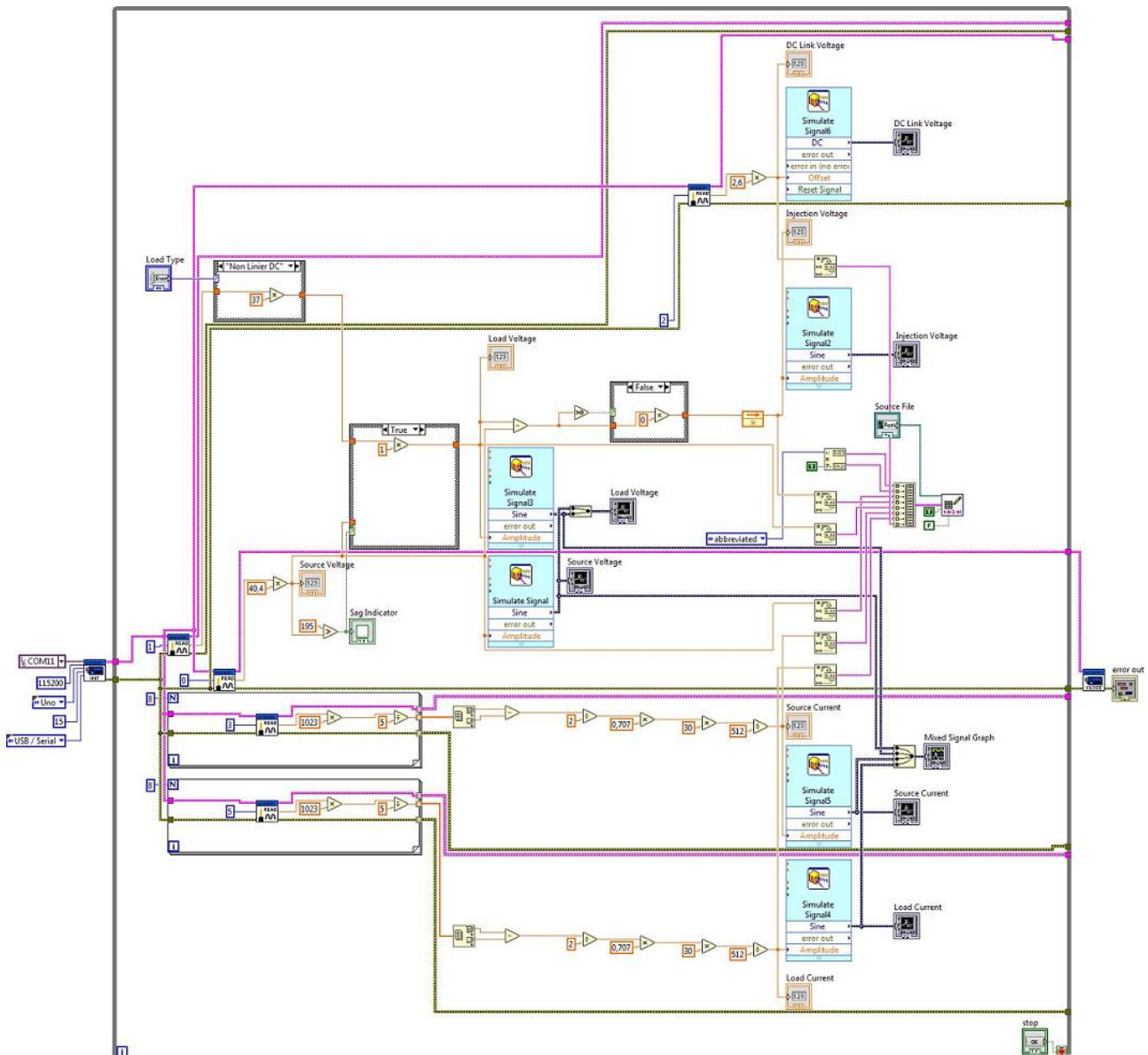


Figure. 5 Software design using LabVIEW interface for simulate signal i.e. (A) arduino-uno data communication, (B) source voltage ( $V_S$ ), (C) injected voltage ( $V_{Inj}$ ), (D) load voltage ( $V_L$ ), (E) source current ( $I_S$ ), (F) load current ( $I_L$ ), (G) DC-link voltage ( $V_{DC-Link}$ ), and (H) mixed signal graph

Table 4. Performance of voltage, current, and sag deviation of load voltage of the single-phase DVR supplied by BES

| No.                 | Load Type | $V_S$ (V) | $V_{Inj}$ (V) | $V_L$ (V) | $I_S$ (A) | $I_L$ (A) | $V_{DC-Link}$ (V) | Sag Dev of $V_L$ (%) |
|---------------------|-----------|-----------|---------------|-----------|-----------|-----------|-------------------|----------------------|
| Without Voltage Sag |           |           |               |           |           |           |                   |                      |
| 1.                  | Bulb Lamp | 203       | 0             | 203       | 0.208     | 0.166     | 13.03             | 0                    |
| 2.                  | FL Lamp   | 203       | 0             | 203       | 0.208     | 0.083     | 13.03             | 0                    |
| 3.                  | LED Lamp  | 203       | 0             | 203       | 0.270     | 0.166     | 13.03             | 0                    |
| With Sag Voltage    |           |           |               |           |           |           |                   |                      |
| 4.                  | Bulb Lamp | 44.7      | 168           | 216       | 0.228     | 0.145     | 8.20              | 6.40                 |
| 5.                  | FL Lamp   | 50.3      | 200           | 256       | 0.166     | 0.208     | 7.33              | 26.13                |
| 6.                  | LED Lamp  | 49.1      | 133           | 185       | 0.249     | 0.789     | 8.06              | 8.87                 |

source voltage ( $V_S$ ) drops from 230 V to 49.1 V and the series transformer injects a voltage ( $V_{Inj}$ ) of 133 V so that the load voltage ( $V_L$ ) remains constant at 185 V. During the disturbance conditions, the value

of the source current ( $I_S$ ) is 0.249 A, and the load current ( $I_L$ ) increases to 0.789 A. To keep the load voltage ( $V_L$ ) maintain constant, BES then releases its energy so that the DC link voltage ( $V_{DC-Link}$ ) drops



Table 5. Performance of power factor and harmonics of the single-phase DVR supplied by BES

| No.                 | Load Type | Source $Pf_{true}$ (pu) | Load $Pf_{true}$ (pu) | Source $THD_I$ (%) | Load $THD_I$ (%) |
|---------------------|-----------|-------------------------|-----------------------|--------------------|------------------|
| Without Voltage Sag |           |                         |                       |                    |                  |
| 1.                  | Bulb Lamp | 0.850                   | 0.999                 | 17.647             | 0.1001           |
| 2.                  | FL Lamp   | 0.900                   | 0.999                 | 11.111             | 0.1001           |
| 3.                  | LED Lamp  | 0.990                   | 0.999                 | 1.010              | 0.1001           |
| With Sag Voltage    |           |                         |                       |                    |                  |
| 4.                  | Bulb Lamp | 0.985                   | 0.998                 | 1.523              | 0.2040           |
| 5.                  | FL Lamp   | 0.985                   | 0.998                 | 1.523              | 0.6040           |
| 6.                  | LED Lamp  | 0.990                   | 0.975                 | 1.010              | 2.5640           |

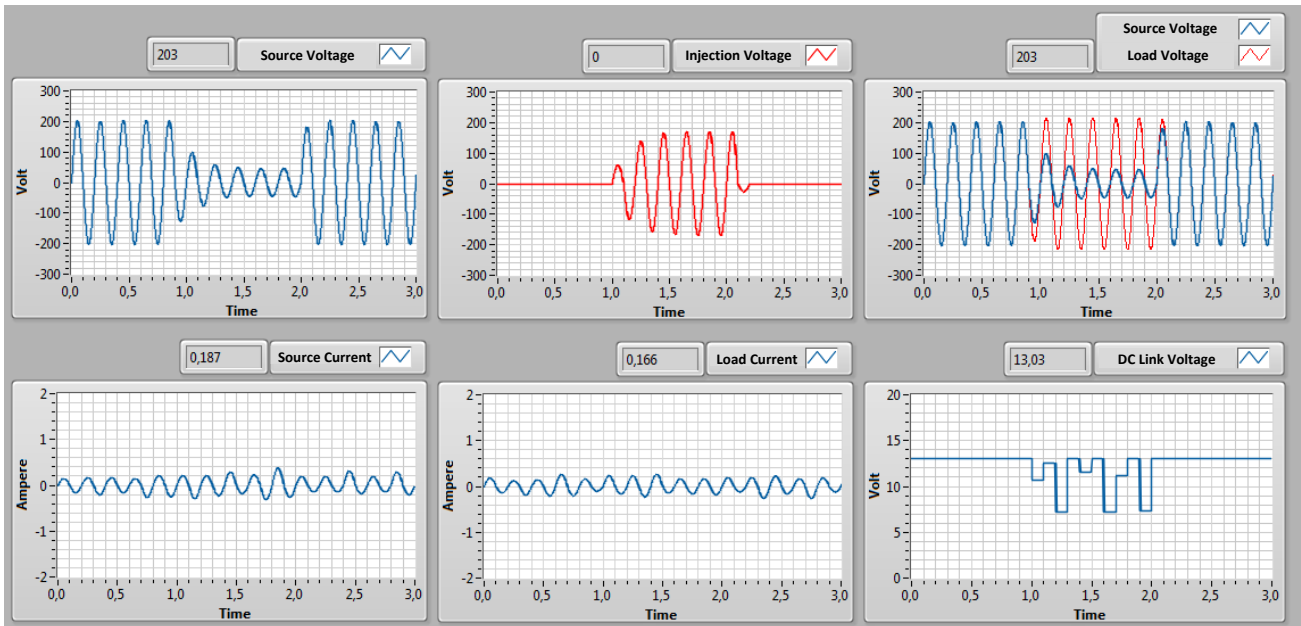


Figure. 6 Performance of  $V_S$ ,  $V_{inj}$ ,  $V_L$ ,  $I_S$ ,  $I_L$ , and  $V_{DC-Link}$  from the single-phase DVR- BES connected to bulb lamp load using LabVIEW

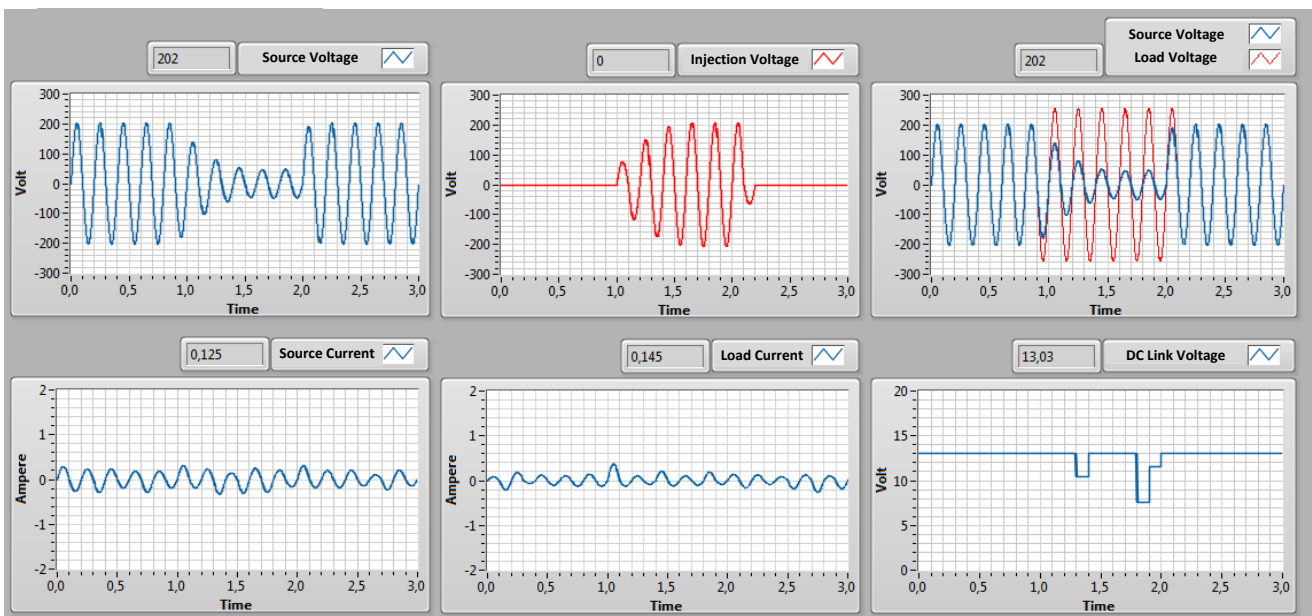


Figure. 7 Performance of  $V_S$ ,  $V_{inj}$ ,  $V_L$ ,  $I_S$ ,  $I_L$ , and  $V_{DC-Link}$  from the single-phase DVR- BES connected to FL lamp load using LabVIEW

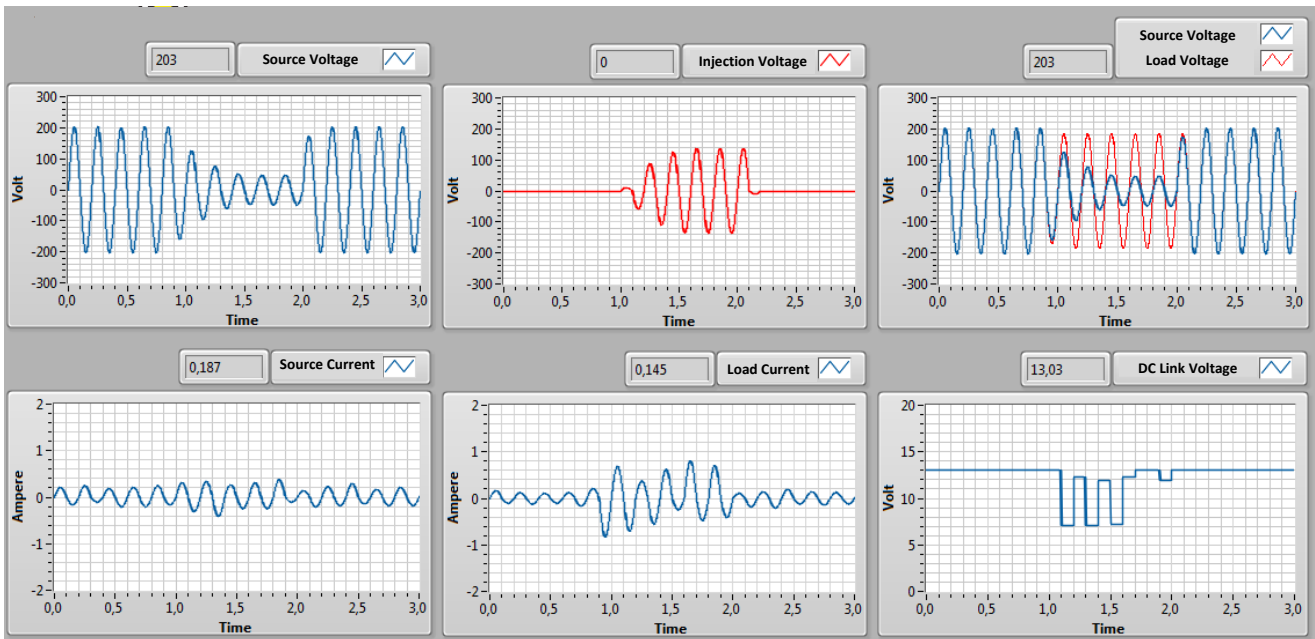


Figure. 8 Performance of  $V_S$ ,  $V_{Inj}$ ,  $V_L$ ,  $I_S$ ,  $I_L$ , and  $V_{DC-Link}$  from the single-phase DVR- BES connected to LED lamp load using LabVIEW

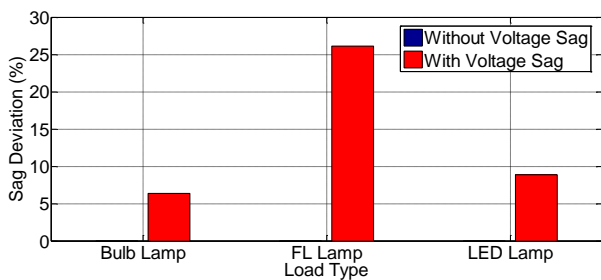


Figure. 9 Performance of sag deviation of  $V_L$  for single phase DVR-BES system on three load type

from 13.03 V to 8.06 V.

Fig. 9 shows that for the system without sag voltage, the series active filter circuit and series transformer on a single-phase DVR-BES system is not able to inject voltage into the load, so produces a percentage of sag deviation of load voltage ( $V_L$ ) of 0%. Otherwise if the system with sag voltage, the single-phase DVR-BES system is able to maintain the load voltage ( $V_L$ ) i.e. bulb lamp, FL lamp, and LED lamp of 216 V, 256 V, and 185 V, respectively.

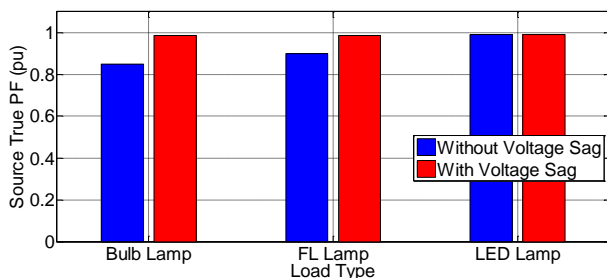


Figure. 10 Performance of source true power-factor for single phase DVR-BES system on three load type

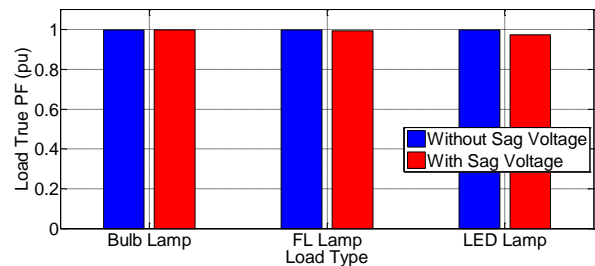


Figure. 11 Performance of load true power-factor for single phase DVR-BES system on three load type

The percentage of load voltage deviation for the system with sag deviation of  $V_L$  for the three loads type are 6.4%, 26.13%, and 8.87%, respectively.

Fig. 10 shows the measurement of source true power-factor without voltage sag of the bulb lamp has the worst true power-factor ( $Pf_{true}$ ) of 0.850 per-unit (pu) leading compared to an FL lamp of 0.900 pu leading and an LED lamp of 0.909 pu leading. Otherwise, for the system with voltage sag, the single-phase DVR-BES system produces source true power factor ( $Pf_{true}$ ) for a bulb lamp, FL lamp, and LED lamp of 0.985 pu leading, 0.985 pu leading, and 0.990 pu leading respectively.

Fig. 11 shows the measurement of load true power-factor without voltage sag for all load categories results in the same true power factor ( $Pf_{true}$ ) of 0.999 pu leading. Otherwise, for the system with voltage sag is able to result in load true power factor ( $Pf_{true}$ ) i.e. bulb lamp, FL lamp, and LED lamp of 0.975 pu leading, 0.998 pu leading, and 0.994 pu leading respectively.

Fig. 12 shows that the system without sag voltage

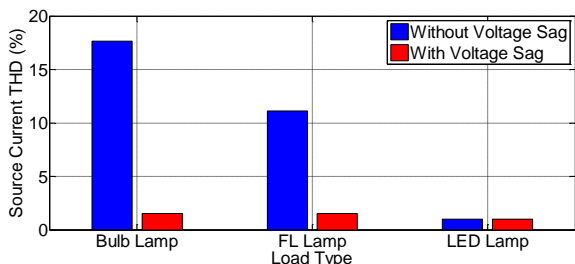


Figure. 12 Performance of source harmonics for single phase DVR-BES system on three load type

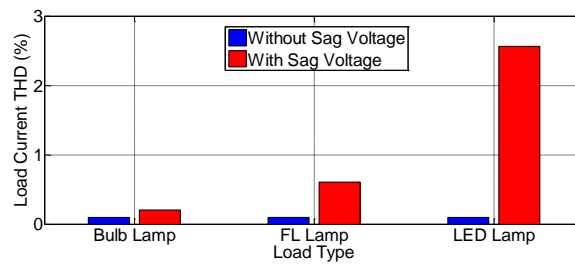


Figure. 13 Performance of load harmonics for single phase DVR-BES system on three load type

Table 6. Comparison of implementation UVTG-DVR-BES-Arduino-Uno-LabVIEW (proposed study) and previous studies

| No. | Authors                         | Methods                                 | Depth Sag of $V_s$ (%)    | Sag Dev of $V_L$ (%)                       | Load $THD_V$ (%)                 | Source $THD_I$ (%)                           | Source $pf_{true}$                           | Real Time  |
|-----|---------------------------------|---|---------------------------|--|----------------------------------|--|--|------------|
| 1   | D.N. Katole, et al [8]          | Improved SRF                            | 42                        | 7.6  | NA                               | NA   | NA   | Not        |
| 2   | M.T. Hagh, et al. [10]          | FLC                                     | 92 without and 95 with DG | 8.9 without DG and 6.4 with DG             | 1.26 without DG and 3.54 with DG | NA   | NA   | Not        |
| 3   | H.K. Yada, et. al [16]          | SOGI-PLL                                | 30                        | 3.0  | NA                               | NA   | NA   | Not        |
| 4   | S. Galeshi, et al. [17]         | Multilevel Cascade H-Bridge Inverter    | 20                        | 0.0  | 4.0                              | NA   | NA   | Not        |
| 5   | R. Nittala, et al [19]          | IDVR with VSI and CSI                   | 27.7 with VSI and CSI     | 0 with VSI and CSI                         | 0.06 with VSI and 0.05 with CSI  | NA   | NA   | Not        |
| 6   | E. Babaei, et. al. [22]         | Direct Converter                        | 65                        | 0  | 7.07 (Average)                   | NA   | NA   | Not        |
| 7   | A. Benhail, et al. [23]         | TDVR-PI                                 | 30                        | 2.18                                       | 24                               | NA   | NA   | Not        |
| 8   | J. Ye, et.al. [26]              | Elliptical Restoration                  | 60                        | NA   | NA                               | NA   | 0.75   | Not        |
| 9   | R. Omar, et.al [28]             | DVR-Super-capacitor                     | 30                        | 0  | NA                               | 2.38   | NA   | Not        |
| 10  | C.K. Sundarabalan, et. al. [29] | CAESPDVR-ANFIS                          | 46.67 (Average)           | 0.4  | 2.35                             | NA   | NA   | Not        |
| 11  | V.K. Awaar, et al. [31]         | VSI-SPWM-NI-myRIO-1900-Labview          | 50                        | 8.79                                       | NA                               | NA   | NA   | Yes        |
| 12  | A.Kiswanton et al. [32]         | UVTG-DVR-BES-PV                         | 80                        | 2.89 (Average)                             | 5.81 (Average)                   | NA   | NA   | Not        |
| 13  | <b>Proposed Study</b>           | <b>UVTG-DVR-BES-Arduino-Uno-Labview</b> | <b>80</b>                 | <b>Bulb=6.4<br/>FL =26.13<br/>LED=8.87</b> | <b>NA</b>                        | <b>Bulb=1.523<br/>FL=1.523<br/>LED=1.010</b> | <b>Bulb=0.985<br/>FL=0.985<br/>LED=0.990</b> | <b>Yes</b> |

Note: NA = note available

is able to produce the source  $THD_I$  for bulb lamp, FL lamp, and LED lamp of 17.64%, 11.111%, and 1.010% respectively. Otherwise, for the same system with sag voltage is able to result source  $THD_I$  for

bulb lamp, FL lamp, and LED lamp of 1.523%, 1.523%, and 1.010% respectively.

Fig. 13 shows that the system without voltage sag is able to produce the same load  $THD_I$  for bulb lamp, FL lamp, and LED lamp of 0.1001%. Otherwise, for

the same system with voltage sag is able to result in load  $THD_I$  for bulb lamp, FL lamp, and LED lamp of 0.204%, 0.604%, and 2.564% respectively. Fig. 10 and Fig. 11 shows in the case of voltage sag and three types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source true power factor ( $Pf_{true}$ ) of 0.990 pu and the lowest source  $THD_I$  of 1.010%. The source  $THD_I$  and load  $THD_I$  value in voltage sag also had met the IEEE 519.

Table 6 shows the validation of the results for the proposed study compared to the 12 previous studies. The parameters observed are depth of sag of  $V_S$ , sag deviation of  $V_L$ , load  $THD_V$ , source  $THD_I$ , and real-time simulation. At [8], D.N. Katole, et.al proposed an improved SRF on the single-phase DVR series. With a depth of sag of  $V_S$  of 42%, this method produces a sag deviation of  $V_L$  of 7.6%. Furthermore, the FLC method for sag stress compensation was proposed by M.T. Hagh, et.al [10]. With a depth of sag of  $V_S$  of 92% without and 95% with DG, the FLC method yields a sag deviation of  $V_L$  of 8.9% without DG and 6.4% with DG, and a load  $THD_V$  of 1.26% without DG and 3.54 with DG. The SOGI-PLL method proposed by Yada et. Al [16], with a depth of sag of  $V_S$  of 30% was able to produce a sag deviation of  $V_L$  of 3.0%. S. Galeshi, et. al [17] already offer Multilevel Cascade H-Bridge Inverter topology. With a depth of sag of  $V_S$  of 20%, this topology produces a sag deviation of  $V_L$  of 0% and a load of  $THD_V$  of 4%. IDVR configuration with VSI and CSI has been proposed by R. Nittala, et.al [19]. With a depth of sag of  $V_S$  of 27.7% (with VSI and CSI), this configuration resulted in a sag deviation of  $V_L$  of 0%, load  $THD_V$  of 0.06% (with VSI) and 0.05% (with CSI). E. Babaei, et. al [22] have proposed a direct converter topology to mitigate voltage sag. With a depth of sag of  $V_S$  of 65%, this topology produces a sag deviation of  $V_L$  of 0% and a load  $THD_V$  of 7.07% (average).

The TDVR-PI configuration has been proposed by A. Benhail, et.al. [23]. With a depth sag of  $V_S$ , of 30%, this configuration results in a sag deviation of  $V_L$  of 2.18% and a load  $THD_V$  of 24%. J. Ye, et.al [26] have proposed an elliptical restoration method for voltage sag compensation and power factor correction. With a depth of sag of  $V_S$ , of 60%, this method is able to produce a source  $Pf_{true}$  of 0.75 pu. The DVR-Super-capacitor configuration has been implemented by R. Omar, et.al [28]. With a depth of sag of  $V_S$ , of 30%, this topology is able to produce a sag deviation of  $V_L$  of 0 % and source  $THD_I$  of 2.38%. The CAESPDVR-ANFIS topology has been investigated by C.K. Sundarabalan, et. al. [29]. With

a depth of sag of  $V_S$ , of 46.67% (average), this topology was able to produce a sag deviation of  $V_L$  of 0.4% and a load of  $THD_V$  of 2.35%. V.K. Awaar, et.al. [31] have implemented a VSI-SPWM-based single-phase DVR model with the NI-myRIO-1900 interface monitored in real-time by LabVIEW. With a depth of sag of  $V_S$ , of 50%, this model was able to produce a sag deviation of  $V_L$  of 8.79%. DVR control supplied by BES-PV using the UVTG method has been observed by A. Kiswantonono [32]. With a depth of sag of  $V_S$ , of 80%, this configuration and method were able to produce a sag deviation of  $V_L$  of 2.89% (average) and a load  $THD_V$  of 5.81% (average). Based on the results of research [31] and [32], then this study has implemented the single-phase DVR model using the UVTG method with the Arduino-Uno interface monitored in real-time by LabVIEW. With a depth of sag of  $V_S$  of 80%, the proposed model is able to produce sag deviation of  $V_L$  of 6.4% (Bulb), 26.13% (FL), and 8.87% (LED). The model is also able to produce  $THD_I$  source of 1.523% (Bulb), 1.523% (FL), and 1.101% (LED) and  $Pf_{true}$  respectively 0.985% (Bulb), 0.985% (FL), and 0.909% (LED). The proposed study is able to give the best performance because it is able to produce source  $THD_I$  lower than [28] and source  $Pf_{true}$  is higher than [26]. Another contribution is that by using the Arduino-Uno interface, the proposed model can be run and monitored in real-time with LabVIEW. It is different from the simulations conducted by 12 previous researchers (except [31]) which were still carried out off-line using Matlab/Simulink environment.

#### 4. Conclusion

The system using a single-phase DVR supplied by BES with load voltage controlled by a UVTG method has been implemented. The model is connected to three types of linear/non-linear load i.e. bulb lamp, FL lamp, and LED lamp. This configuration is proposed to mitigate 80% voltage sag using the Arduino-Uno hardware and monitored by LabVIEW simulation in real-time. The investigated parameter is source voltage, injection voltage, load voltage, source current, load current, and DC-link voltage. The true power-factor measurements are also carried out to obtain the harmonics of the source current and load current. During voltage sag, the single-phase DVR-BES system is able to maintain load voltage for all types of loads. From the system with voltage sag and three different types of loads, the LHE lamp is able to result in the best performance because it is able to produce the highest source current power factor ( $Pf_{true}$ ) and

the lowest source  $THD_I$ . The source  $THD_I$  and load ( $THD_I$ ) with voltage sag also had met the IEEE 519. The proposed study is able to give the best performance because it is able to produce source  $THD_I$  lower than the previous studies. By using the Arduino-Uno interface, this model can be run and monitored in real-time with LabVIEW better from the simulations conducted by previous researchers which were still carried out off-line using Matlab/Simulink.

In a system using a single-phase DVR-BES connected to the FL load, there is a significant increase in load voltage of 256 V compared to the source voltage. The percentage of sag voltage for FL lamps also increased by 26.13% and has far exceeded the value of 5%. The implementation of a single-phase bidirectional inverter circuit as the interface between the BES and series active filters can be proposed as future work to overcome this problem. The measurement of source  $THD_V$  and load  $THD_V$  in the proposed model is also necessary to determine the harmonic mitigation performance of the voltage within the IEEE 519 limit.

### Conflicts of Interest

The authors declare no conflict of interest.

### Author Contributions

Conceptualization, Y.A. Setiawan and A. Amirullah; methodology, Y.A. Setiawan and A. Amirullah; software, Y.A. Setiawan; validation, Y.A. Setiawan; formal analysis, Y.A. Setiawan and A. Amirullah; investigation, Y.A. Setiawan and A. Amirullah; resources, Y.A. Setiawan; data curation, Y.A. Setiawan; writing—original draft preparation, Y.A. Setiawan; writing—review and editing, Y.A. Setiawan; visualization, Y.A. Setiawan; supervision, A. Amirullah; project administration, Y.A. Setiawan; funding acquisition, A. Amirullah. All authors read and approved the final manuscript.

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