

Simulation study of L-V-F-C Operational Amplifier

M. Nizamuddin

Assistant Professor, ECE Deptt., BGSB University, Rajouri, J&K
nizamdelhi25@gmail.com

Abstract—In this research paper, Simulation study of folded cascode Op Amp based on low voltage has been performed. DC voltage gain, average power, unity gain bandwidth and output resistance have been computed using HSPICE Software. Low voltage folded cascode Op Amp results in high performance. Further, the low voltage Cascode Op Amp has better DC Gain, output resistance and less power dissipation. Thus the simulation studies have revealed that the performance of the low voltage folded cascode Op Amp can be improved optimized at different voltage.

Index terms- low voltage, folded cascode Op Amp, simulation, dc gain, power consumption, output resistance, Bandwidth

I. INTRODUCTION

Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the MOSFETs reduces the performance (degraded bandwidth, low voltage swing etc.) to some extent but there is increase in the static power dissipation.. [1-10]. The performance analysis of conventional Op Amps techniques at large channel length is going to out of reach in near future. The appropriate topology is suggested which has a perfect balance between complexity and performance. Scaling of complementary metal-oxide semiconductor (CMOS) technology to the nano ranges has many limitations and leads to increase the leakage currents, power dissipation, and short-channel effects [16-20].

II. PROPOSED FOLDED CASCODE OP AMP DESIGN

The Figure 1 shows the schematic of a folded-cascode op-amp using a class AB output buffer. In the frequency response of the op-amp, the load of the op-amp is a 1 pF capacitor. Folded cascode Operational Amplifier is designed at different voltages. The widths of MOSFETs are chosen to be identical for a reasonable comparison.

We simulated the proposed circuit using HSPICE which can be used in VLSI systems such as microprocessors, DSP architectures and nano-micro systems.

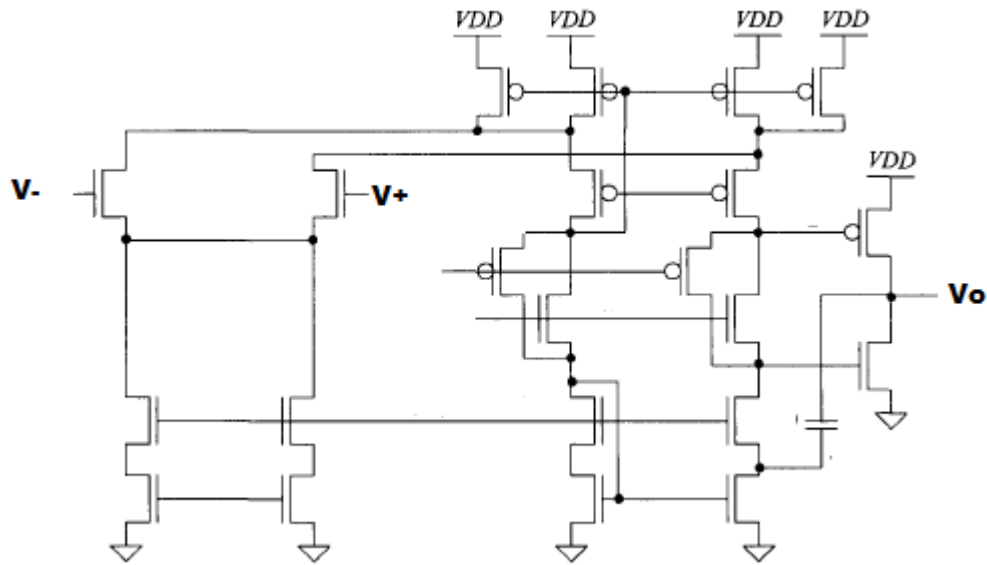


Figure 1. Proposed FOLDED CASCODE OP AMP DESIGN

SIMULATIONS OF PROPOSED FOLDED CASCODE OP AMP DESIGN

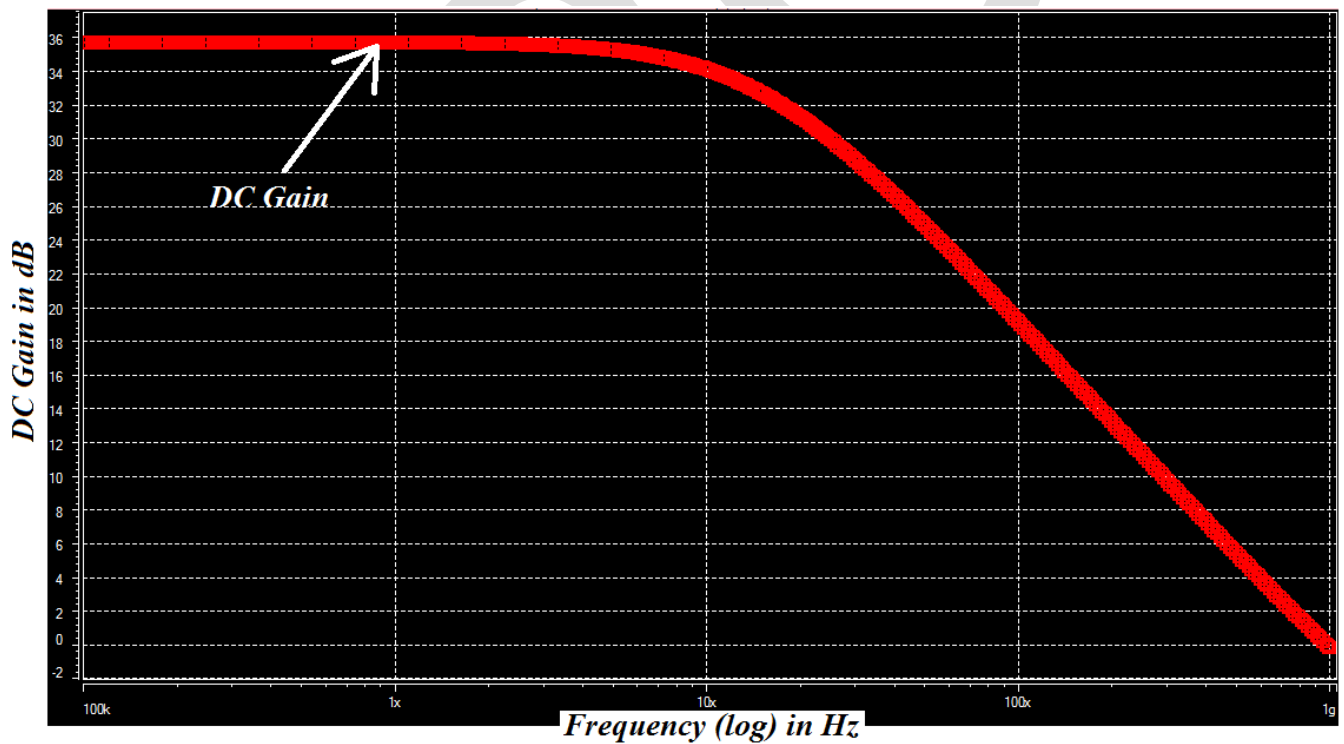


Figure2: Frequency response of CMOS based folded cascode op amp design at 1.4V

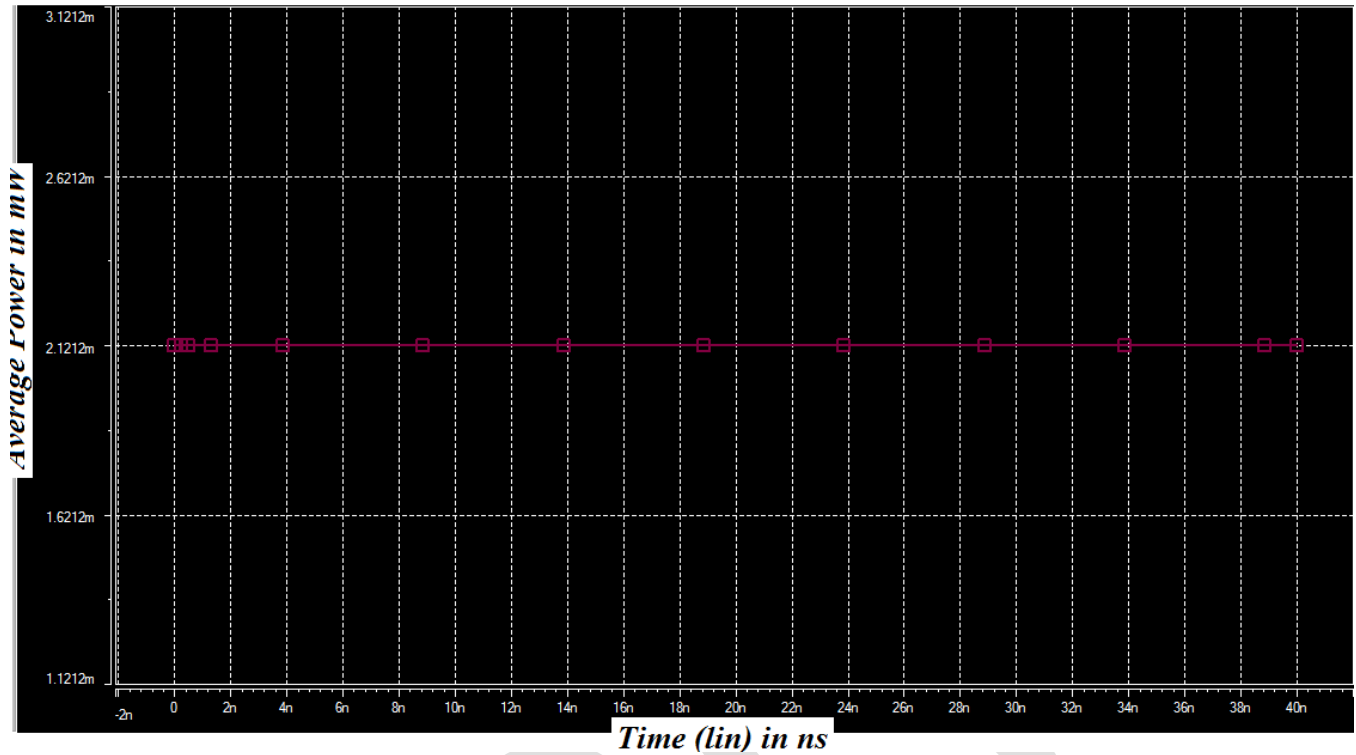


Figure 3: Average Power of CMOS based folded cascode op amp design at 1.4V

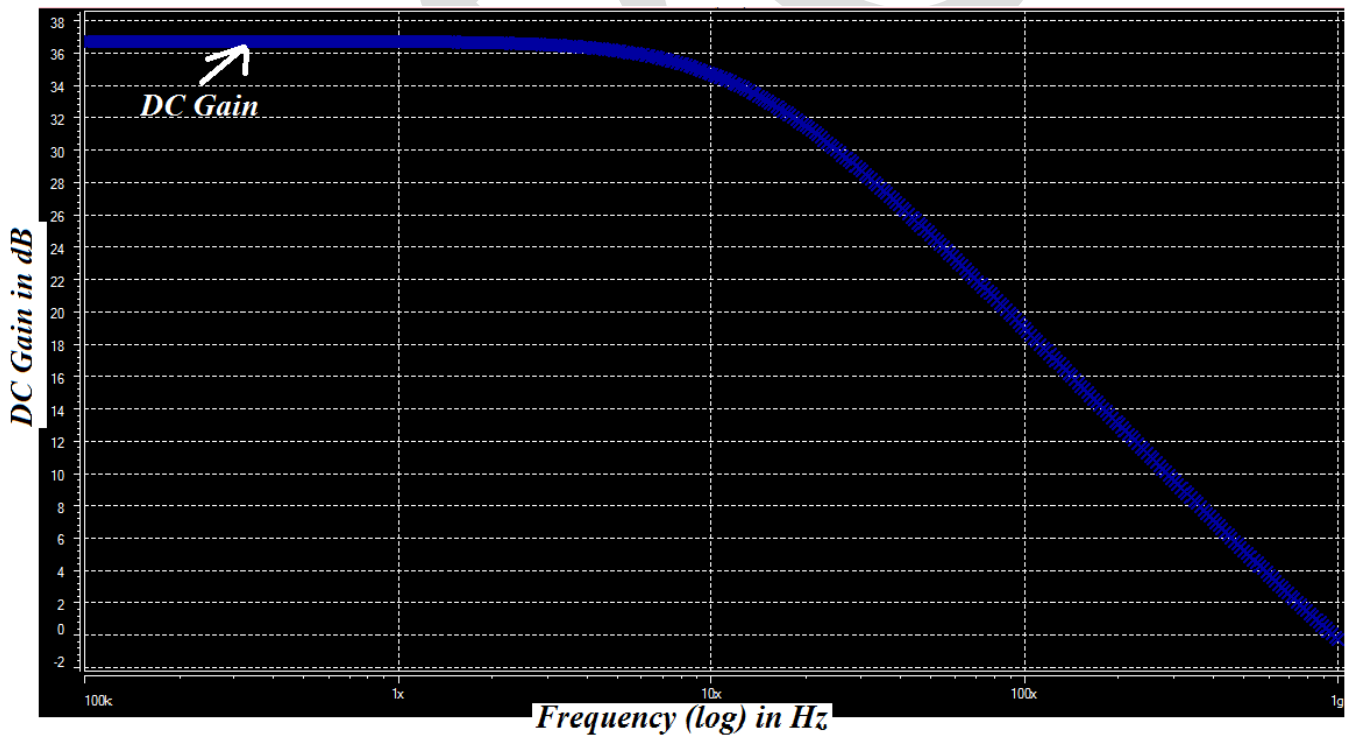


Figure4: Frequency response of CMOS based folded cascode op amp design at 1.2V

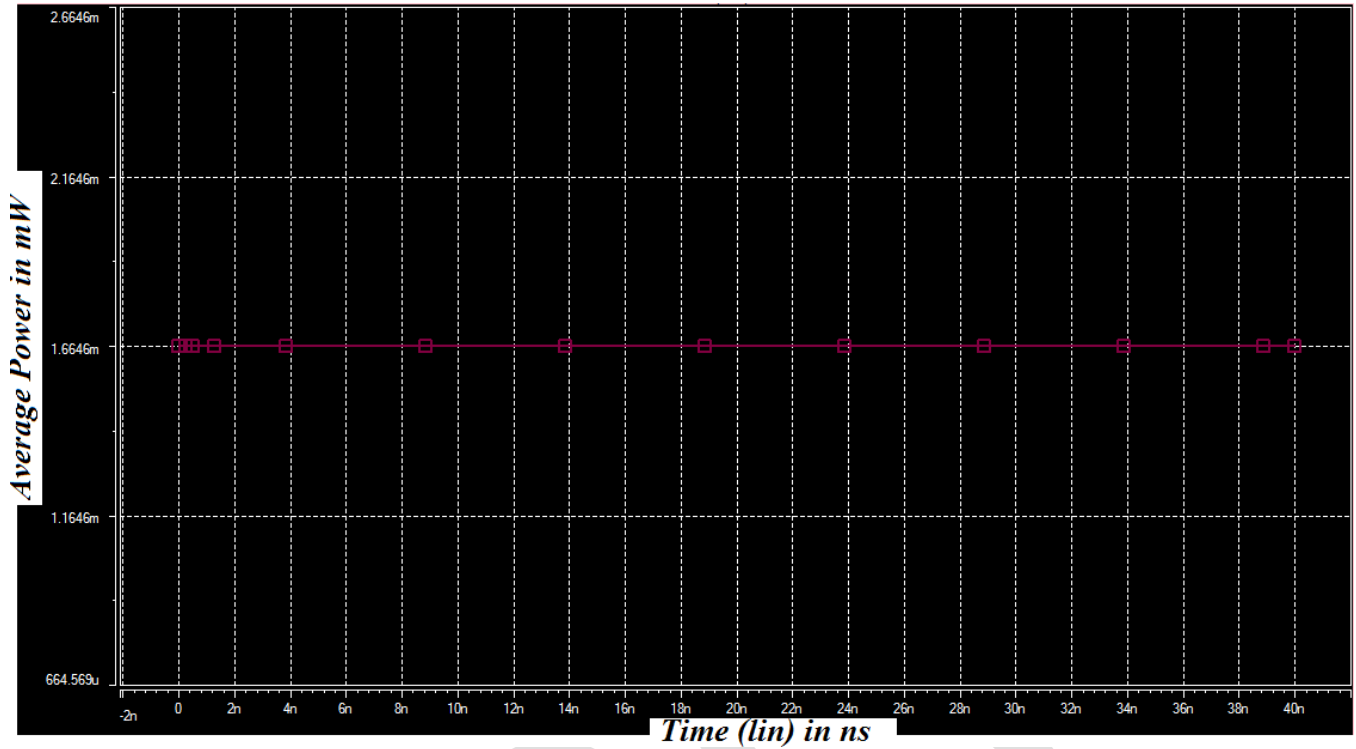


Figure 5: Average Power of CMOS based folded cascode op amp design at 1.2V

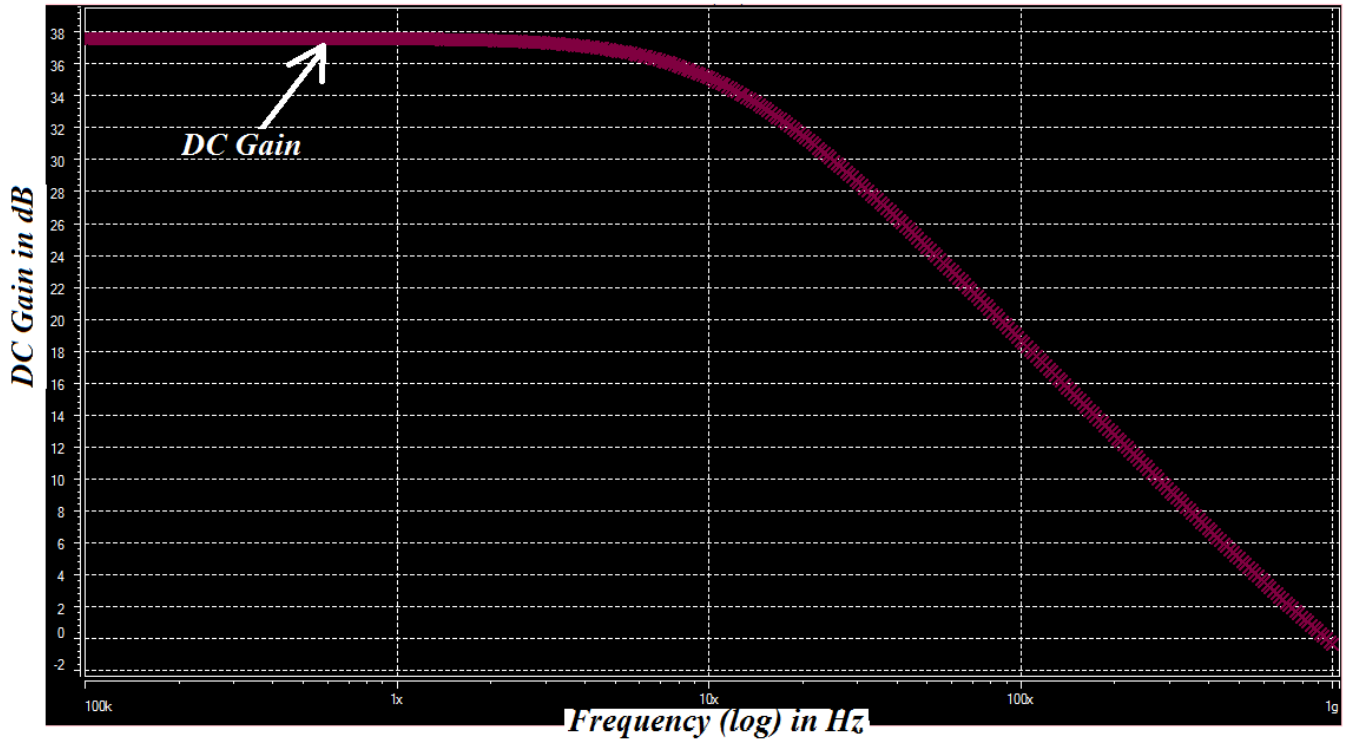


Figure6: Frequency response of CMOS based folded cascode op amp design at 1 V

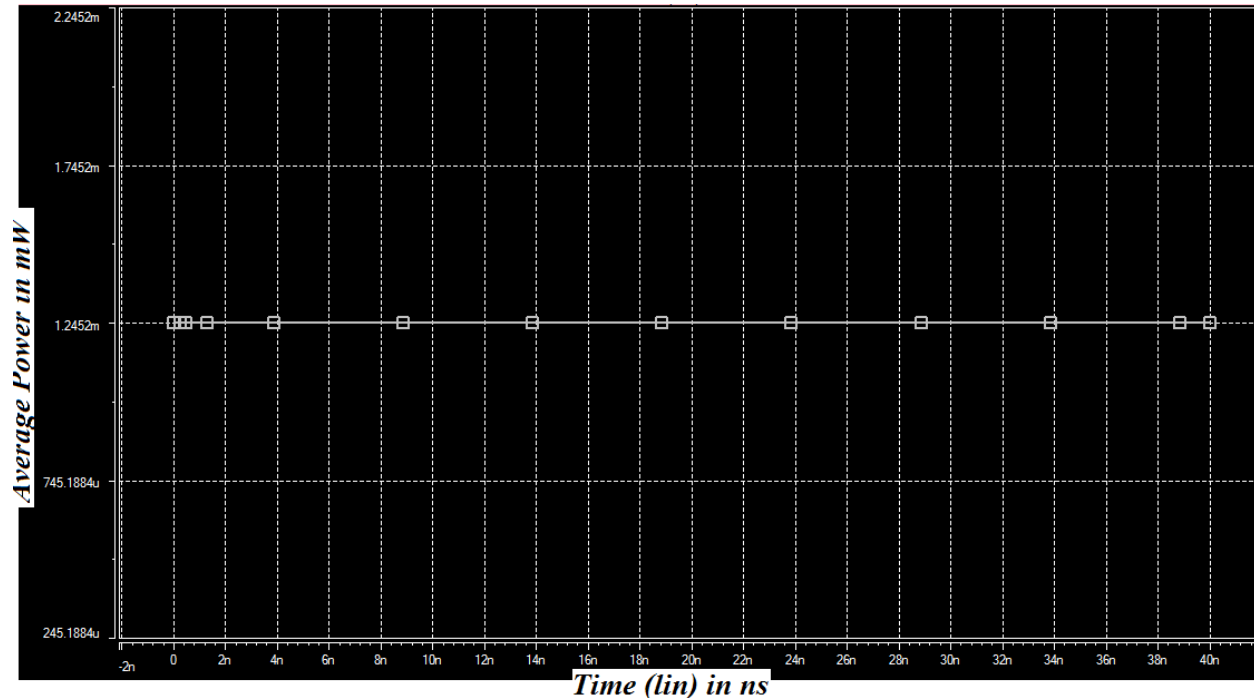


Figure 7 Average Power of CMOS based folded cascode op amp design at 1V

Table 1: Comparative analysis of Folded Cascode Op Amp Design with $C_L = 1$ pf, at different V_{DD} .

S. NO.	PARAMETERS	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1V	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1.2V	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1.4 V
1	DC GAIN	37.6 dB	36.7 dB	35.7 dB
2	Unity Gain Freq	951 MHz	963 MHz	978 MHz
3	Output Resistance	23.1 Ohms	23.4 Ohms	24 Ohms
4	Average Power	1.24mW	1.66mW	2.12 mW
5	Phase Margin	79.2 ^o	80.5 ^o	81 ^o
	Slew Rate	8.57E+8	1.1E+9	1.3E+9

III. CONCLUSION

In this research paper, simulation of low voltage folded cascode Op Amp based on different voltages has done at 45 nm .DC voltage gain, average power, Unity gain bandwidth and output resistance have been computed using HSPICE Software . low voltage folded cascode Op Amp results in high performance. The proposed low voltage Cascode Op Amp is better for applications in VLSI design for low voltage applications.

REFERENCES:

- [1] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58, 2010.
- [2] S.Sinha,A.Balijepalli,Yu Cao,"Compact Model of Carbon Nanotube Transistor and Interconnect",IEEE Trans on Electron Devices,Vol.56,No.10,Oct.2009.

- [3]Phan Minh,Phan Hong Khoi,"Carbon Nanotube: A novel material for applications", APCTP-ASEAN Workshop on Advanced Materials & Nanotechnology, Journal of Physics: Conf. Series 187 (2009).
- [4]J.Appenzeller et.al.,"Carbon Nanotubes as potential building blocks for future nanoelectronics ", Elsevier,Microelectronics Engineering 64(2002).
- [5] R.T.Bate et.al.,"An overview of nanoelectronics",Texas Instruments Tech.J.pp.1,July/Aug-1989.
- [6]D.G.Gordon,M.S.Montemerlo,J.C.Love,G.J.Opiteck,J.M.Ellenbogen"Overview of Nanoelectronics Devices", Proceedings of IEEE, Vol 85 ,No.4,April 1997.
- [7]Wei Zhang et.at.,"Modeling of Carbon Nanotube Field –Effect Transistor with Nanowelding treatment", Elsevier,Microelectronics Engineering 40(2009).
- [8]H.S PhilipWong et.at.,"Carbon Nanotube Transistor Circuits-Models and Tools for Design and Performance Optimization",ICCAD'06 Nov 5-9,2006.
- [9]Adrian Bachtold,et.at.,"Logic Circuits with Carbon Nanotube Transistor",Science Mag, Vol 294 , Nov 9,2001.
- [10]Zhihong Chen et.at.,"An Integrated Logic Circuit Assembled on a Single Carbon Nanotube",ScienceMag,BREVIA Vol 311,Mar 24 ,2006.
- [11] T. Agarwal, A. Sawhney, A.K. Kureshi, M. Hasan, Performance comparison of CNFET and CMOS based full adders at the 32 nm technology node, Proceedings of VLSI Design and Test Symposium (VDATE) (2008) 49–57 Bangalore, India.
- [12] R.Jacob Baker,"CMOS Circuit Design ,Layout and Simulation" 3rd Edition , IEEE Series on Microelectronic Systems, page 797.
- [13] H.-S. P. Wong, "Beyond the Conventional Transistor," IBM Journal of Research & Development, Vol. 46, Issue 2.3, March 2002, pp. 133-168.
- [14] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong and F. Breuf , "The Road to the End of CMOS Scaling ", IEEE Circuits Devices Magazine, Vol. 21, 2005, pp. 16 -26.
- [15] P. Avouris, "Supertubes: the Unique Properties of Carbon Nanotubes May Make Them the Natural Successor to Silicon Microelectronics," IEEE Spectrum, Vol. 41, no. 8, August 2004, pp. 40-45.
- [16]. Hashempour H, Lombardi F: Circuit-level modeling and detection of metallic carbon nanotube defects in carbon nanotube FETs. DATE07 2007.
- [17]. Lin Sh, Kim YB, Lombardi F, Lee YJ: A new SRAM cell design using CNTFETs. IEEE ISOC 2008.
- [18]. Avouris P, Appenzeller J, Martel R, Wind S-J: Carbon nanotube electronics. Proc of IEEE 2003, 1772:1784.
- [19] P. Grade, —Transconductance cancellation for operational amplifiers, "IEEE J. Solid-State Circuits", vol. SC-12, pp. 310–311, June 1977 .
- [20]] R. Harjani, R. Heineke, and F. Wang, "An integrated low-voltage class AB CMOS OTA," IEEE Journal of Solid-State Circuits, vol. 34, pp. 134-142, 1999.