



Simulation, hardware implementation and control of a multilevel inverter with simulated annealing algorithm

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ABSTRACT

Harmonic pollution is a very common issue in the field of power electronics, Harmonics can cause multiple problems for power converters and electrical loads alike, this paper introduces a modulation method called selective harmonic elimination pulse width modulation (SHEPWM), this method allows the elimination of a specific order of harmonics and also control the amplitude of the fundamental component of the output voltage. In this work SHEPWM strategy is applied to a five level cascade inverter. The objective of this study is to demonstrate the total control provided by the SHEPWM strategy over any rank of harmonics using the simulated annealing optimization algorithm and also control the amplitude of the fundamental component at any desired value. Simulation and experimental results are presented in this work.

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1. Introduction

Electronic motor controllers play a major role in our daily life, these devices can be found anywhere especially in industrial applications. There are multiple types of power converters such as AC to DC, DC to DC and DC to AC. The Direct to Alternative Current converters (DC to AC) are the most used type of power converters for the control of alternating current motors. Cascade DC to AC multilevel inverters are suitable for high power applications they can withstand a huge amount of voltage stress ; they are also very easy to make and to maintain due to their modular structure. The conventional multilevel cascade configuration can be achieved by connecting multiple H-bridge modules in series ; this configuration will be briefly covered in this work. The harmonic content in an AC voltage waveform generated by an inverter can affect significantly the performance of AC machines. For example, harmonics can raise the temperature of an AC motor which

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decreases the lifetime of the insulation and consequently the lifetime of the motor itself. One way to fight this problem is by choosing the right modulation strategy. Several modulation strategies have been proposed and studied for the control of multilevel inverters such as Sinusoidal Pulse width modulation (SPWM) [1] and space vector pulse width modulation (SVPWM) [2]. A more efficient method called selective harmonic elimination pulse width modulation (SHE-PWM) is also used; the method offers a lot of advantages such as operating the inverters switching devices at a low frequency which extends the lifetime of the switching devices. The main disadvantage of selective harmonic elimination method is that a set of non-linear equations extracted from the targeted system model must be solved to obtain the optimal switching angles to apply this strategy. Multiple computational methods have been used to calculate the optimal switching angles such as Newton-Raphson (N-R) [3], this method dependent on initial guess of the angle values in such a way that they are sufficiently close to the global minimum (desired solution). And if the chosen initial values are far from the global minimum, non-convergence can occur. Selecting a good initial angle, especially for a large number of switching angles can be very difficult. Another approach is to use optimization algorithms such as genetic algorithm (GA) [4], firefly algorithm (FFA) [5] and particle swarm optimization (PSO) [6] and differential evolution (DE) [7]. The main advantage of these methods is that they are free from the requirement of good initial guess. This article discusses the possibility of using the simulated annealing algorithm to solve the selective harmonic elimination problem, and also to demonstrate the possibility of eliminating any undesired harmonic of any rank. The simulated annealing algorithm was first introduced in 1979 by Armen G. Khachaturyan in and it was used in multiple applications such as solving facility layout problems [8], telecommunication network problems [9], optimal reactive power problem [10] and integrated circuits design [11]. In this work the SA algorithm is used to compute the optimal switching angles necessary for the SHEPWM method, in the case of a uniform step five level waveform, only one harmonic is eliminated and the fundamental component is controlled. This work is organized as follows the next section will present briefly the SHEPWM for multilevel inverters and the simulated annealing optimization method. The third section presents the obtained simulation results, simulation and experimental results are presented in the last section.

2. SHEPWM for Multilevel Inverts

2.1. Proposed converter and the SHEPWM strategy

The structure of the converter chosen in this study is presented in left side of figure 1, the converter consists of two H-bridges, each bridge is powered by its own isolated direct current power source Vdc_1 and Vdc_2 with $Vdc_1 = 25V$ and $Vdc_2 = 25V$, this particular configuration can generate five voltage levels. In order to apply the SHEPWM strategy to this inverter the generated output voltage waveform has to be a simple stepped signal, the left side of figure 1 illustrates a generalized form of a uniform stepped voltage waveform with θ_1 and θ_2 are the optimal angles to be computed in order to eliminate the undesired harmonics and control the fundamental component simultaneously.

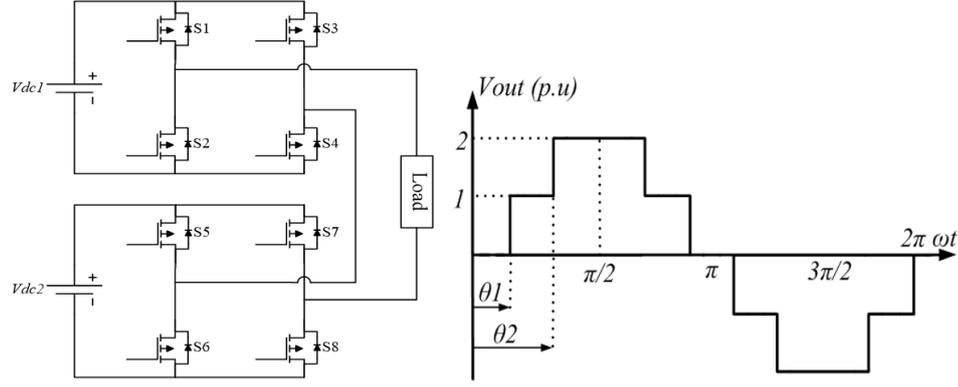


Fig. 1 – Schematic of the proposed multilevel converter (Left) Generalized five level voltage waveform (Right).

The number of voltage levels that can be generated by Cascade multilevel inverters is generally presented by $2P+1$ where P represents the number of voltage levels or switching angles in a quarter waveform of the signal, and $P-1$ is the number of undesired harmonics that can be eliminated from the generated waveform. In a five level inverter with uniform step voltage waveform, the number of voltage levels generated in quarter waveform is two plus the zero level which means only one harmonic can be eliminated. To control the peak value of the output voltage and eliminate any harmonic, with quarter and half wave symmetry characteristics of the voltage waveform are taken in consideration, the Fourier series expansion is given as :

$$V(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \left[\frac{4V_{dc}}{n\pi} \sum_{i=1}^p \cos(n\theta_i) \right] \sin(n\omega t) \quad (1)$$

Where n is rank of harmonics, $n = 1, 3, 5, \dots$, and $p = (N - 1)/2$ is the number of switching angles per quarter waveform., and θ_i is the i^{th} switching angle, and N is the number of voltage levels per half waveform. The optimal switching angles θ_1 and θ_2 can be determined by solving the following system of non-linear equations :

$$\begin{cases} H_1 = \cos(\theta_1) + \cos(\theta_2) = M \\ H_n = \cos(n\theta_1) + \cos(n\theta_2) = 0 \end{cases} \quad (2)$$

Where $M = (((N - 1)/2)r/4)$, r is the modulation index end. The obtained solutions must satisfy the following constraint :

$$0 < \theta_1 < \dots < \theta_p < \pi/2 \quad (3)$$

An objective function is necessary to perform the optimization operation, the function must be chosen in such way that allows the elimination of low order harmonics while maintaining the amplitude of the fundamental component at a desired value Therefore the objective function is defined as :

$$f(\theta_1, \theta_2) = \left(\sum_{n1}^2 (\cos(\theta_n) - M) \right)^2 + \left(\sum_{n1}^p (\cos(n\theta_n)) \right)^2 \quad (4)$$

The optimal switching angles are obtained by minimizing Eq (4) subject to the constraint Eq (3). The main problem is the non-linearity of the transcendental set of Eq (2), the simulated annealing is used to overcome this problem.

2.2. Simulated annealing

The simulated annealing is a stochastic global optimization method that can differentiate between multiple local optima points. The algorithm is inspired from the process of cooling metal after heating it to get a perfect crystal structure with minimum defects. While many optimization methods get stuck in a local minimum instead of converging to a global minimum, the simulated annealing solves this problem by performing a random search. Figure (2) presents a simplified flowchart of the simulated annealing algorithm.

The algorithm deals with the minimization of an objective function using a parameter called temperature to evaluate the probability of accepting worst values to escape local minima. The algorithm starts by defining the values of parameters and algorithm operators, and also sets the temperature parameter T to an initial value with initial set of solutions. In this algorithm new random solutions are generated for each iteration, if the newly generated solution improves the objective function $f(x)$ expressed in (4) and gave better result than the previous one, then the proposed solution is accepted. Another technique to evaluate the improvement of the system, is to accept the new random solution with a likelihood according to a probability of $e^{-\Delta f}$, where Δf is the variation of the objective function, this variation can be expressed by the following equation.

$$\Delta f = f(x^k) - f(x^{k-1}) \tag{5}$$

Where k is the current iteration.

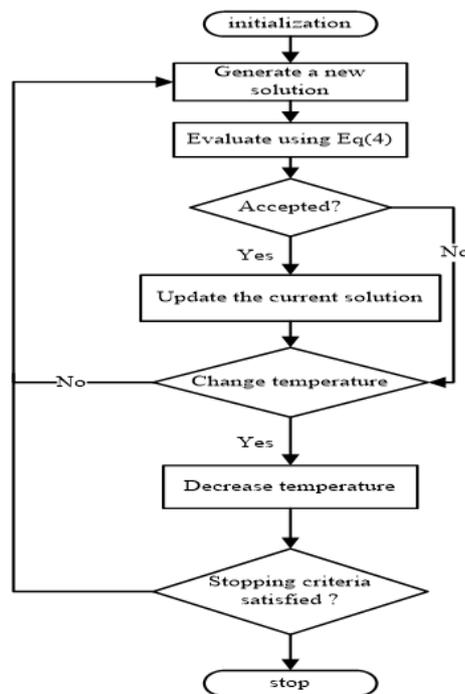


Fig. 2 – Generalized five level voltage waveform.

3. Simulation Results

In order to prove the theoretical predictions and to test the effectiveness of the proposed algorithm, the control method and the mathematical model of the proposed inverter were developed and simulated using MATLAB/SIMULINK scientific programming environment ; the optimization program was executed on a computer with Intel(R) Core(TM) i3 CPU@ 2.13GHz Processor and 4GB of RAM, the optimization algorithm takes 127.43 seconds to complete the computation process.

The left side of figure (3), figure (4) and figure (5) show the generated waveforms in the case of eliminating the third, fifth and the seventh harmonics respectively, and for different modulation indices r where $r_1 = 0.7$, $r_2 = 0.85$ and $r_3 = 0.9$, whereas the left side of the same figures show the FFT analysis of the generated waveforms for the above mentioned cases and also for different values of r . It can be noticed from the voltage waveforms that by decreasing the modulation index, the switching angles will have higher values and this will lead to a decrease in the amplitude of the fundamental component this effect can be clearly observed in the FFT analysis figures. And also it can be clearly seen from the FFT analysis that the undesired harmonics were successfully eliminated in each case, for example in figure (3) the third harmonic was eliminated while the fifth harmonic remained untouched, whereas in figure (4) the fifth harmonic was eliminated while the third and the seventh harmonics remained untouched.

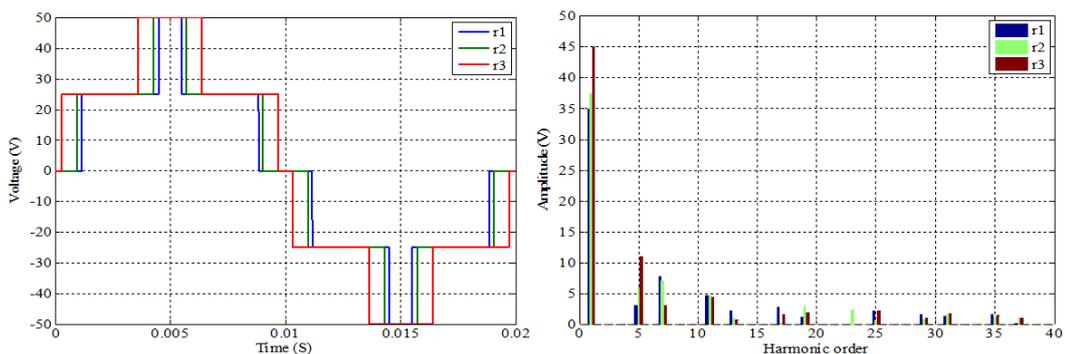


Fig. 3 – Generated Voltage waveforms (Left) and FFT analysis (Right) in the case of eliminating the third harmonic.

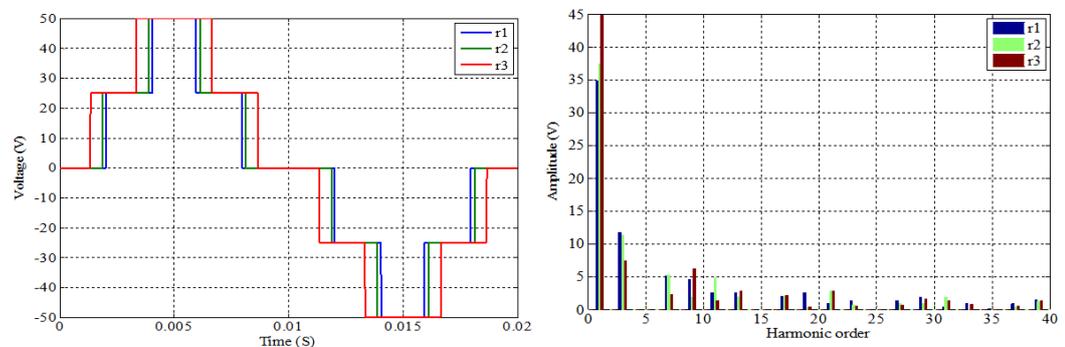


Fig. 4 – Generated Voltage waveforms (Left) and FFT analysis (Right) in the case of eliminating the fifth harmonic.

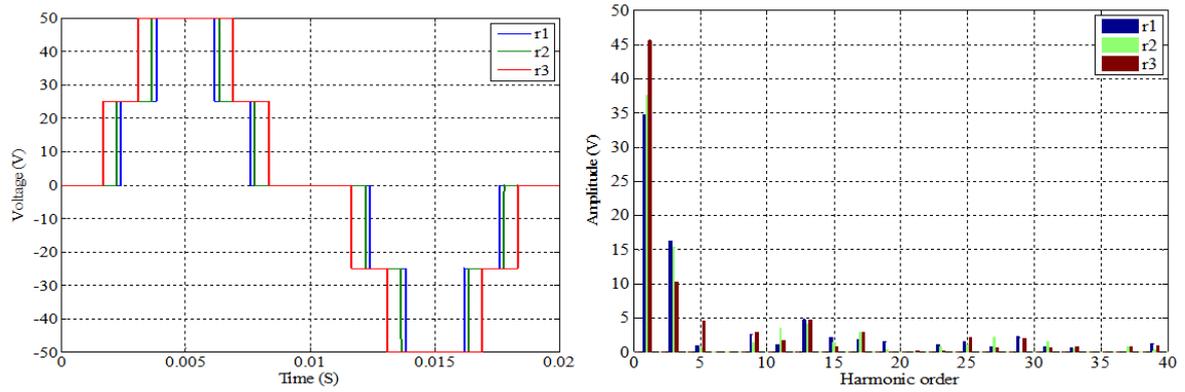


Fig. 5 – Generated Voltage waveforms (Left) and FFT analysis (Right) in the case of eliminating the seventh harmonic.

4. Experimental Results

A five level inverter prototype was built to validate the results obtained from the simulation process; Irf640 MOSFETS were used as switching devices for the proposed inverter, 4N25 optocouplers were used to protect the microcontroller used in this experiment, Siglent SDS 1000 oscilloscope with FFT capability was used to preview the voltage waveforms and to perform FFT analysis. The left side figure 6, figure 7 and figure 8 show the experimental waveforms in the case of eliminating the third, fifth and seventh harmonic respectively, and each waveform was generated for a particular value of modulation index r . The right side of same figures show the FFT analysis of generated waveforms for the cases mentioned previously, and it can be clearly seen that the third, fifth and the seventh harmonics were successfully eliminated, and also it can be noticed that there is a slight change in the value of the fundamental component.

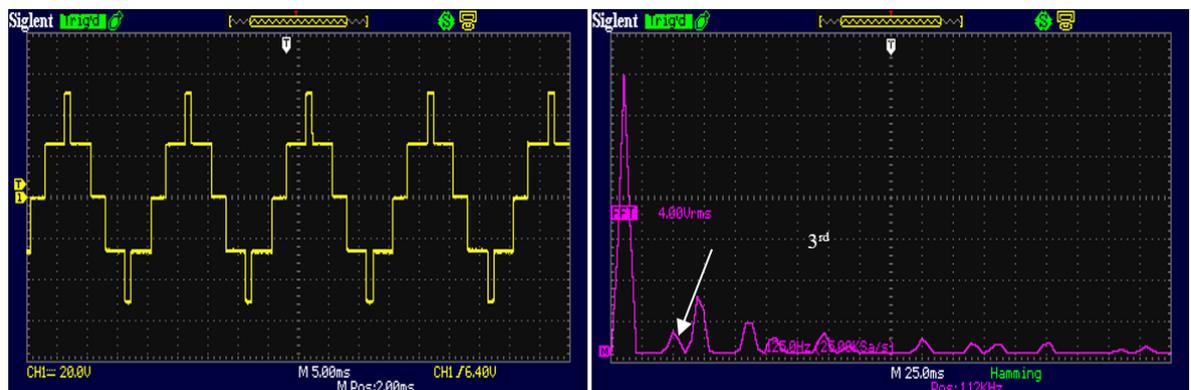


Fig. 6 – Generated Voltage waveforms (Left) and FFT analysis (Right) in the case of eliminating the third harmonic $r = 0.7$.

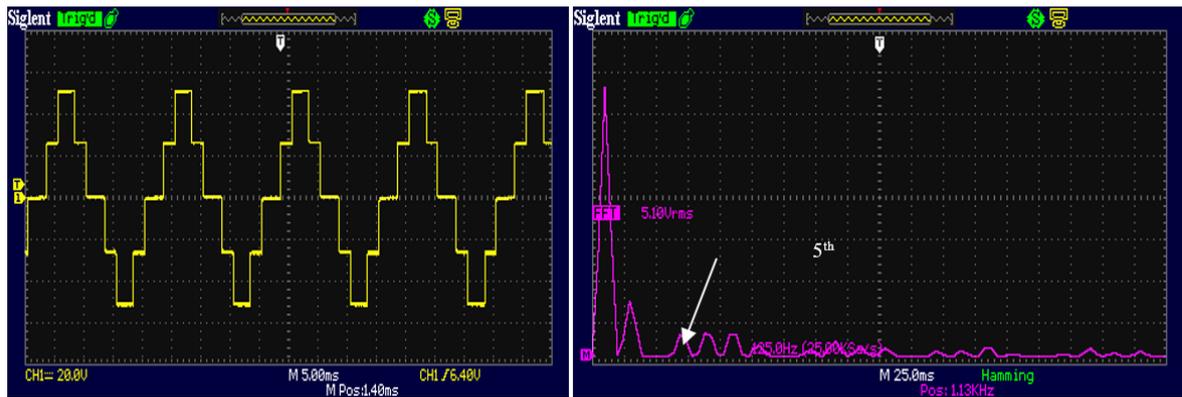


Fig. 7 – Generated Voltage waveforms (Left) and FFT analysis (Right) in the case of eliminating the fifth harmonic $r = 0.85$.

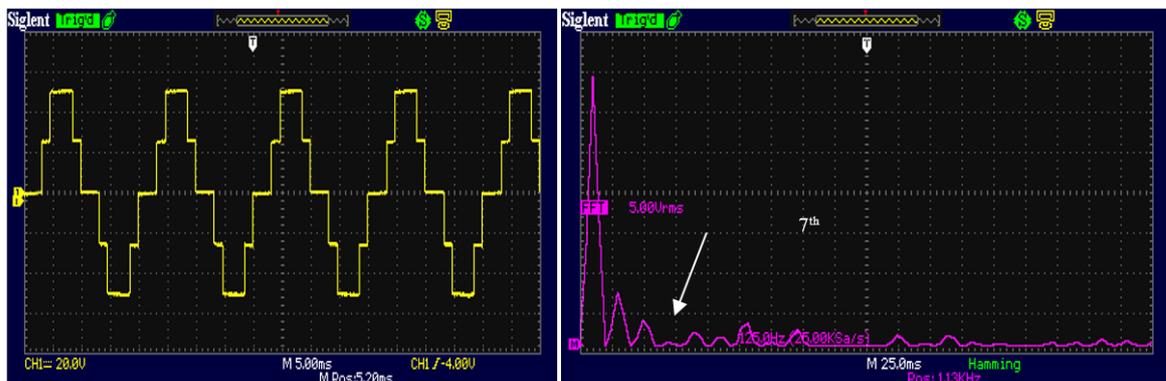


Fig. 8 – Generated Voltage waveforms (Left) and FFT analysis (Right) in the case of eliminating the seventh harmonic for $r = 0.9$.

5. Conclusion

This paper demonstrated the ability of the selective harmonic elimination strategy for multilevel inverters of eliminating any undesired harmonics and maintain the fundamental component at a desired value, and also the possibility of using the simulated annealing algorithm to solve the optimal switching problem for multilevel inverters. The set of non-linear equations that describe the overall system are solved to obtain the optimal switching angles using the proposed optimization algorithm which belongs to the physics inspired optimization methods. The selective harmonic elimination strategy was tested in this paper for multiple situations and different values of modulation index r in order to prove the efficiency of this control method. Simulation and experimental results show a great agreement in this work.

REFERENCES

[1] Karami, B. Barzegarkhoo, R. Abrishamifar, A. and Samizadeh, M., 2015 .A switched-capacitor multilevel inverter for high AC power systems with reduced ripple loss using SPWM technique, In Power Electronics, Drives Systems & Technologies Conference , pp. 627-632.

- [2] Jana, K. C. and Biswas, S. K., 2015. Generalized switching scheme for a space vector pulse-width modulation-based N-level inverter with reduced switching frequency and harmonics, in *IET Power Electronics*, vol. 8, no. 12, pp. 2377-2385.
- [3] Mistry, T. Bhatta, S. K. Senapati, A. K. and Agarwal, A., 2015, May. Performance improvement of induction motor by Selective Harmonic Elimination (SHE) using Newton Raphson (N-R) method, In *International Conference on Energy Systems and Applications*, pp.364-369.
- [4] Deniz, E. Aydogmus, O. and Aydogmus, Z., 2016. Implementation of ANN-based Selective Harmonic Elimination PWM using Hybrid Genetic Algorithm-based optimization, In *Measurement*, Vol. 85, pp. 32-42.
- [5] Gnana Sundari, M. Rajaram, M. and Balaraman, S., 2016, April. Application of improved firefly algorithm for programmed PWM in multilevel inverter with adjustable DC sources, In *Applied Soft Computing*, Vol. 41, pp.169-179.
- [6] Letha, S. S. Thakur, T. Jagdish, K. 2016, July. Harmonic elimination of a photo-voltaic based cascaded H-bridge multilevel inverter using PSO (particle swarm optimization) for induction motor drive, In *Energy*, Volume 107, pp. 335-346.
- [7] Chabni, F., Taleb, R., Mellakhi, A., 2016, Elimination of Harmonics in Modified 5-Level CHB Inverter Using DE Algorithm, *Mediterranean Journal of Modeling and Simulation (Med. J. Model. Simul.)*, vol. 6, no. 1, pp. 23-33.
- [8] Grobelny, J. and Michalski, R., 2017, March. A novel version of simulated annealing based on linguistic patterns for solving facility layout problems, In *Knowledge-Based Systems*.
- [9] Valdivieso, C. Novillo, F. Gomez, J. and Dik, D., 2016, Centralized channel assignment algorithm for WSN based on simulated annealing in dense urban scenarios, 2016 In *8th IEEE Latin-American Conference on Communications*, pp. 1-6.
- [10] Raha, S. B. Mandal, K. K. and Chakraborty, N., 2013, Parametric variation based simulated annealing for reactive power dispatch," In *IET Chennai Fourth International Conference on Sustainable Energy and Intelligent Systems*, pp. 29-34.
- [11] Sadiq M. Sait, Oughali, F. C. and Al-Asli, M., 2016, Design partitioning and layer assignment for 3D integrated circuits using tabu search and simulated annealing, In *Journal of Applied Research and Technology*, Volume 14, Issue 1, pp 67-76.