International Journal of Engineering Research and General Science Volume 4, Issue 2, March- April, 2016
ISSN 2091-2730

Design and Implementation of Binary Motion Vector technique with Pruning DWT for Video Compression

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Abstract— Now days, video quality is a very important factor in entertainment world. A movie could be interesting only because of its quality and its graphics. To send and store these videos, we have to compress them, rejecting part of the unneeded data to reduce the video capacity. Video Compression algorithms combine Spatial image compression and Temporal motion compression.The sequence of frames contains Spatial and Temporal redundancies that Video Compression algorithms attempt to eliminate or code in smaller size.In this paper,We presented a design of Binary motion vector technique with Pruning Discrete Wavelet Transform for the compression of AVI video.Here,Binary motion vector technique used for searching the Best matching block.This technique requires less candidates block than other motion vector technique. Pruning based DWT uses thresholding which enhanced the compression ratio with desirable Peak Signal to Noise ratio .This algorithm has simulated on XilinxISE13.1 and Model Sim 6.2c and implemented on SPARTEN3 FPGA. Hardware implementation of algorithm consumes 15% of slices on Xilinx SPARATEN3 FPGA with maximum operating speed of 198MHz.

Keywords— Video compression,Binary motion vector algorithm,Block Matching,Pruning DWT,MATLAB,Compression ratio,FPGA

I. INTRODUCTION

Video is an illusion that makes use of the properties of eye. Eye has a peculiar property that image sensed by eye persists for 1/30th of a second and video clips are made up of sequences of individual images, or "frames." Video compression is essential for developers of embedded systems, processors, and tools targeting video applications. In order to achieve compression of video signals, motion estimation between the successive frames is performed which contributes significant bit saving by transmitting only the motion vectors. This is the most computationally intensive operation in the coding and transmitting of video signals. For this, Block Matching is the most preferred Motion Estimation technique. BM divides the video frames into NxN pixel blocks and tries to find the block from the reference frame in a given search range that best matches the current block. Sum of Absolute Differences (SAD) is the most preferred block matching criterion because of its low computational cost.The block with minimum SAD is then taken as Best reference block. Among the BM algorithm, Full search algorithm achieves the best performance since it searches all search locations in the given search range. But, its computational complexity is very high, it requires huge hardware and large candidate blocks[1].Many Frequency based techniques are also used which uses Fourier Transform. But if we compare fourier Transform with DWT. then, DWT is effective because it has multiresolution capability. Wavelets are signals which are local in time and scale and generally have an irregular shape. The wavelet transform can be seen as a decomposition of a signal in the time-scale plane. Once this is done the coefficients of the wavelets can be decimated to remove some of the details. Wavelets have the great advantage of being able to separate the fine details in a signal. Different types of wavelets also present which has different features. One particular wavelet may generate a more sparse representation of a signal than another So, we are using here Binary Motion Vector technique with Pruning DWT.

The binary motion vector technique classifies each block to a class, in which each pixel is given a value of "0" , "1","2","3", depending on the pixel value after the Frequency transformation.. When the reference block has the same class of the current block, this reference block is considered a candidate block, and otherwise the reference block is rejected. Then after adding the 64 pixels of the block, this block is classified as one of 8 classes. This algorithm will be implemented on FPGA.

II. PREVIOUS WORK

Many algorithms are proposed in the literature for the Video compression which requires less computational complexity. Fast search methods such as three step search, square search, diamond search and hexagon search can be used instead of FS algorithm [6]. Square and diamond search is used to determine the BRF of the current block, and this BRF is searched using FS algorithm in literature. In the literature [5],Arithmatic encoding and Run length encoding algorithm is implemented.Here, Discrete cosine transform is used to convert each pixel value into frequency domain.RLE algorithm is easy to implement but not gives high compression ratio. In the literature[1],Multiple reference frame motion estimation is used.This algorithm uses number of reference frames for each macro block and early termination. This hardware has less energy consumption.

III. PROPOSED WORK

We are using Binary Motion vector technique with Pruning DWT and then the algorithm will be implemented on Xilinx Sparten3 FPGA.First,input to the DWT is given in form of frames. For this,Video is divided into Frames using MATLAB tool. We are taking the Video of different format .The flowchart of algorithm is given in the following figure1.

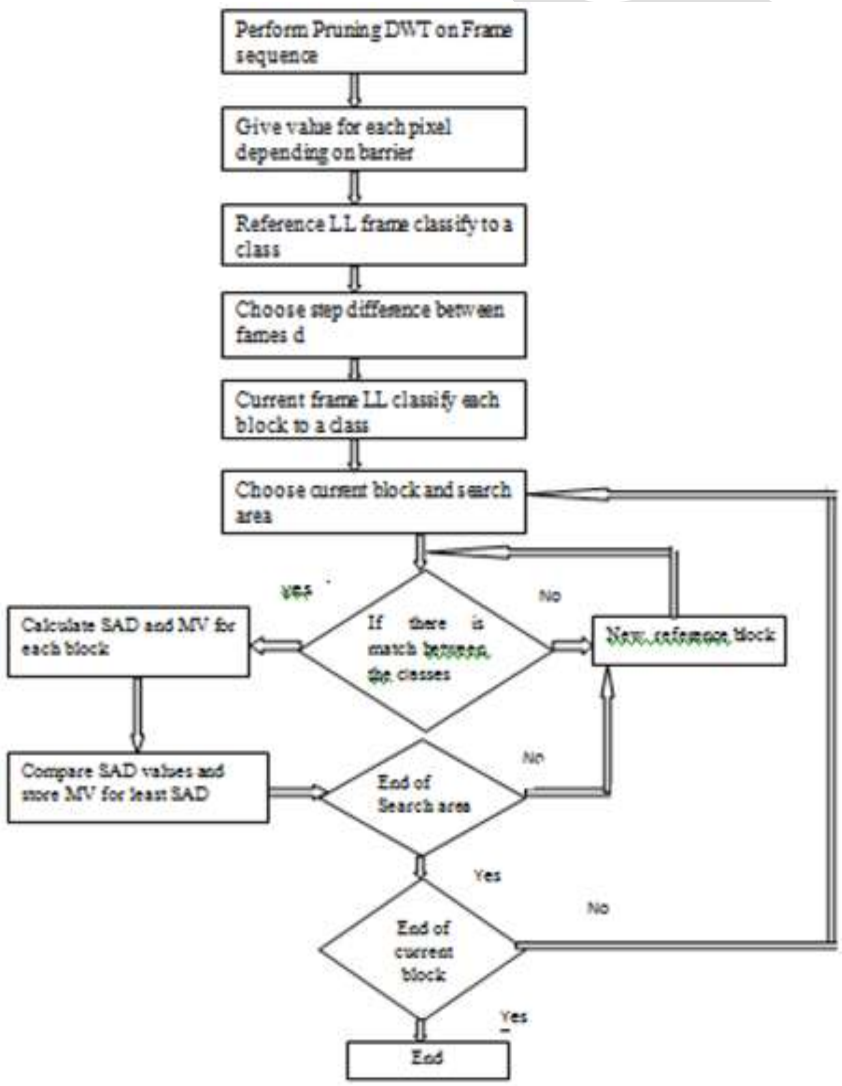

Figure 1: Flowchart of algorithm

A] Pruning based DWT

Due to a wavelet transform,a signal can be decomposed into many shifted and scaled representation of original mother wavelet. Many wavelets display a property ideal for compact signal representation: orthogonality.

This property ensures that data is not over represented.

A wavelet function Ψ(t) has two main properties,

$$\int_{-\infty}^{0} \Psi(t)dt = 0;$$

That is, the function is oscillatory or has wavy appearance,

$$\int_{-\infty}^{0} \left|\Psi(t)\right|^2 dt < \infty;$$

That is, the most of the energy in Ψ(t) is confined to a finite duration.

the proposed compression technique with pruning proposal based on discrete wavelet transform (DWT) first decomposes an image into coefficients called sub-bands and then the resulting coefficients are compared with a threshold. Coefficients below the threshold are then taken as zero and coefficients above the threshold value are encoded.

B] Proposed algorithm

Architecture of proposed algorithm is shown in the figure2.It consist of main blocks such as block creater unit, accumulator unit, class unit,SAD unit amd comparator unit. Here,step difference is taken as distance between the reference frame and current frame.If step difference is 4 then it take 4 reference frame. In DWT, each frame is divided into four quarters, Low Low (LL) coefficients having the image information, High Low (HL) coefficients, Low High coefficients (LH) and High High (HH) coefficients having only the sharp edges of the image.After transformation, LL coefficients are used in the process while LH, HL and HH coefficients are sent to the decoder to be used in retrieving the frames. After retrieving these frames, these frames are used as reference frame. After transformation, LL quarter is divided to 8x8 pixel blocks, each pixel is given a number depending on its value. We then add all the values of all pixels, Then the block is classified to a class of 8 classes. Compare the current block to the corresponding block in the reference frame; in addition to all the blocks in a search area. Where the search area is a square area of 7 blocks above the corresponding block in the reference frame, 7 blocks below, 7 blocks right and 7 blocks. Candidate blocks are selected if having the same class, a higher class or a lower class. Calculate the Sum of Absolute Differences (SAD) between the candidate block and the current block, the block with the least SAD is the best matching one. MV is calculated for the best matching block.MV and residuals are sent, this method is applied for all block in the current frame.

In the architecture of algorithm, there is control unit that control the entrance of frames at the DWT unit where each pixel coefficients transformed into Discrete wavelet coefficients. We only take the LL coefficients by the help of the control unit. After transformation, each pixel coefficient is divided by "2", in order to operate on 8 bits instead of 9 bits.then coefficients will take to the block creater unit where coefficients will be put in matrix form.in this way one by one all frames enters and stored in the RAM. When each frame is transformed, the control unit orders the RAM to save data in its place. At the same time, after filling the matrix in the block creator unit, the control unit controls the process of releasing each coefficient to the class stage, in a block manner. A simple 2 counters in the control unit manage this process, each coefficient in the barrier block take a value of "0" or "1" or "2" "3"or”4”depending on the number of frames. and then flows to the accumulator block, where summation of the pixel coefficients takes place. then the summation flows to the class look-up table to classify the block to a class number. The class will be saved in the RAM in an address after to the block addresses.To save data in the RAM,RAM is divided into the number of stages depending on the number of frames entering.

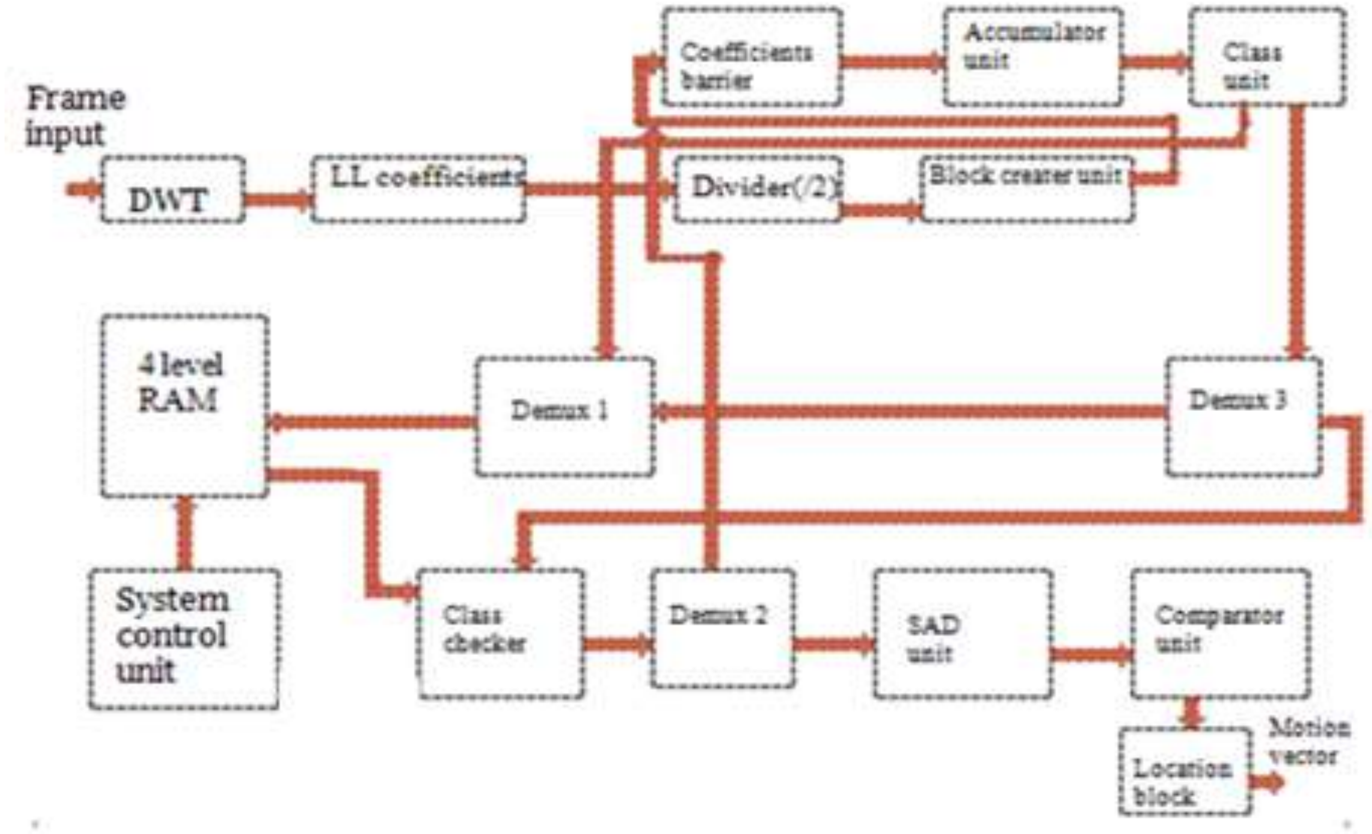

Figure2: Proposed algorithm design

For the current block,we have to calculate motion vectors. the control unit calls the 1st main block to the class checker unit, where it will pass normally as its class is calculated, then to Demux 2 where the control unit makes it pass to the SAD block.The control unit calls for blocks in search area.

The control unit produces a number called the location number which is number of candidate block in the search area. The class checker then calls for each candidate block,if the class was calculated. Then it will goes to the SAD unit. Demux 2 allows this block to flow back to the class stage, in order to calculate the candidate block class, in case the block is a overlapping not a main block. The main block is the block that when the frame is divided regularly to blocks, these blocks are main ones, but that doesn't mean that the frame doesn't have any other blocks than these.There can be overlapping bloks. So the possibility that the best matching candidate block in the overlapping blocks is much more than the main blocks.Demux3 is to send the data back to the class checker where it makes sure if the class is calculated. the candidate block data flows through DEMUX 2 to the SAD unit. Now two blocks are in the SAD block, the SAD value is calculated.Then SAD values will go to the comparator unit where it compares two values till we get least SAD values.after that block with least sad value is taken as best matching block.Finally, its location number flows to the location block where the MV is calculated. This process is then done for all blocks of the current frame of video.

IV. RESULTS

The proposed architectures of algorithm has simulated using VHDL language using Xilinx 13.1 ISE. It has been implemented on Xilinx 13.1ISE,SPARTAN 3FPGA .We have taken three videos of AVI,3GP,FLV and retrieved frames for each videos. For each video, Performance is measured in the form of parameters like Compression rate, PSNR ratio. Results of three videos are shown below

Figure 3: Original frame

Figure 4: Retrieved frame

Video	Original file size (KB)	Compressed file size (KB)	Compression rate(%)	PSNR(db)
1	2310	769	3	30

Figure 5: Original frame

Figure 6: Retrieved frame

Video	Original file size (KB)	Compressed file size (KB)	Compression rate(%)	PSNR(db)
2	2310	769	3	33

Figure 7: Original frame

Figure 8: Retrieved frame

Video	Original file size (KB)	Compressed file size (KB)	Compression rate(%)	PSNR(db)
3	3850	769	5	38

Performance of Proposed algorithm and area utilization on Xilinx Spartan 3 FPGA

Video	Original file size(KB)	Compressed file size (KB)	Maximum frequency (MHz)	Used no. of slices	Compression	No. of LUT's used
1	38500	769	198	15%	50%	20

V. CONCLUSION

In this paper, We proposed Binary Motion vector algorithm architecture which improves the video quality and compression ratio. Also, Pruning DWT is applied on the frames of video to store the image in few coefficients which is useful for compression of video. In comparison of DCT, DWT has many advantages like multi resolution. It improves compression. Here, SAD parameter is used as measuring parameter for best matching block. It requires less computational complexity and easy to implement. Our proposed algorithm consumes 15% of slices on Xilinx SPARATEN3 FPGA with maximum operating speed of 198MHz.

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