

Removal of DC Imperfections in Op-Amps by using DC Restoration Technique

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Abstract— This paper gives us a brief idea about the removal of the DC imperfections in operational amplifiers which occurs due to the mismatches of current or voltage at inverting and non-inverting terminal of Op-Amp. These DC imperfections are considered to be errors in Op-Amps as DC errors. We need to take care of these errors so that, using Op-Amp in signal conditioning system should work properly in order to obtain the desired output.

Keywords— Operational Amplifier, DC imperfections, Input Offset Voltage, Input Offset Current, Input Bias Current, Signal Conditioning, DC Restoration.

INTRODUCTION

Operational Amplifiers, or Op-Amps as they are more commonly called, are one of the basic building blocks of Analog Electronic Circuits. *Operational amplifiers* are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation.

An **Operational Amplifier**, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or “operation” of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of “Operational Amplifier”. [2]

Operation of Op-Amp

The amplifier's differential inputs consist of a non-inverting input (+) with voltage V_+ and an inverting input (–) with voltage V_- ; ideally the Op-Amp amplifies only the difference in voltage between the two, which is called the differential input voltage. The output voltage of the Op-Amp V_{out} is given by the equation:

$$V_{out} = A_{OL}(V_+ - V_-)$$

Where A_{OL} is the open-loop gain of the amplifier (the term "open-loop" refers to the absence of a feedback loop from the output to the input). [3]

Schematic symbol of Op-Amp:-

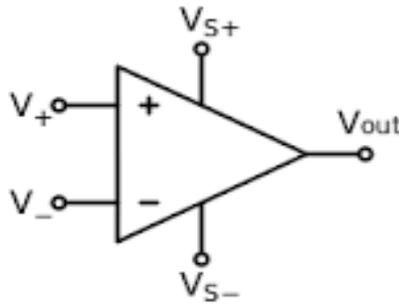


Fig. 1 Schematic symbol of Op-Amp

Ideal characteristic of Op-Amp:

1. Infinite voltage gain.
2. Infinite input resistance.
3. Zero output resistance.
4. Zero offset voltage.
5. Infinite bandwidth.
6. Infinite common mode rejection ratio (CMMR)
7. Infinite slew rate.
8. Zero power supply rejection ratio.[6]

Practical characteristic of Op-Amp:

1. Input offset voltage (V_{OS}) :

It is the voltage that must be applied between the two input terminals of Op-Amp to nullify the Output.

2. Input offset current (I_{OS}) :

The algebraic difference between the current entering into inverting and non-inverting input terminals of Op-Amp is called input offset current.

$$I_{OS} = |I_{B+} - I_{B-}|$$

Where I_{B+} & I_{B-} are currents at input terminals of Op-Amp.

3. Input bias current (I_B) :

The average of currents into inverting and non-inverting input terminals of Op-Amp is called input bias current.

$$I_B = \frac{I_{B+} + I_{B-}}{2}$$

4. Input resistance (R_i):

This is the differential input resistance as seen at either of the input terminals with other terminal connected to ground.

5. Input Capacitance:

It is the equivalent capacitance that can be measured at either of the input terminal with other terminal connected to ground.

6. Output resistance:

It is the resistance measured between the output terminal of Op-Amp and ground.

7. Supply current:

It is the current drawn by Op-Amp from power supply.

8. Power consumption:

It is the amount of quiescent power that must be consumed by Op-Amp so as to operate properly.

9. Voltage gain:

It is the ratio of output voltage to differential input voltage.

10. CMRR (common mode rejection ratio) :

It is the ratio of differential mode voltage gain to common mode voltage gain, It is measured in decibels (dB).

$$CMRR = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$$

11. SVRR (supply voltage rejection ratio):

It is the change in the Op-Amp's input offset voltage due to variation in supply voltage.

12. Output voltage swing:

It indicates the value of positive or negative saturation voltages of an Op-Amp.

13. Output short circuit current:

This is the current that may flow if an Op-Amp may get shorted accidentally.

14. Slew rate:

It is defined as maximum rate of change of output voltage per unit time.

15. Gain bandwidth product:

It is bandwidth of Op-Amp when voltage gain is unity. [6]

From all of the above characteristics the input offset voltage, input offset current and input bias current are the DC imperfections which causes DC errors in the any signal conditioning system which are described as follows.

Input offset voltage V_{OS} :

In the circuit of Fig.2, with $v(+)=v(-)=0$, the output voltage is ideally zero, $V_o = 0$. Due to unavoidable mismatches in the characteristics of the devices in the input differential stage of the Op-Amp, the output voltage is not zero. Instead, a small DC voltage would have to be applied between the Op-Amp input terminals to set the output voltage to zero. The input offset voltage V_{OS} is defined as the voltage that results in zero output $V_o = 0$ when applied between the (+) and (-) input terminals. The input offset voltage, which is ideally zero, is considered a random quantity that can take positive or negative values in a certain worst-case range around zero. Figure 2 shows a model of an op-amp with the input offset voltage V_{OS} .

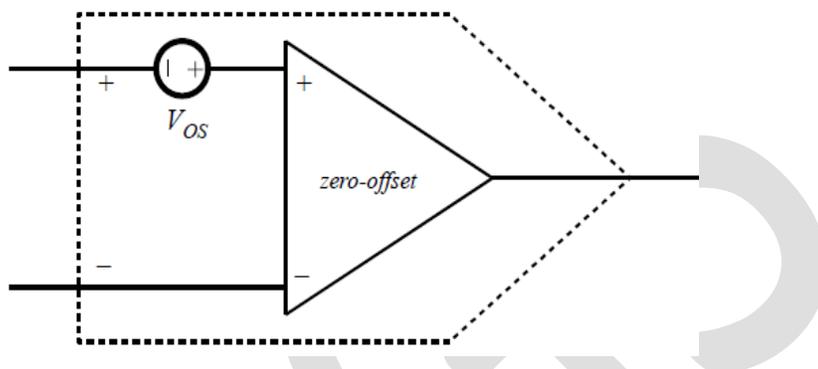


Figure 2: Model of an op-amp with the input offset voltage V_{OS} .

The model simply consists of an ideal, zero-offset Op-Amp model, and a dc voltage source V_{OS} in series with one of the input terminals. Since the sign of V_{OS} is not known in advance, the reference polarity of the offset voltage source in series with one of the inputs is arbitrary. [4]

As an example, let us consider the effects of the input offset voltage on the operation of the analog integrator. Using the model of Fig. 2, the circuit model of the integrator is shown in Fig. 3.

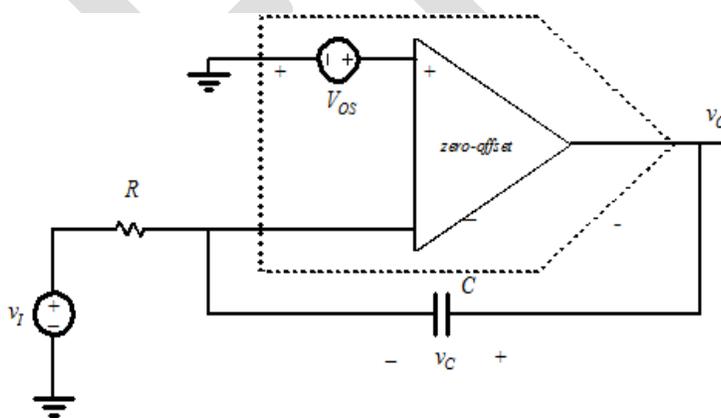


Figure 3: Model of the analog integrator circuit using an op-amp with input offset voltage V_{OS} .

Suppose that $V_I = 0$, and that the circuit is powered up at time $t = 0$. Let the initial value of the capacitor voltage V_C be zero, $V_C(0) = 0$. Assuming the op-amp has very large open-loop voltage gain, $v(-) = V_{OS}$, and the current V_{OS}/R charges the capacitor up (or down, depending on the sign of V_{OS}), until the output voltage reaches one of the saturation limits, $V_{o,max}$ if $V_{OS} > 0$, or $V_{o,min}$ if $V_{OS} < 0$. Therefore, the DC operating point of the analog integrator is at one of the saturation limits

$$V_0(t) = V_{OS} + \frac{1}{C} \int_0^t \frac{V_{OS}}{R} dt$$

$$V_0(t) = V_{OS} + \frac{1}{C} \frac{V_{OS}}{R} t$$

Input bias current I_B :

The input bias current I_B is the dc bias current flowing into (or out of) the op-amp input terminals. The input bias current is required for proper operation of the op-amp input transistor stage. The sign and the nominal value of I_B are known, and are usually given in op-amp data sheets. For op-amps with bipolar junction transistors, the input bias current is typically in the order of μA . For CMOS op-amps the input bias current, which is much smaller (in the order of pA), can usually be neglected. Figure 4 shows an op-amp model with non-zero input bias currents. [4]

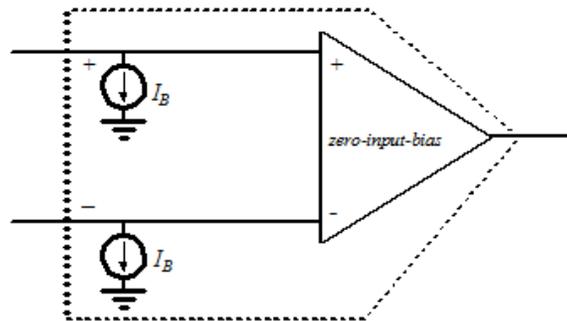


Figure 4: Model of an op-amp with the input bias currents I_B .

As an example, applying the model of Fig. 4 in the analog integrator, we get the circuit model in Fig. 5.

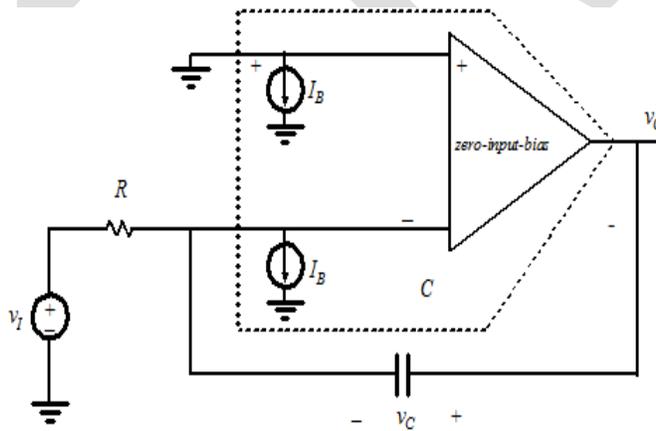


Figure 5: Model of the analog integrator circuit using an op-amp with input bias currents I_B .

Suppose that $V_I = 0$, and that the circuit is powered up at time $t = 0$. Let the initial value of the capacitor voltage V_C be zero, $V_C(0) = 0$. Assuming the op-amp has very large open-loop voltage gain, $v(-) = 0$, and the current I_B charges the capacitor up (or down, depending on the sign of I_B), until the output voltage reaches one of the saturation limits, V_{Omax} if $I_B > 0$, or V_{Omin} if $I_B < 0$. Therefore, because of the input bias currents, the DC operating point of the analog integrator is again at one of the saturation limits, even if the input offset voltage were equal to zero.

$$V_0(t) = \frac{I_B}{C} t$$

Input offset current

So far, we have assumed that the input bias currents for the (+) and (-) terminals are the same, $I_+ = I_- = I_B$. In practice, because of mismatches in the op-amp input transistor stage, this is not the case, and we define the input offset current I_{OS} and the input bias current as

$$I_{OS} = |I_{B+} - I_{B-}|$$

$$I_B = \frac{I_{B+} + I_{B-}}{2}$$

The input offset current I_{OS} is typically at least an order of magnitude smaller than I_B . The offset current, just like the offset voltage, is considered a random quantity specified in a worst-case \pm range around zero. [8]

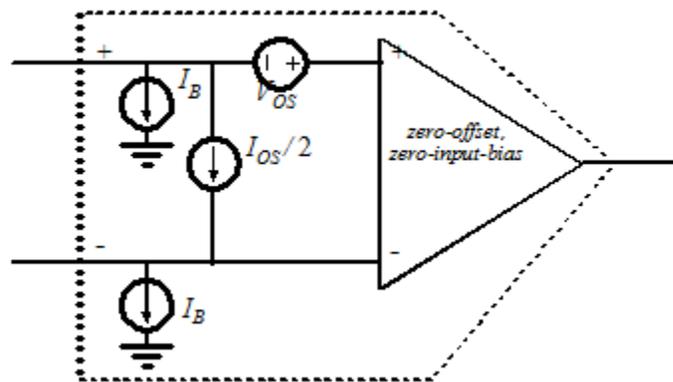


Figure 6: Model of an op-amp with the input offset voltage V_{OS} , the bias currents I_B , and the input offset current I_{OS} .

$$V_0(t) = V_{OS} + \frac{1}{C} \frac{V_{OS}}{R} t + \frac{I_{B-}}{C} t$$

DC RESTORATION TECHNIQUE

To eliminate the effect of input offset voltage, input bias current and input bias voltage on Operational Amplifiers we need a DC restoration circuit which will compensate these DC errors and make the circuit error free.

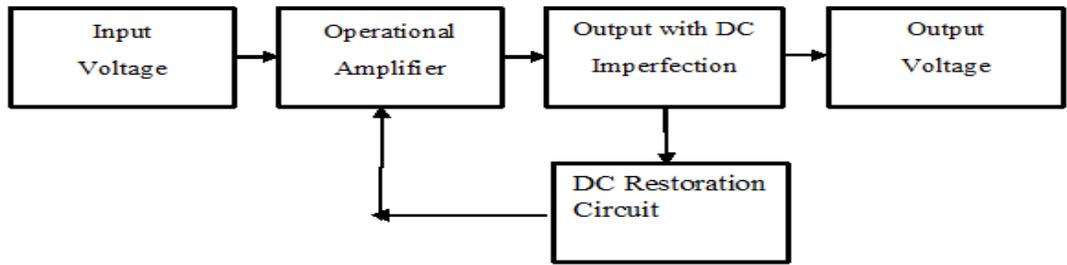


Fig.7 Block diagram of signal conditioning system with DC restorer Circuit

The AC input signal is applied to the operational amplifier which will get amplified with a certain gain depending upon external feedback components such as resistors and capacitors between its output and input terminals. This output signal obtained from the Op-Amp may not be the desired one because of DC imperfections which also get amplified by Op-Amp and appears at the output with given input signal. These DC imperfections are considered as an error which affects the operation of Op-Amp and leads to saturation state.

In order to remove these errors in Op-Amp the DC restoration Technique is used here. In this technique DC voltage along with the AC which appears as the output of the Op-Amp is integrated by Integrator, with the proper selection of feedback components R and C the AC signal at the input of the Integrator is attenuated with certain gain $1/j\omega RC$ and DC signal will get amplified with a very large gain in this way only amplified DC appear at the end at the output of the Integrator this signal is fed back to the input of the Op-Amp in such a way that it subtracts the DC imperfections which appears at the output. This process continues till all the DC at the output gets eliminated.

OBSERVATION AND RESULTS:

Following results shows us that the AC signal is amplified with a constant gain and DC imperfections are eliminated.

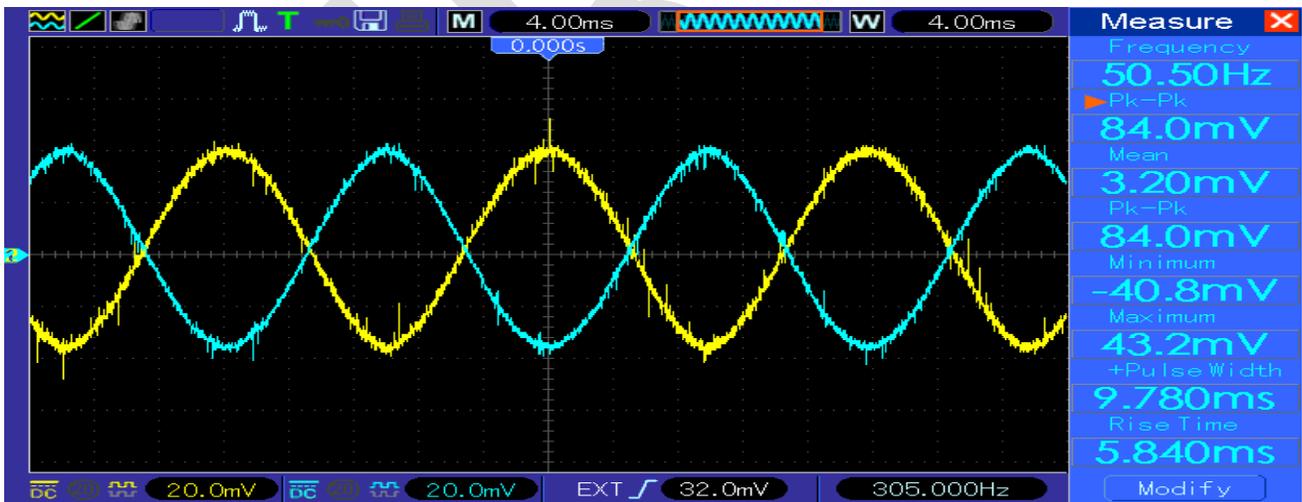


Fig.8 input and output waveform at 50Hz frequency

As we can see in the following Fig.9 and Fig.10 even though an external positive or negative offset is added to the input, there is no change in the output.

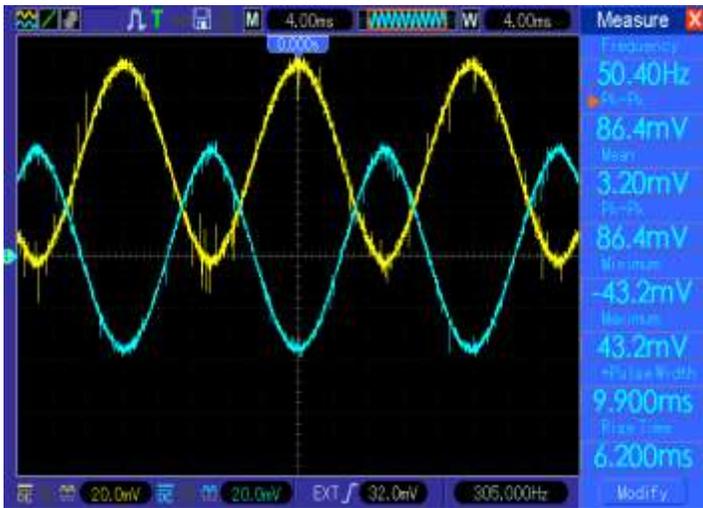


Fig.9 input and output waveform at with positive offset
 at 50Hz frequency

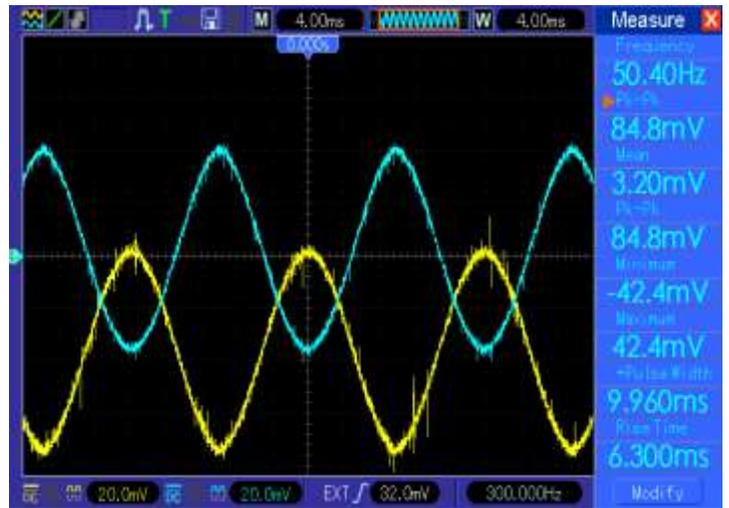


Fig.10 input and output waveform at with negative offset
 at 50Hz frequency

Following table shows us that at various frequencies starting from 50 Hz and downwards, The gain of the circuit remains constant.

AC frequency in Hertz with Constant 100mV (peak-peak)input Vin	Output of Op-Amp (Peak-peak)(mV) Vo
50	84
40	84
30	84
20	84
15	84
14	84
13	86
12	86
11	86
10	86
9.5	86
9	86
8.5	88
8	88
7.5	90
7	92
6.5	92
6	92

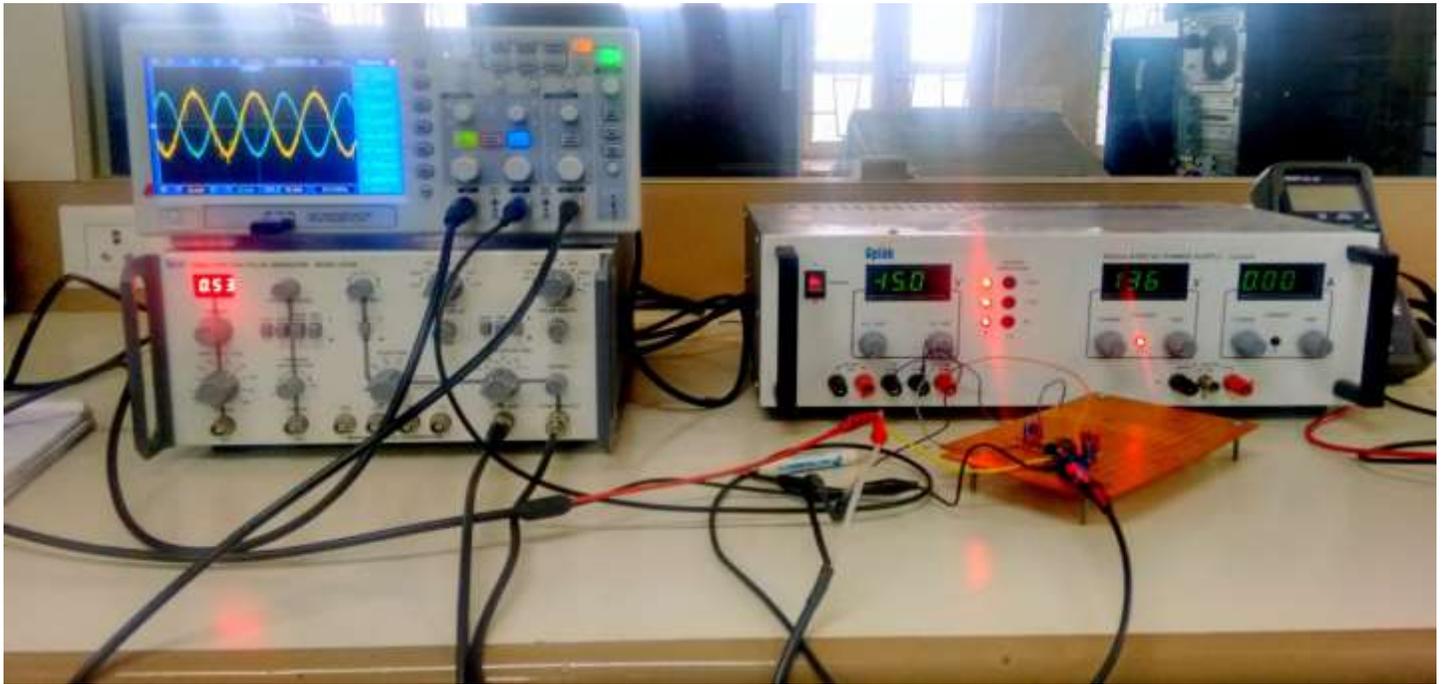


Fig. 11 The Entire testing Set-up

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CONCLUSION

The results of a typical DC restoration circuit which was designed to restore DC voltage have been reported in this paper using an experiment conducted by addition of external DC to the signal and removing this DC component from the output using a DC restoration circuit. Low-frequency signals are also processed successfully without any distortion.

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