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Sobel Edge Detection Implementation using Spartan 3 FPGA and Xilinx System Generator

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Abstract— This paper presents implementation of an image processing algorithm applicable for edge detection of an image in Xilinx Spartan 3 FPGA by using System Generator. Usually Sobel edge detection algorithm is preferred which is most trustworthy and gives an efficient output. If VHDL code is written for this algorithm in Xilinx FPGA then it is too time consuming and bulky. Here the system is designed by using Xilinx System Generator blocks. This tool has high level graphical interface under the environment of MATLAB. Since FPGA has large embedded multipliers and internal memory, it offers parallelism. Hence, it provides platform for real time processing with higher performance than microprocessor programmable and Digital Signal Processor (DSPs).

Keywords— *Edge detection, FPGA, MATLAB, Real-Time image processing, Sobel operator, Xilinx system generator,*

I INTRODUCTION

In lower level image processing edge detection plays very important role. Quality of detected edges has significant role in image segmentation, scene analysis, focused area Selection, object recognition. For accurate edge extraction, both changes in the colour and changes in the brightness between neighbouring pixels should be demoralized. Many forceful and complex edge detection techniques have been presented in the previous literatures. These provide different outputs and particulars to the same input image. Here Sobel operator based edge detection technique is used and is extended for real-time applications. Due to the property of counteracting the noise sensitivity Sobel operator for edge detection over other gradient operators are chosen. The Sobel operator commonly known as Sobel filter is used for image processing and computer vision, which creates an image which focuses edges and transitions. It is discrete differentiation operator that calculates the gradient approximation of the image intensity function. The result of the Sobel operator is the corresponding gradient vector at that particular point. The Sobel operator convolves the image with an integer valued filter in vertical and horizontal direction so it is thus relatively cheaper in terms of computations. The gradient estimation that it produces is relatively simple for high frequency variations in the image.

II LITERATURE REVIEW

For real time image processing a vast work is done in the field of feature extraction. Edge detection is primary step for any image processing process; it provokes great interest for the systematic community. Edge detection alters the image for human interpretation and information extraction in various fields such as in biomedical processing, satellite communication, traffic monitoring, land acquisition, etc. Image edge detection with Hardware co-simulation is implemented over Xilinx Virtex 5 board using XSG in [2]. For optimized parameter Sobel edge detection algorithm is implemented over hardware platform in [3]. Real time FPGA based tracking and counting system for people is proposed. Spartan 3E is used as hardware platform in [4]. Simplified approach is proposed in [5] for vehicle edge detection for traffic analysis by hardware implementation using 'Xilinx System Generator. In [6] high throughput rate is achieved for FPGA based implementation of sobel edge detection algorithm by maximum utilization of FPGA resources. Comparative analysis is proposed in [7] for hardware and software based video surveillance. Hardware implementation tends to yield faster results. FPGA based object detection utilizing edge information proposed to offer high speed, energy efficient design in [8]. Machine implementation and pattern analysis is projected using canny edge detection algorithm with satisfactory results in [9].

III SOBEL EDGE DETECTION ALGORITHM

The Sobel operator is kind of first order edge detection operator. It calculates the gradient of image intensity function. The resultant gradient at every point in the image is given by Sobel standard. There are only two convolutions that is 0 and 90 degree convolution

kernel used by this Sobel operator. The gradient magnitude at each point is calculated by adding these individual kernels. The magnitude of gradient is given by

$$GM(x,y)=\sqrt{Hx^2 + Hy^2} \text{ - - - - - - - - - (1)}$$

$$Hx=\begin{bmatrix}-1 & 0 & 1\\ -2 & 0 & 2\\ -1 & 0 & 1\end{bmatrix} \text{ and } Hy=\begin{bmatrix}-1 & -2 & -1\\ 0 & 0 & 0\\ 1 & 2 & 1\end{bmatrix}$$

Hx (Convolution kernel in x direction) and Hy (Convolution kernel in y direction)
The magnitude of gradient at each point given by

$$GM(x , y) = | Hx | + | Hy$$

This helps in much faster computation. The advantage of sobel operator is its simplicity in computation. Since edges are detected with aid of two convolution kernel so it has less accuracy.

IV PROPOSED MODEL

The proposed model is as shown in figure 1. Here the input image is taken from MATLAB workspace. The processing is done on input image which basically includes resizing and filtering. After this Sobel edge detection algorithm is designed in Xilinx system generator using system generator blocksets. The output image is displayed using display controller unit in MATLAB which provides edge detected result of input image.

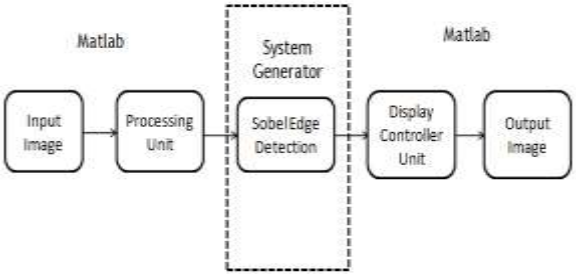

Figure 1: Proposed Model

V DESIGN METHODOLOGY

The figure below describes design methodology for the Sobel edge detection algorithm. Firstly Sobel edge detection is implemented using Xilinx blocksets in MATLAB environment. After that VHDL code is generated from the designed algorithm. Synthesis is done by using Xilinx ISE 10.1 which provides dumping on FPGA for hardware implementation.

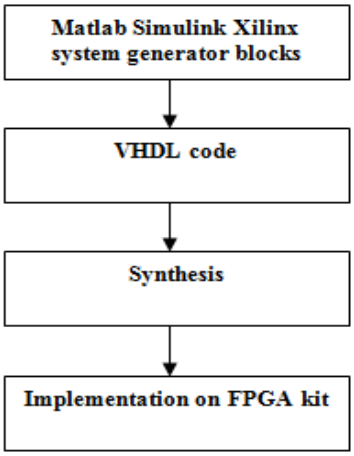

Figure 2: Design Methodology

VI SYSTEM IMPLEMENTATION

The system implementation involves horizontal and vertical gradients which require following Xilinx blocksets whose functions are summarised as follows

System Generator- Each design must have at least one system generator token which is used for VHDL code and bit file generation.

Resource Estimator- It defines how many FPGA resources we are going to require for the entire implementation of an algorithm.

Gateway In and Gateway Out (D_{in} and D_{out})- They are used to define input and output boundary of the FPGA. Gateway In is used to convert floating point data into fixed point data whereas Gateway Out is used to convert fixed point data into floating point data.

RGB to intensity- It is used to convert colour information between colour spaces.

Sub System- It is used for 2D to 1D conversion of an input image and vice-versa. It mainly includes frame converter and unbuffer.

Video Viewer- It is used to display image.

FIR filter- It performs filtering operations on image according to coefficients of each one of the filter.

Add Sub- performs the fast addition of Xilinx blocks

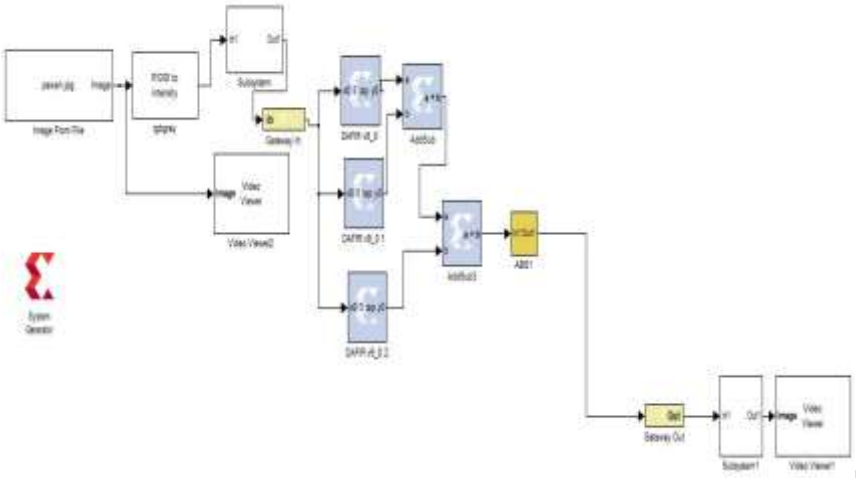

Figure 3: Complete Sobel Edge Detection Algorithm

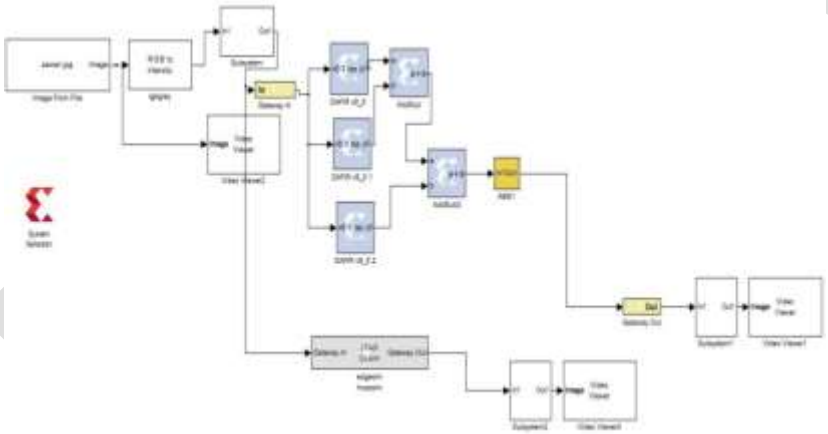

Figure 4: Complete Sobel Edge Detection Algorithm using JTAG hardware co-simulation block

VII HARDWARE IMPLEMENTATION

For hardware implementation of above design in FPGA board the whole design should be converted to format which is properly synthesizable to the FPGA. For this reason main module of edge detection is transformed to JTAG hardware co-simulation. This can be done by using System generator block; particularly its system generator token. According to the target platform this block is configured. Hardware co-simulation target is selected after the generation of bit stream file and in this proposed work for hardware implementation Spartan 3 FPGA kit is used. The entire architecture with the hardware and software co-simulation design is shown in figure 5.

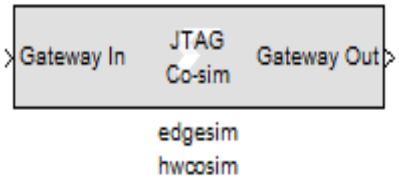

Figure 5: Generated JTAG hardware block via system Generator

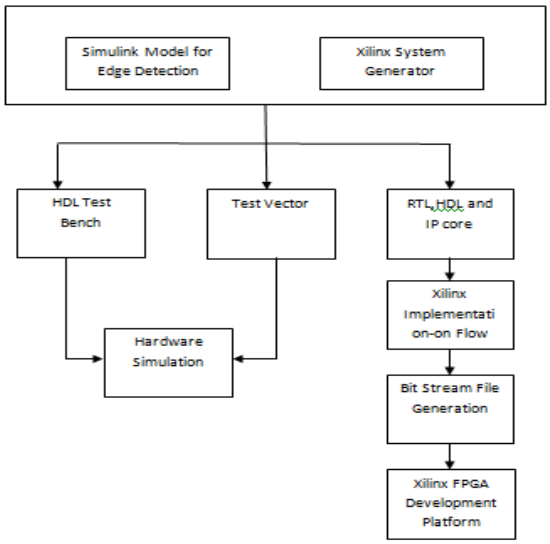

Figure 6: FPGA Hardware Implementation

The proposed algorithm is implemented on Xilinx Spartan Spartan 3 Part-XC3S200 FPGA Kit by generating VHDL code for Sobel operator using ISE design Suite10.1. The ISE design Suite10.1 hold design entry and synthesis that supports Verilog or VHDL, place and route which is used to configure the FPGA chip. Figure 7 shows the Spartan 3 FPGA Kit that is used in this work.

Figure 7: Xilinx Spartan 3 FPGA kit

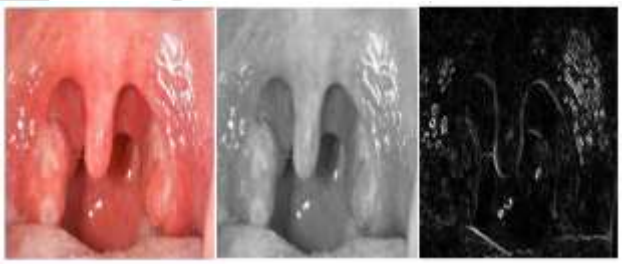

Figure 8: (a) Input Image; (b) Converted grayscale image; (c) Edge detected output image

Table 1 shows the device utilization summary generated for Xilinx Spartan 3 FPGA kit

Logic utilization	Used	Available	Utilization
Number of Slices	460	1920	23%
Number of Slice Flip Flops	769	3840	20%
Number of 4 input LUTs	611	3840	15%
Number used as logic	581	2408	24%
Number used as Shift registers	30	2408	1%
Number of bonded IOBs	0	97	0%

IX CONCLUSION & FUTURE SCOPE

This paper explains the concept of edge detection using Sobel Operator and focuses on detecting the edges of the normal and disease affected images. The hardware is implemented using Xilinx Spartan 3 FPGA Kit. The entire process is coded using VHDL. As Sobel edge detection operator is insensible to noise this method reduces the system complexity. By comparing the device utilization summary with other Xilinx Spartan 3 kits, it has been observed that the area is optimized using Spartan 3 Part-XC3S200. This design is able to locate the edges of the input image properly. Pipelining can be used to improve the processing speed and efficiency of the system. Also processing speed can be taken into consideration for FPGA kit.

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