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An Efficient Implementation of Speed-PFC of Interleaved Converter FED BLDC Motor Drive System

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Abstract— This project proposes a power factor corrected (PFC) interleaved converter- fed brushless direct current (BLDC) motor drive.Back Emf sensing method is proposed which reduces switching loss and no attenuation.Speed control is done by controller which makes the corrected PWM signals.And also efficiency is improved by using interleaved converter.

Keywords— Interleaved converter, Back Emf sensing, PID controller

INTRODUCTION

Efficiency and cost are the major concerns in the development of low-power motor drives targeting household applications such as fans, water pumps, blowers, mixers, etc. The use of the brushless direct current (BLDC) motor in these applications is becoming very common due to features of high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems. These BLDC motors are not limited to household applications, but these are suitable for other applications such as medical equipment, transportation, HVAC, motion control, and many industrial tools. A BLDC motor has three phase windings on the stator and permanent magnets on the rotor. The BLDC motor is also known as an electronically commutated motor because an electronic commutation based on rotor position is used rather than a mechanical commutation which has disadvantages like sparking and wear and tear of brushes and commutator assembly, Power quality problems have become important issues to be considered due to the recommended limits of harmonics in supply current by various international power quality standards such as the International Electro technical Commission (IEC). For class-A equipment (<600 W, 16 A per phase) which includes household equipment, IEC 61000-3-2 restricts the harmonic current of different order such that the total harmonic distortion (THD) of the supply current should be below 19%. A BLDC motor when fed by a diode bridge rectifier (DBR) with a high value of dc link capacitor draws peaky current which can lead to a THD of supply current of the order of 65% and power factor as low as 0.8. Hence, a DBR followed by a power factor corrected (PFC) converter is utilized for improving the power quality at ac mains. Many topologies of the single-stage PFC converter are reported in the literature which has gained importance because of high efficiency as compared to two-stage PFC converters due to low component count and a single switch for dc link voltage control and PFC operation. The choice of mode of operation of a PFC converter is a critical issue because it directly affects the cost and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the two modes of operation in which a PFC converter is designed to operate. In CCM, the current in the inductor or the voltage across the intermediate capacitor remains continuous, but it requires the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, which is not cost-effective. On the other hand, DCM requires a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch; hence, DCM is preferred for low-power applications. The conventional PFC scheme of the BLDC motor drive utilizes a pulsewidth-modulated voltage source inverter (PWM-VSI) for speed control with a constant dc link voltage. This offers higher switching losses in VSI as the switching

losses increase as a square function of switching frequency. As the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed control is achieved by the variable dc link voltage of VSI. This allows the fundamental frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses. Singh and Singh [11] have proposed a interleavedconverter feeding a BLDC motor based on the concept of constantdc link voltage and PWM-VSI for speed control which has high switching losses.

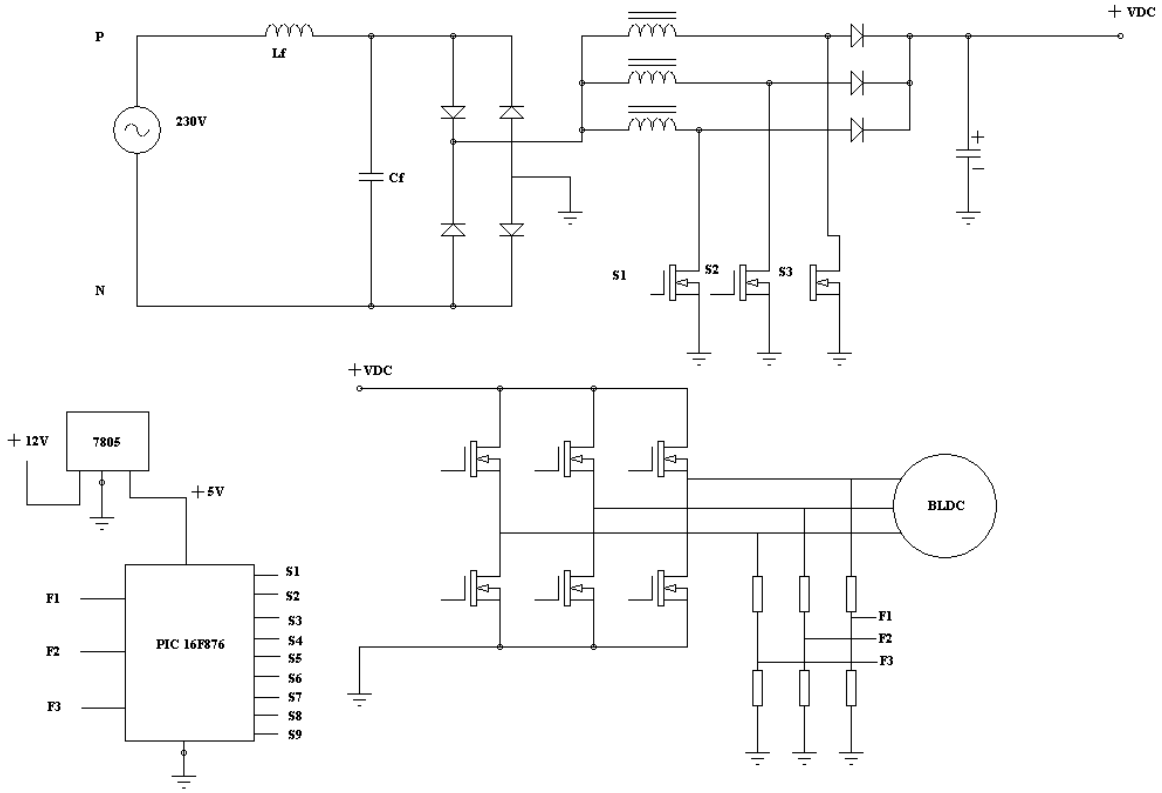


FIG. 1. PROPOSED BLDC MOTOR DRIVE WITH FRONT-END INTER LEAVED CONVERTER.

The circuit diagram for An Efficient Implementation Of Speed -PFC Of Interleaved Converter Fed BLDC Motor Drive System is shown in fig 1.In this diagram consists of Ac source, interleaved converter, PWM generator, back EMF sensing, Error amplifier, PID controller, and BLDC motor drives. By applying AC source voltage to the interleaved converter.it converts Ac into DC supply by using both interleaved converterthe output of the Dc supply is converted into the three phase Ac supply by using three phase inverter and given to the BLDC motor drive.

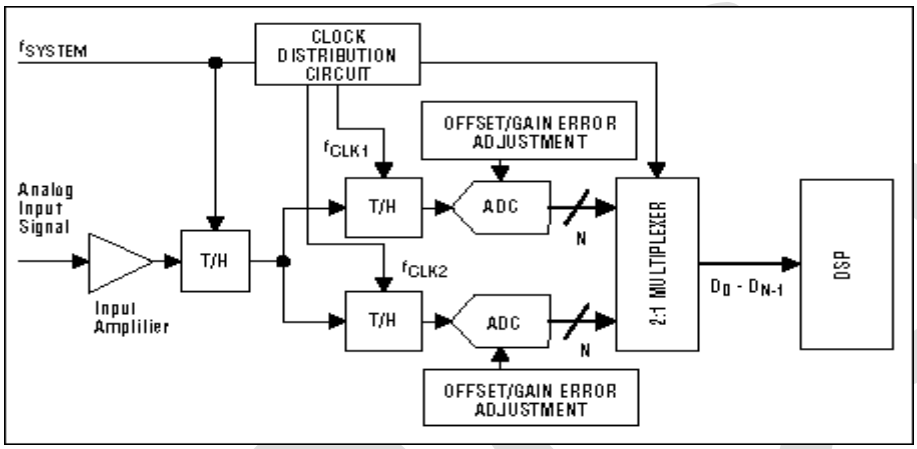
This paper presents a interleaved converter-fed BLDC motor drive with variable dc link voltage of VSI for improved power quality at ac mains with reduced components.

INTERLEAVED CONVERTER:

- It is a method of paralleling converters.
- It has additional benefits when comparing the general approaches of paralleling converters.
- Widely used in personal computer industry to power central processing units.

TIME INTERLEAVING:

For very-high-speed applications, time interleaving increases the overall sampling speed of a system by operating two or more data converters in parallel. This sounds reasonable and straightforward but actually requires much more effort than just paralleling two ADCs. Before discussing this arrangement in detail, compare the sampling rate of a time-interleaved system with that of a single converter. As a rule of thumb, operating N number of ADCs in parallel increases the system's sampling rate by approximately a factor of N. Thus, the sampling (clock) frequency for an interleaved system that hosts N ADCs[1] can be described as follows:



$$f_{SYSTEM\_CLK} \approx \sum_{n=1}^{n=N} f_{CLK\_ADC(n)}$$

The simplified block diagram in Figure 1 illustrates a single-channel, time-interleaved DAQ system in which two ADCs double the system's sampling rate. This rate (f_{SYSTEM_CLK}) is a clock signal at twice the rate of $f_{CLK1} = f_{CLK2}$. Because f_{CLK1} is delayed with respect to f_{CLK2} by the period of f_{SYSTEM_CLK}, the two ADCs sample the analog input signals alternately, producing an overall sample rate equal to f_{SYSTEM_CLK}. Each converter operates at half the sampling frequency.This simplified block diagram depicts a two-step, time-interleaved ADC system for high-speed data acquisition.

BRUSHLESS DC ELECTRIC MOTOR:

(**BLDC motors**, **BL motors**) also known as **electronically commutated motors** (ECMs, EC motors) are synchronous motors that are powered by a DC electric source via an integrated inverter/switching power supply, which produces an AC electric signal to drive the motor. In this context, AC, alternating current, does not imply a sinusoidal waveform, but rather a bi-directional current with no restriction on waveform. Additional sensors and electronics control the inverter output amplitude and waveform (and therefore percent of DC bus usage/efficiency) and frequency (i.e. rotor speed).

PWM GENERATION:

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a modulation technique that controls the width of the pulse, formally the pulse duration, based on modulator signal information. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors. In addition, PWM is one of the two principal algorithms used in photovoltaic solar battery chargers, the other being

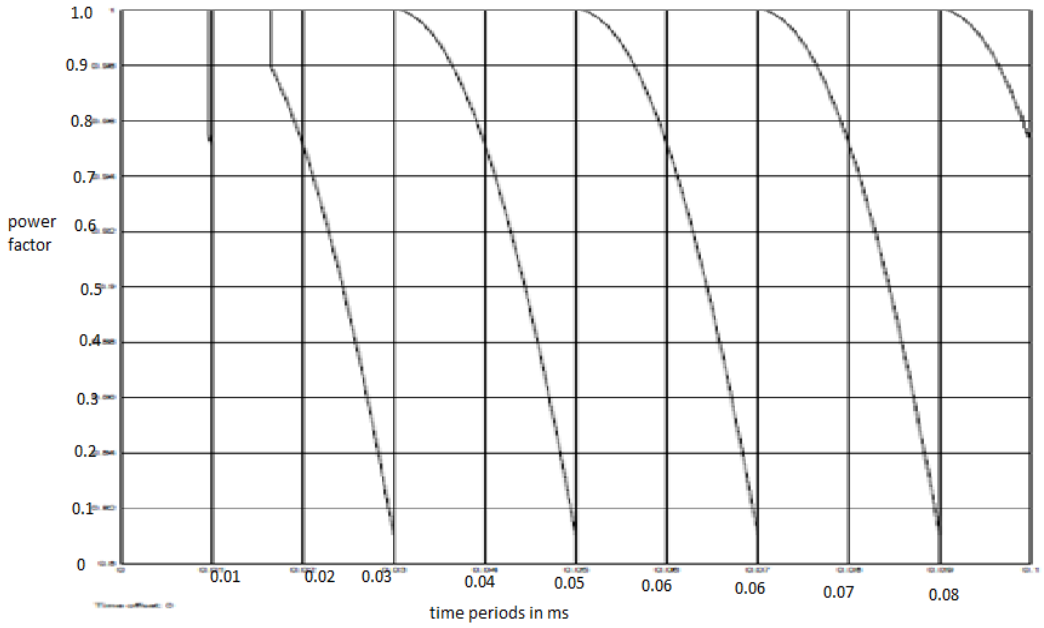
MPPT.The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load.

POWER FACTOR CORRECTION:

PFC (power factor correction; also known as power factor controller) is a feature included in some computer and other power supply boxes that reduces the amount of reactive power generated by a computer. Reactive power operates at right angles to true power and energizes the magnetic field. Reactive power has no real value for an electronic device, but electric companies charge for both true and reactive power resulting in unnecessary charges. PFC is a required feature for power supplies shipped to Europe.In power factor correction, the power factor (represented as "k") is the ratio of true power (kwatts) divided by reactive power (kvar). The power factor value is between 0.0 and 1.00. If the power factor is above 0.8, the device is using power efficiently. A standard power supply has a power factor of 0.70-0.75, and a power supply with PFC has a power factor of 0.95-0.99.Is there a way to correct this inefficient use of current? The answer is yes, by using power factor correction capacitors. These capacitors are wired in parallel with the load. They may be installed at the service entrance of the building or be dedicated to a specific device with a low power factor.PF correction capacitors are sized by the amount of KVAR they are able to correct. To determine proper sizing, the PF for the building or the device must be measured under normal operating conditions. A target PF such as 95 percent is selected.

REMAINING CONTENTS

SIMULATION RESULT OF SPEED-PFC OF INTERLEAVED CONVERTER FED BLDC MOTOR DRIVE SYSTEM:



The performance of the proposed BLDC motor drive is simulated in MATLAB/Simulink environment using the Sim-Power-System toolbox. The performance evaluation of the proposed drive is categorized in terms of the performance of the BLDC motor and BL interleaved converter and the achieved power quality indices obtained at ac mains. The parameters associated with the BLDC motor such as speed (N), electromagnetic torque (*Te*), and stator current (*ia*) are analyzed for the proper functioning of the BLDC motor.

Parameters such as supply voltage (*Vs*), supply current (*is*), dc link voltage (*V*dc), inductor's currents (*i*Li1, *i*Li2), switch voltages (*V*sw1, *V*sw2), and switch currents (*i*sw1, *i*sw2) of the PFC BL interleaved converter are evaluated to demonstrate its proper functioning.

Moreover, power quality indices such as power factor (PF), displacement power factor (DPF), crest factor (CF), and THD of supply current are analyzed for determining power quality at ac mains. *Steady-State Performance* The steady-state behaviour of theProposed BLDC motor drive for two cycles of supply voltage at rated condition (rated dc link voltage of 200 V) is the discontinuous inductor currents (*i*Li1 and *i*Li2) are obtained, confirming the DICM operation of the BL buck–boost converter. The performance of the proposed BLDC motor drive at speed control by varying dc link voltage from 50 to 200 V. The harmonic spectra of the supply current at rated and light load conditions, i.e., dc link voltages of 200 and 50 V, also shown in Fig. 7(a) and (b), respectively, which shows that the THD of supply current obtained is under the acceptable limits of IEC 61000-3-2.The dynamic behaviour of the proposed drive system during a starting at 50 V, step change in dc link voltage from 100 to 150 V, and supply voltage change from 270 to 170 Voltage.

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If acknowledgement is there wishing thanks to the people who helped in work than it must come before the conclusion and must be same as other section like introduction and other sub section.

CONCLUSION

A PFC interleaved converter-based VSI-fed BLDC motor drive has been proposed targeting low-power applications. A new method of speed control has been utilized by controlling the voltage at dc bus and operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor for reducing the switching losses in VSI. The front-end BL interleaved converter has been operated in DICM for achieving an inherent power factor correction at ac mains. A satisfactory performance has been achieved for speed control and supply voltage variation with power quality indices within the acceptable limits of IEC 61000-3-2. Moreover, voltage and current stresses on the PFC switch have been evaluated for determining the practical application of the proposed scheme. Finally, an experimental prototype of the proposed drive has been develop to validate the performance of the proposed BLDC motor drive under speed control with improved power quality at ac mains. The proposed scheme has shown satisfactory performance, and it is a recommended solution applicable to low-power BLDC motor drives.

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