



Performance of Micro Controller Based Multilevel Inverter for Single Phase Induction Motor

Richa Bhargava, Amit Shrivastava and Anula Khare

*Department of Electrical & Electronics Engg.
Oriental College of Technology, Bhopal, (MP)*

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ABSTRACT: This paper presents a micro controller based control of multilevel inverter for single phase Induction motor. Pulse Width Modulation (PWM) techniques; introduced three decades ago, are the most used methods to control the voltage and frequency supplied to electrical AC machines. Multi level inverter has gained attention in recent years due to its high power capability associated with lower output harmonics. Several multilevel topologies have been reported in the literature and this paper focuses on cascaded H-bridge multilevel inverter built to implement the proposed conduction table with five voltage levels. Gating signals are generated using PIC microcontroller. The performance of the inverter has been analyzed and compared with the result obtained from theory. A scheme based on 5-level PWM inverter, which control a high performance 8-bit standard microcontroller with gate driver circuit and additional hardware is used, which allows a flexible and economical solution. The output voltage can be varied in a large range and with a good resolution. Experimental data obtained from an induction motor drive will be presented.

Key word:-PWM, microcontroller, multilevel inverter, induction motor.

I. INTRODUCTION

Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage source inverter particularly in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in organization and avoids. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power switches when compared to ordinary cascaded multilevel inverter.

The induction motor accepted in variable speed drives due to its distinguished advantages of easy construction as well as low cost machine. This asynchronous machine uses some internal parts that need maintenance or

replacement. The control voltage applied to the asynchronous machine can transform the expression of electromagnetic torque of the asynchronous machine to practically the torque of the D.C. machine. In this work, the decoupling V_{ds} and V_{qs} are used to control the flux particularly in the course of the component I_{ds} and I_{qs} , which sharply to the suggestions of decoupling of the dependent excited D.C motor. In this to determine the couple, the junction temperature, rotor flux and the stator pulsation. The control of induction motor can transform the expression of electromagnetic torque of to nearly the torque of the DC machine. Moreover, with multilevel inverter PWM and application of rotor flux, the voltage applied to the Induction Motor (IM) solicits a modulator stage. This stage adds to the signal processing (orders IGBTs of the inverter of the type H) time and consequently limits the reactions of the control system, and hence the torque and speed response time. Also a hardware implementation of multilevel convertor with microcontroller control methodology for single phase induction motor system and its implementation in term of programming and code in real time operating system [5].

II. MULTILEVEL PWM INVERTER

The multilevel PWM inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages in stepped waveform. The commutation of the switches allows the addition of the capacitor voltages which reaches the high voltage level at the output, while the power semiconductors withstand only with reduced voltage. A five-level PWM inverter generates an output voltage with five values (levels) with respect to the negative terminal of the capacitor. By considering that ‘n’ is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load ‘K’ is defined by:

$$K = 2m + 1 \quad \dots(1)$$

The number of steps p in the phase voltage of a single-phase load in wyes connection is given by:

$$p = 2k+1 \quad \dots (2)$$

The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveforms, it results to reduction in harmonic

distortion. However, a high number of levels results in increasing the complexity and also introduce voltage imbalance problems [1].

Three different topologies have been proposed for multilevel inverters as diode-clamped (neutral-clamped), capacitor-Clamped (flying capacitors) and cascaded multicell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination and space-vector modulation (SVM).

The most attractive features of multilevel inverters are as follows:

- [1] It can generate output voltage with extremely low distortion.
- [2] It draws input current with very low distortion.
- [3] It generates smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, by using sophisticated modulation methods, CM voltages can be eliminated [8].
- [4] They can operate with a lower switching frequency.

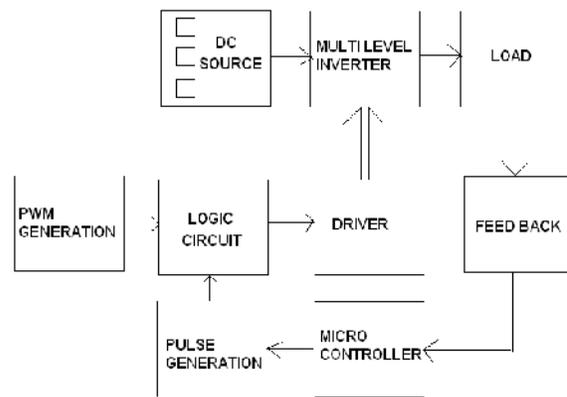


Fig.1. Block diagram of proposed 5-level inverter.

The early forms of DC to AC conversion are derived from the basic buck converter, where a power semiconductor is used to switch a DC signal into a square wave (Square Wave Inverter). With the introduction of power storage components, such as inductors and capacitors, this square wave will resemble a rough sinusoidal wave. The desired sinusoidal output can be further refined with the use of logic control on the semiconductors. It enables the positive and negative peaks of the square wave to be delayed (Phase Shifted

Square Wave inverters), by creating a zero level. All these adjustment were made in the aid of producing a perfect sinusoidal output or in other words to decrease the Total Harmonic Distortion (THD).

The PWM inverter further refines the conversion of the DC input to an AC output. This advancement in inverter was not possible until recent semiconductor technology advancements. In this particular project, the semiconductors must have a high power rating combined with a high switching frequency.

PWM inverters use high-speed semiconductor switches to switch the DC signal at varied time intervals, this will create varied pulse widths, hence the name Pulse Width Modulator [5-6].

Three voltage levels can be obtain using two voltage sources and two H-bridges. If V_{dc} is the voltage of first H-bridge H_1 then second H-bridge H_2 is supplied 0.5 of V_{dc} . appropriate IGBT are switched on in order to get

different voltage level. $0.5 V_{dc}, V_{dc}, 1.5 V_{dc}, 0$. Which are repeated continuity and IGBT sequence is inverted for negative values.

III. HARDWARE IMPLEMENTATION

To Capture and Compare the PWM modules version of the modulator suitable for the voltage control, accepts as:

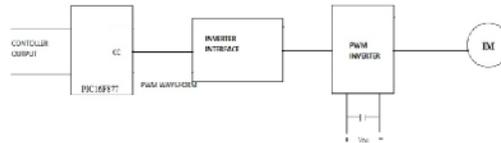


Fig. 2. Block diagram of proposed 5-level PWM inverter.

Inputs the voltage demand in dqstator coordinates (U_d and U_q), and generates the on-line single-phase PWM digital waveforms, which drive the power stages. In the proposed solution, the modulator hardware is just a 8-bit microcontroller with minimum additional logic, which provides the interface with power stage. The microcontroller is a 16F877A microcontroller for specially designed for complex, real-time control applications. It shares a common, register-based architecture core that eliminates the accumulator bottleneck and enables fast context switching. Although the 16F877A microcontrollers are 8-bit architecture, all

devices have bit, byte, word and 8-bit operations. The motion control family has peripherals that are optimized for single-phase AC induction motor control and power inverter applications. These devices have a unique peripheral, the capture and compare module (CCM), which greatly simplifies the control with 5-level PWM inverter gate driver circuit and external hardware used for generating single-phase pulse width modulation waveforms. The capture and compare carrier-overlapping PWM pulses with resolutions of 250 ns (with a 16 MHz oscillator). Once initialized, the CCM require to change PWM duty cycles.

Table: 1 Proposed Conduction table of cascaded H-bridge 5-level PWM inverter.

S1	S2	S3	S4	S5	S6	S7	S8	OUTPUT
1	0	0	1	0	0	1	1	$0.5V_{DC}$
0	0	1	1	1	0	0	1	V_{DC}
1	0	0	1	1	0	0	1	$1.5 V_{DC}$
0	0	1	1	1	0	0	1	V_{DC}
1	0	0	1	0	0	1	1	$0.5 V_{DC}$
0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	1	1	$-0.5 V_{DC}$
0	0	1	1	0	1	1	0	$-V_{DC}$
0	1	1	0	0	1	1	0	$-1.5 V_{DC}$
0	0	1	1	0	1	1	0	$-V_{DC}$
0	1	1	0	0	0	1	1	$-0.5 V_{DC}$

The CCM features programmable Switching (or carrier) frequency up to 1 kHz, duty cycle and dead time. The dead time generator (included in the CCM peripheral) prevents the complementary outputs from being turned on at the same time, in order to avoid a short circuit in one leg of the power inverter. This peripheral also has all programmable high drive capability outputs for each phase. The outputs have programmable polarity, or may be forced high or low. Fig. 3 shows the CCM how to produces the PWM waveforms. The register determines the switching frequency. The CC-COUNTER register is

a8-bit counter which is clocked every state machine. When the counter is running, it continuously counts up and down between. When the counter equals the outputs are complemented, so, this register set the pulse width. Each time the CC-COUNTER register reaches the CC-RELOAD value, an interrupt is generated (PI-Interrupt). This interrupt is used to CC-COMP register values (if needed) [2].

- Capture is 16-bit, max. Resolution is 12.5 ns
- Compare is 16-bit, max. Resolution is 200 ns
- PWM max. Resolution is 10-bit

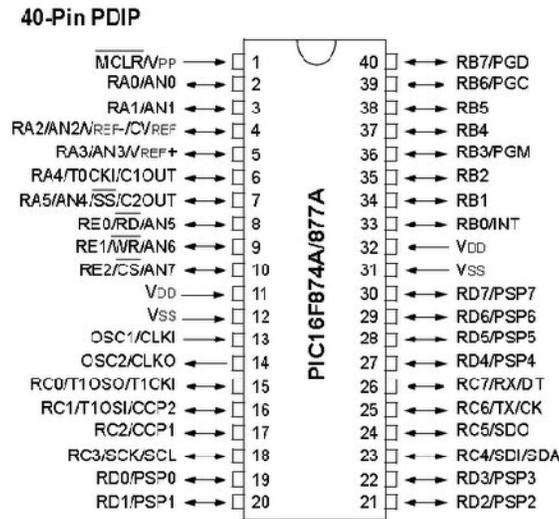


Fig. 3. Pin description of PIC16F877A.

IV. EXPERIMENTAL RESULTS

This section presents the experimental results of the asymmetric five-level inverter employing CO PWM A technique. PIC16F877A is used to generate trigger pulses for the semiconductor devices (IGBT) used in the circuit. The opto coupler used is PC 923, which is an optically coupled gate that combines a Gas plight emitting diode. Fig.7 shows the hard ware set-up of Cascaded H-bridge 5-level inverter for single phase induction motor. Fig.6 shows the experimental output waveform of Gate driver circuit and Fig.5 shows the experimental

output waveform of five-level inverter.0.5 Hp induction motor is connected to the system and successfully run using 5-level inverter techniques the supply voltage under take is 100V maximum in total. The motor is tested under no load condition. The hardware and power components run in under operating temperature in normal and industrial environment. Different input voltages are applied to check the motor performance for suitable running with the help of solar power as input source in further uses. Fig.7 shows complete hardware model in below.

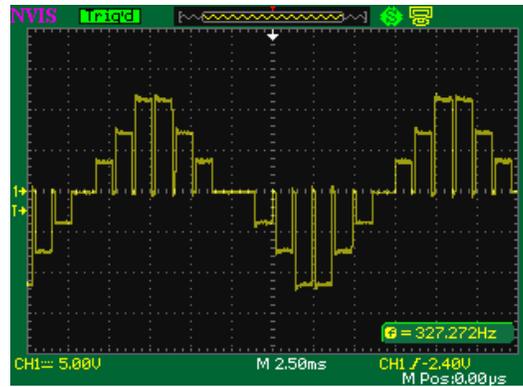


Fig. 5. Experimental output waveform of 5-level PWM inverter.

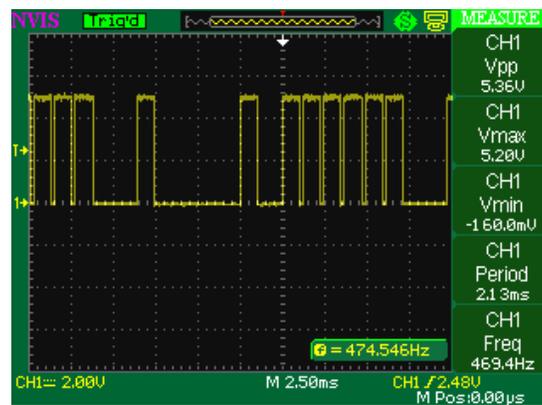


Fig. 6. Experimental output waveform of gate driver circuit.



Fig.7. Complete hardware set-up cascaded H-bridge 5-level PWM inverter for single phase IM.

VI. CONCLUSION

A PWM modulator, suitable for voltage control is tested on a 0.5 H.P. single-phase induction motor fed by an IGBT 5-level PWM inverter. The solution is based on a high performance 8-bit microcontroller with gate driver circuit and additional hardware. The implemented algorithm is very efficient, leaving enough time to implement. High switching frequencies can be achieved with fine resolutions within a large output frequency range.

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