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Research Article

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A novel inverter design with optimized multilevel programmed drive sequences

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Abstract This paper presents a novel inverter topology. A four-level inverter design is presented. A circuit topology is implemented that requires a single isolation supply for gate drive of all drive MOSFETs. The drive sequences are multilevel counter parts of binary programmed pulse width modulation, in that the set of integral values for voltage input to inverter circuit has four members rather than two as in the case of binary. These sequences are optimized using mixed integral linear programming tool of Matlab. The resulting sequences are tested on circuit of inverter in Pspice using SPLS interface. The harmonic contents comparison of the proposed technique is performed with its binary counterpart inverter, which confirms the performance superiority of the presented technique.

Keywords Multilevel Inverter, Mixed Integral Linear Programming, Simulink SLPS Interface, OrCad Pspice, Harmonic Distortion.

1. Introduction

Multilevel inverters play a vital and significant role in the development of industry as well as household. They not only result in outputs with very reduced harmonic contents and harmonic distortion but also mitigate the need of high power rating devices and transformers in many cases, as compared with their two-level counterparts. They allow the series and parallel combinations of solid state devices and can provide higher currents and voltages, ultimately resulting in high power devices with reduced switching loses. Although these devices present a challenge of complex switching sequences, however, the availability of cheap and high speed digital processing devices such as micro controllers and field programmable gate arrays (FPGA) has eradicated this issue and there is a boom in the research and development of these inverters for over a decade now.

One of the active area of research in multilevel technology is the optimization of the switching sequences. There is a lot of research available in the literature pertaining switching sequence optimization subjected to various constraints. An Intelligent optimization technique for real-time harmonics reduction in multilevel inverters is presented in [1], where particle swarm optimization algorithm is used to find the solution for the set of equations where the input voltages are the known variables and the switching angles are the unknown variables and the artificial neural networks is trained to store solutions without excessive memory storage requirements. Harmonic distortion optimization of multilevel PWM inverter using genetic algorithms is detailed in [2], where a multi-PWM modulation is generated to minimize total harmonic distortion to almost zero. Asymmetrical cascaded multi-level inverter using optimization angle control technique is presented in [3]. Selective harmonic optimization for flexible single-phase operation of Cascaded H-bridge multilevel inverters is presented in [4]. Harmonic elimination of multilevel inverters by moth-flame optimization algorithm is explained in [5], which is a recently developed heuristics method. Particle swarm optimization based modified selective harmonic elimination method for cascaded H-bridge multilevel inverters is presented in [6]. Performance analysis of multilevel inverter with battery balanced discharge function and harmonic optimization with genetic algorithm is detailed in [7]. Ant Colony Optimization applied to selective harmonic elimination in multilevel inverters is

explained in [8]. Optimal pulse width modulation of cascade nine-level inverter for medium voltage high power industrial AC drives is presented in [9].

Other than the optimization technique, using a hybrid simulation of a system using best features of various simulation tools is key for advance simulation methodology. In this regard, Simulink-Pspice co-simulation of power electronics generates the best results. An interface known as SLPS has been developed by Cadance and Mathworks for this purpose and has been successfully deployed for various research projects such as research on modeling control module of DC-DC converter for Simulink using SLPS tool is present in [10]. Pspice and Simulink co-simulation for high efficiency DC-DC converter using SLPS interface software is described in [11].

This research paper presents a novel multilevel inverter topology. An optimization problem for this multilevel inverter is developed and optimized sequences are obtained using genetic algorithm in Matlab. The generated sequences are applied to the power circuit built in Cadence-Pspice using SLPS interface. Results are obtained in Simulink and observer for harmonic distortion and success and feasibility of the proposed methodology is verified in that simulation.

2. Overview of the Inverter Topology

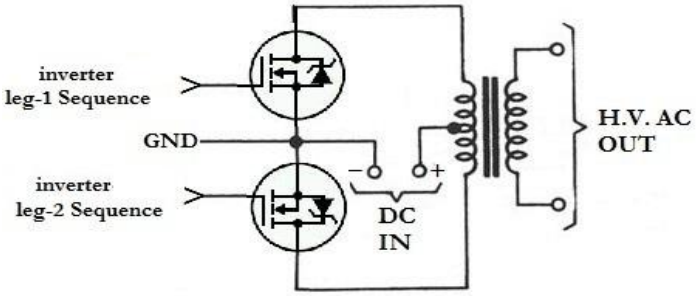

Figure 1: Single level inverter topology

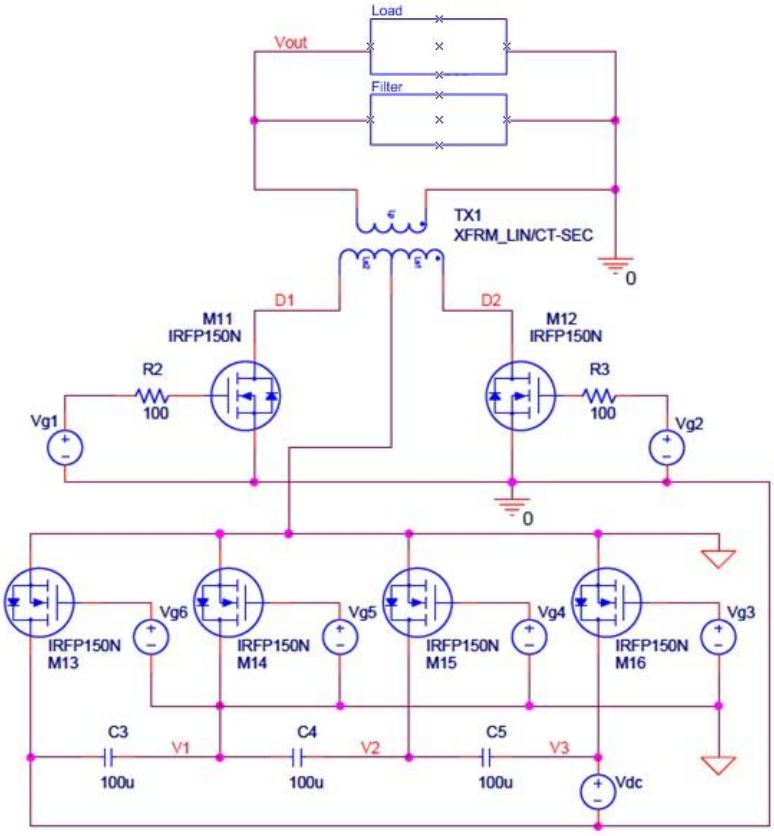

Figure 2: An overview of four level the inverter topology in Pspice

Figure 1 shows the circuit diagram of single level inverter topology, which requires a single isolation supply for gate drive of either MOSFET. This single level topology has been extended to four level topology in Figure 2 and can easily be generalized to n-level inverter.

In Figure 2, input voltage V_d has been divided into four voltage levels using capacitive voltage divider. Each of these levels can be negated by the switching of alternate MOSFETs corresponding to the base topology of Figure 1. Hence the lower four MOSFETs in Figure 2 represent four voltage level and any of the level can be selected by turning that MOSFET on and turning all remaining of these four MOSFETs. Now MOSFETs corresponding to the base topology can be tuned on and off and decide the polarity of the voltage level selected for the output voltage.

3. Optimized Multilevel Programmed Sequences Generation Problem

The optimized Multilevel Programmed sequence generation problem involves generation of sequence, such that if this sequence is used as a gate drive signal for the inverter MOSFET board in Figure 2 then the output of the inverter has desired fundamental amplitude and desired harmonic contents. The Multilevel Programmed sequence is selected to have the quarter wave symmetry; hence we need to design the sequence for interval $[0, \pi/2]$ and extend it accordingly. The quarter wave interval is subdivided into N bins for the Multilevel Programmed sequence as shown in Figure 3. We have to select a binary value v_θ for each bin such the resulting Multilevel Programmed sequence has maximum fundamental component and selected harmonic contents removed or minimized in its Fourier spectrum.

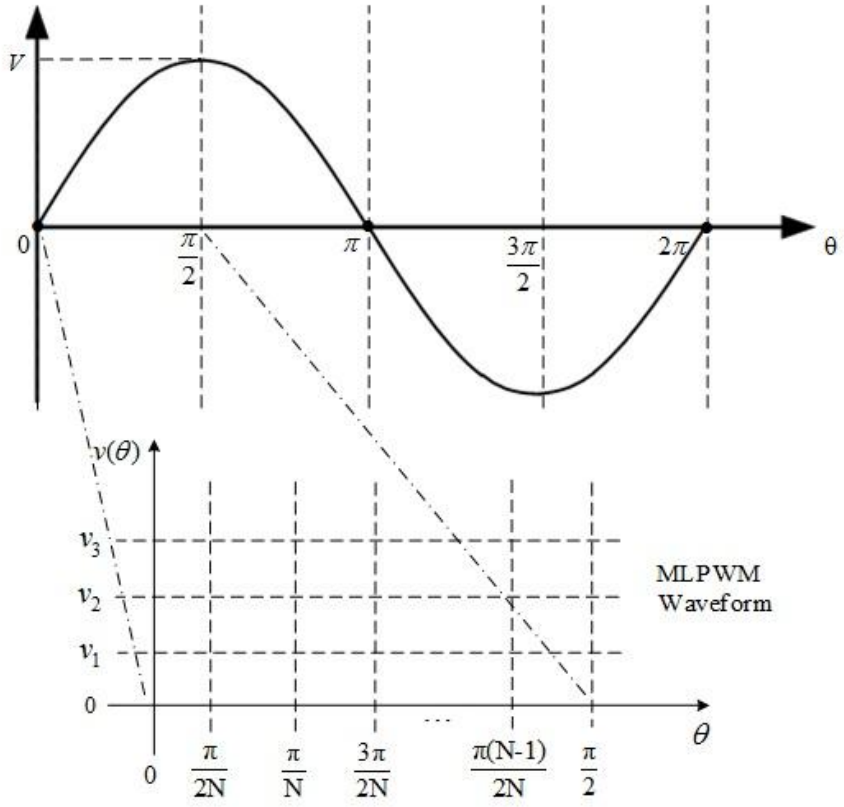

Figure 3: Multilevel programming problem formulation

The harmonic contents of Multilevel Programmed sequence are given by Equation 1.

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} v_i \sin(n\theta)\, d\theta \tag{1}$$

The above equation can be written as:

$$b_n = \frac{4}{\pi}\sum_{i=0}^{i=N-1}\int_{i\frac{\pi}{2N}}^{(i+1)\frac{\pi}{2N}} v_i \sin(n\theta)\,d\theta, \text{ where } \beta_0 = 0 \text{ and } \beta_N = \frac{\pi}{2} \quad (2)$$

Rearranging the terms, we get:

$$b_n = \frac{4}{\pi}\left[-\sum_{i=0}^{i=N-1}\frac{v_i\cos(n\theta)}{n}\Bigg|_{i\frac{\pi}{2N}}^{(i+1)\frac{\pi}{2N}}\right] \quad (3)$$

$$b_n = \frac{4}{\pi n}\left[\sum_{i=0}^{i=N-1} v_i\left[\cos\left(ni\frac{\pi}{2N}\right)-\cos\left(n(i+1)\frac{\pi}{2N}\right)\right]\right] \quad (4)$$

$$b_n = \frac{4}{\pi n}\left[\sum_{i=0}^{i=N-1} v_i\left[2\cos\left(ni\frac{\pi}{2N}+n\frac{\pi}{4N}\right)\sin\left(-n\frac{\pi}{4N}\right)\right]\right] \quad (5)$$

Where:

$$v_i \in \{0, V_\Delta, 2V_\Delta, 3V_\Delta\}, \text{ where } V_\Delta = \frac{V_d}{N} \quad (6)$$

The Multilevel Programmed sequence generation problem can be formulized as a Mixed-Integer Linear Programming (MILP) optimization problem given by Equation 2.

$$\max_{v_\theta} b_1 = \frac{4}{\pi}\left[\sum_{i=0}^{i=N-1} v_i\left[2\cos\left(i\frac{\pi}{2N}+\frac{\pi}{4N}\right)\sin\left(-\frac{\pi}{4N}\right)\right]\right] \quad (7)$$

Subjected to:

$$b_k = \frac{4}{\pi k}\left[\sum_{i=0}^{i=N-1} v_i\left[2\cos\left(ki\frac{\pi}{2N}+k\frac{\pi}{4N}\right)\sin\left(-k\frac{\pi}{4N}\right)\right]\right] = 0 \quad (8)$$

$$v_i \in \{0, V_\Delta, 2V_\Delta, 3V_\Delta\} \quad (9)$$

We have selected to eliminate first 16 odd harmonics with N=50. Solving the problem using MILP solver in MATLAB. The resulting sequence is given by:

$$v_k = \{00000233112333123333333333333333333233333333333333\} \quad (10)$$

This quarter wave sequence is plotted in Figure 4.

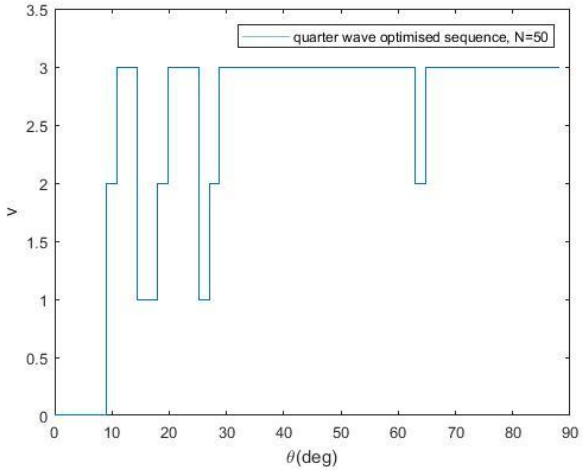

Figure 4: Optimized four level 50-bin quarter wave sequence

The quarter wave sequence can be extended to full wave sequence as shown in Figure 5.

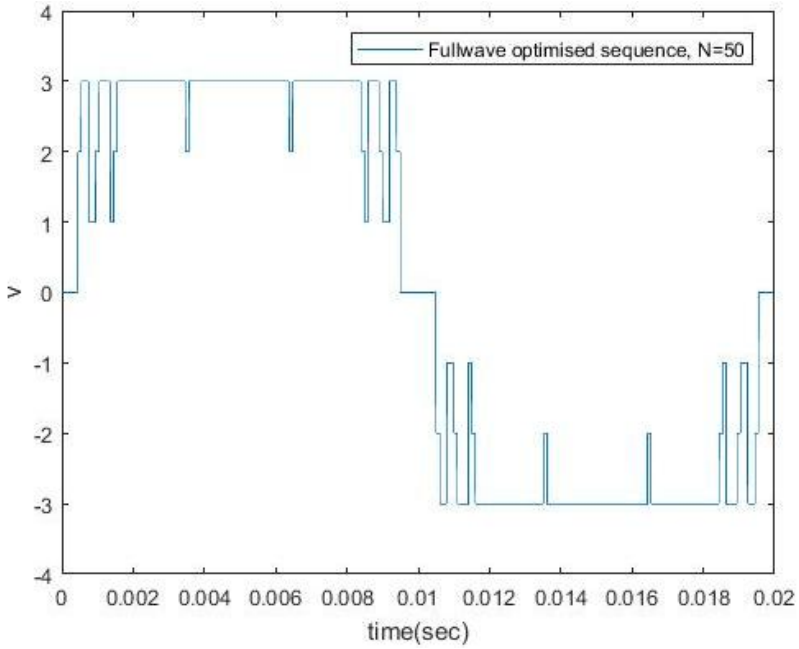

Figure 5: Optimized four level 50-bin full wave sequence.

4. Simulink-Pspice Co-Simulation using SLPS and Results

The Simulation methodology of Figure 6 is used in our paper.

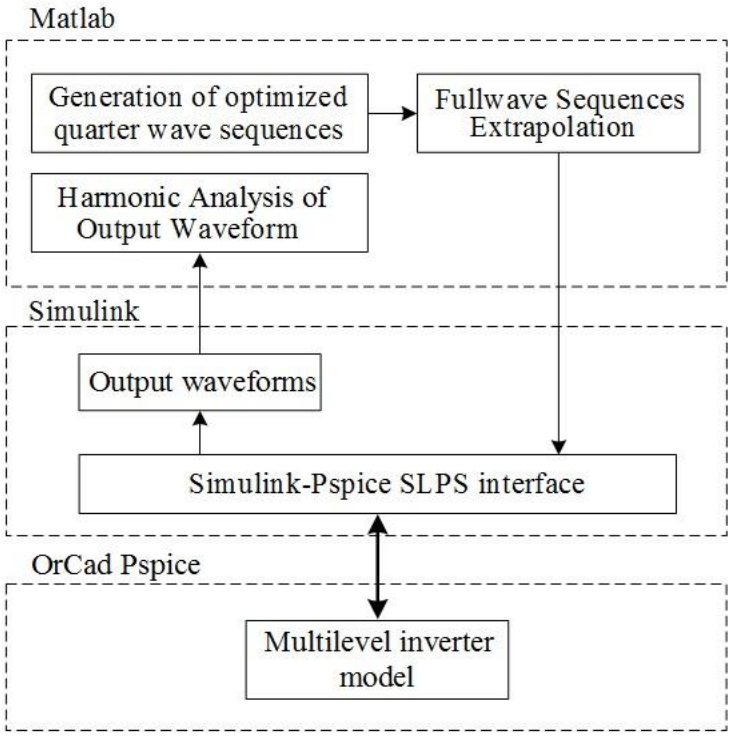

Figure 6: Block diagram of simulation methodology

The optimized sequences in Figure 5 can be transformed into gate drive sequences of Pspice model. These sequences are given by:

f_{hw} = [0 0 0 0 0 2 3 3 1 1 2 3 3 3 1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3]

vg6=[1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]

vg5=[0 0 0 0 0 0 0 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]

vg4=[0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0] (11)

vg3=[0 0 0 0 0 0 1 1 0 0 0 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1]

vg2=[1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1]

vg1=[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]

These sequences are plotted in Figure 7.

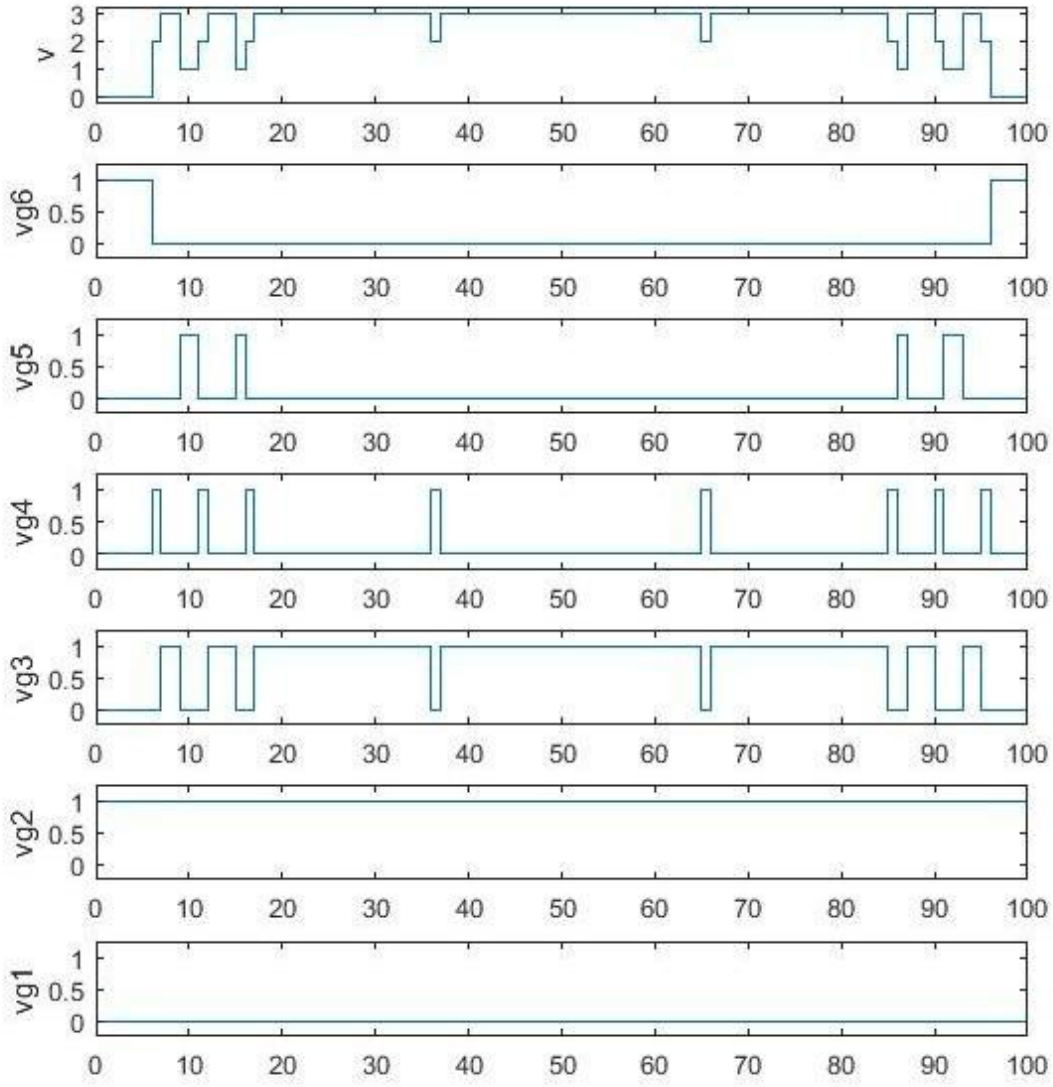

Figure 7: Gate Drive sequences for positive half cycle generation of output

The sequences of Equation 11 are generated in Matlab and exported to Simulink in accordance with Figure 6. From Simulink, they are interfaced to the Pspice model using SLPS block interface as shown in Figure 8.

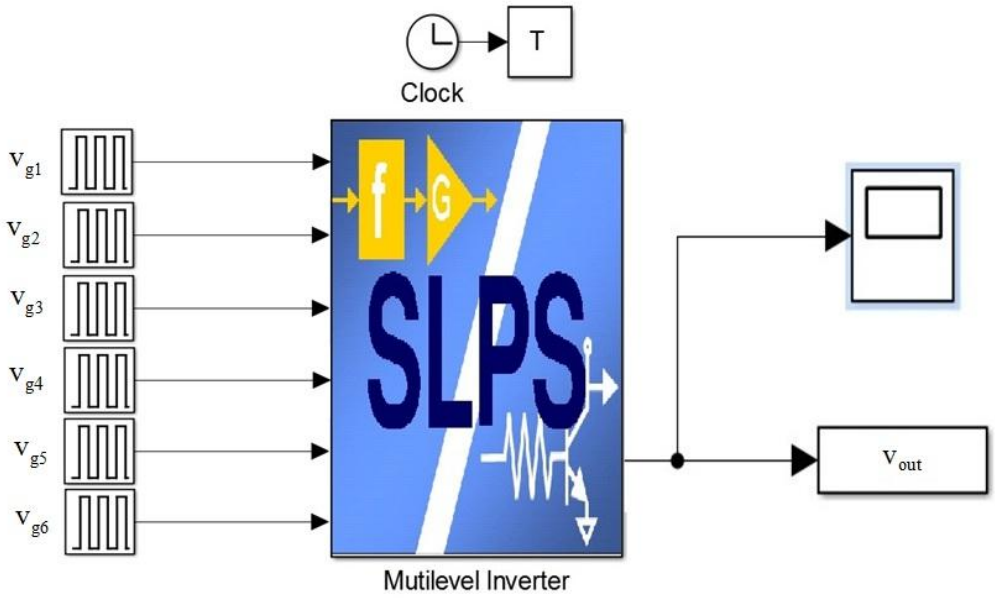

Figure 8: Simulink-Pspice co-simulation interface

From Pspice, results are exported to Simulink and back to Matlab are analyzed for the harmonic contents. Figure 9 shows the harmonic comparison with the standard Binary Programmed PWM of equal harmonics reduction and same number of bins.

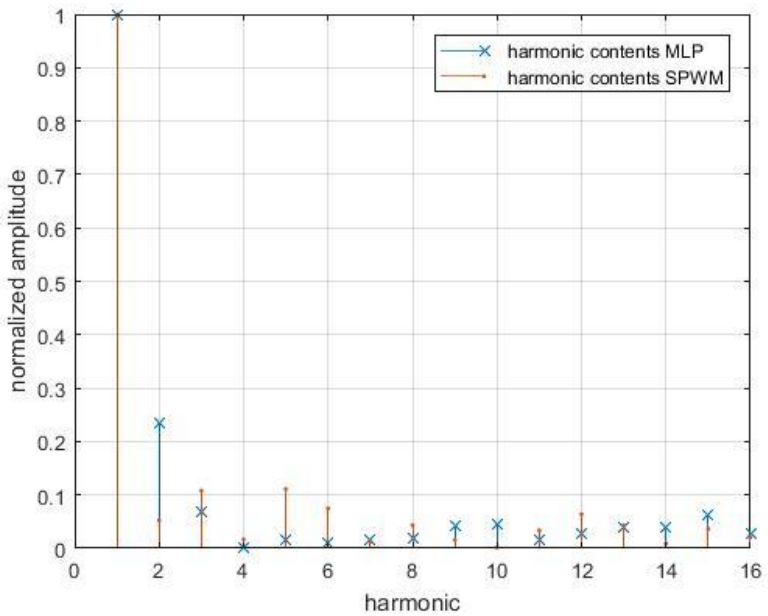

Figure 9: Harmonic content comparison

It is clearly visible in Figure 9 that the propose technique is successful in better eliminated harmonics hence resulting in reduced harmonic distortion. A 14% reduction in the harmonic distortion is observer.

5. Discussion and Conclusion

A four-level inverter topology has been presented, which requires only single isolation supply. Multilevel N-bin based gate drive sequences are synthesized. Inverter topology is implemented on Pspice and signals generated in Matlab are directed to Pspice using SLPS interface. Inverter output waveforms are observed back in Matlab for harmonic contents. Nearly 14% reduction in harmonic distortion is observed, which confirms the performance

superiority of the proposed technique. Increasing the level of inverter may further reduce the harmonic distortion of the inverter output; this study is left as a future research topic.

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